Live Demonstration: Gaussian Pyramid Extraction with a CMOS Vision Sensor

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***Abstract*—This live demonstration showcases the Gaussian pyramid with a CMOS vision sensor. The chip features a 176 × 120 pixel array in standard 0.18 μm CMOS technology. The sensing elements are designed as 3-Transistor Active Pixel Sensors (3T-APS) with in-pixel ADC and CDS. The Gaussian pyramid is extracted concurrently with a double-Euler switched-capacitor network on the same substrate, giving RMSE errors below 1.2% of FSO. The chip provides a Gaussian pyramid of 3 octaves with 6 scales each with an energy cost of 26.5 nJ/px at 2.64 Mpx/s.**

I. Introduction

Gaussian pyramid provides feature detectors with the ability to give the same response regardless the distance of the object to the camera [1]. The construction of the Gaussian pyramid comprises several downscalings of the input scene, the so-called octaves. In so doing, octave O_i is the 1/4 downscaling of the former octave O_{i-1}. Every octave is a set of images called scales which are the result of applying Gaussian kernels with increasing widths. The Gaussian pyramid generation is a very time-consuming task, which, as reported in [2], might take up to 90% of the computing time of a feature detector.

II. Chip Features

This live demonstration presents a fast and power-efficient CMOS vision sensor chip with concurrent image acquisition and Gaussian pyramid extraction that comprises an array of 176 × 120 3T-APS in standard 0.18 μm CMOS technology within an area of 5 × 5 mm^2. Photodiodes and processing circuitry are arranged in Processing Elements (PE) of 44 × 44 μm^2. Every PE contains 4 3T-APS, per-PE ADC and CDS circuitry, and the circuits of a double-Euler switched-capacitor network. The chip consumes 70 mW for scene acquisition and the extraction of a Gaussian pyramid of 3 octaves and 6 scales each. The Gaussian pyramid takes 8 ms (ADC included). This renders 26.5 nJ/px at 2.64 Mpx/s. The Gaussian pyramid is provided with less than 1.2% FSO error when compared to a software solution. Interested readers can probe references [3], [4], [5] for further details of the chip.

III. Live Demonstration Setup

Fig. 1 shows a picture of the live demonstration setup. The system comprises the chip in a PGA120 package, the lens with a focal distance of 35 mm, f1/4 as focal and mount C type, a carrier board of 15 × 6 cm^2, a DE0 Terasic FPGA to provide control signals for the chip, and a Raspberry-Pi with an ARM processor for visualization purposes.

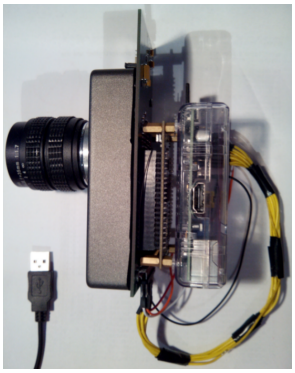

Fig. 1. Live demonstration setup.

IV. Visitor Experience

Real-time tests with the chip setup will be conducted during the conference. Visitors will interact with the system and see different scales across the Gaussian pyramid.

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