Semi-empirical RF MOST model for CMOS 65 nm technologies: theory, extraction method and validation

Rafaella Fiorelli and Eduardo Peralías

Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/Universidad de Sevilla)

Av. Américo Vespucio s/n, Seville, Spain

Abstract

This paper presents a simple but accurate semi-empirical model especially focused on 65 nm MOST (MOS transistor) technologies and radio-frequency (RF) applications. It is obtained by means of simple dc and noise simulations extracted over a constrained set of MOSTs. The fundamental variable of the model is the MOST transconductance to current drain ratio g_m/I_D. Specifically it comprises the large signal DC normalized current, all conductances and transconductances and the normalized intrinsic capacitances. As well, noise MOST characteristics of flicker noise, white noise and MOST corner frequency description are provided. To validate the referred model the widely utilized cascoded common source low noise amplifier (CS-LNA), in 2.5 GHz and 5.3 GHz RF applications is picked. For the presented set of designs different g_m/I_D ratios are considered. Finally, the model, circuit and validation results are done by computing and electrical simulations.

Keywords: MOS transistor, g_m/I_D, semi-empirical, RF, nanometer technology, 65nm CMOS, inversion level, CS-LNA.

1. Introduction

Whatever being the considered appliances of electronic devices over the enormous set of implementations existent nowadays, as in medicine, agriculture, entertainment, or environment, among many others, the majority of those existent surely contains analog RF modules. This telecommunication boom has been possible due to the continuous CMOS technology shrink that has allowed more processing capability in the same chipset. In particular, RF designer takes profit of this technology reduction using the smallest MOST length, L_o, to achieve higher transition frequencies (f_T), what is to say low power for low working frequencies.

But the utilization of the smallest L_o in nanometer technologies leads to the appearance of short-channel effects which cannot longer be considered second-order ones. In addition, to rapid develop the applications mentioned above, a reduction of the whole design time obliges the use of accurate MOST models. They should be applied even at first design stages, which notably reduces circuit redesign. Finally, a wide range of wireless applications are battery-supplied, so the requirement of low and ultra-low power is mandatory. Generally it means that the MOST biased in moderate/weak inversion regions [**?**] should be taken into consideration from the beginning of the circuit design process.

In particular, for analog RF designs, the MOST model must be correctly described among its basic electrical magnitudes and its small-signal parameters as conductances and transconductances, the MOST quasi-static capacitances and the noise parameters. Here, three possible type of MOST compact models are classified as [**?**]:

- Empirical models: those are manifolds or simple look-up tables (LUTs) fitted from measurements whose parameters are non physically based.
- Analytical models: equations or topology physical-based models. Relations between basic electrical magnitudes (currents or voltages) are given. Their parameters are extracted from fitting of measured data. Examples of these models are BSIM [**?**] or PSP [**?**], ACM, HiSIM or EKV [**? ? ?**].
- Semi-empirical or semi-analytical models: being them a mixture between empirical and analytical ones, i.e.: a) the first ones are empirical models expressed as e.g. LUTs or fitted functions to data obtained from electrical simulations with really analytical models; and b) the semi-analytical ones are analytical models whose parameters are expressed by LUTs or by fitted functions to data also obtained from electrical simulations.

Each model type has its pros and cons and its election depends on several factors. On one side there are the empirical models, generally used when none of the other models are available. Their extraction is a tiresome and time-consuming process if an accurate description is desired, that logically needs a wide set of fabricated devices. On the other side are the analytical models which includes the physical-equation based compact models. Those are the ones implemented in the electrical simulation tools, as BSIM [**?**] or PSP [**?**]. Others, as ACM, HiSIM or EKV [**? ? ?**] have been thoroughly used for years in the design stage before electrical simulations. To simplify their use, specially when working with sub-micrometer MOST,

the parameters of their fundamental equations are considered as constants for all operation regions of the MOST. However, with nanometer MOST, this simplification is not possible any more. Yet, the second and higher order effects visibly modify the MOST performance and cannot be disregarded. It means that those formerly simple models [**?**] are transformed into a bulky set of equations with parameters depending on basic electrical magnitudes. If a simplification is made, large errors appear, especially when the MOST is in subthreshold region. The complexity of employing analytical models for nanometer technologies as well as the time spent in adjusting their large number of parameters are one of the reasons of contemplate the use of semi-empirical models [**?**]. Finally the election is also fixed by the difficulties when incorporating the model in the design flux and methodology of the circuit into consideration.

In this paper it is developed a semi-empirical model for MOST. It is 1) accurate, 2) easy to use and 3) quick and simple to obtain, complying with analog designers' expected demands. It is extracted and verified for a 1.2-V 65-nm bulk CMOS technology, and developed for the minimum transistor drawn length of this technology L_o = 60 nm, in order to achieve the best transition frequency f_T. All the MOST characteristics described in this model are given as functions of the transconductance-to-current-ratio, g_m/I_D [**?**]. In particular, the curve of g_m/I_D versus the normalized current $i = I_D/(W/L_o)$ (also called inversion level) [**? ?**] is, theoretically, an intrinsic characteristic of the technology, independent of the MOST width W and it serves to indicate the inversion level of the transistor (i.e. strong, moderate or weak inversion). The g_m/I_D values are constrained to a very small range of some tens of values, roughly between 1 V^{-1} and 30 V^{-1}. In general, biasing the transistor in strong inversion means low g_m/I_D values while working in weak inversion is translated to high g_m/I_D figures. The g_m/I_D is a fundamental feature when analog low-power design is the focus, contrary to what happens when the overdrive voltage $V_{OD} = V_{GS} - V_{th}$ variable is used, because for moderate-weak inversion V_{OD} is around or below zero and small changes mean a great variation in the MOST behavior. The number of works that report the use of the commonly named "g_m/I_D design methodology" is paramount [**? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ? ?**], among many others, showing its multiple uses in different technologies and devices.

In this paper, all the MOST characteristics covered by the model and the extraction method are clearly stated. To do so, the MOST behavior is revisited in its different operation regions, as done in [**?**]; the MOST model has not been restricted to the saturation region. The relation between g_m/I_D and the drain current I_D and its normalized current i is defined. Onwards, it is evaluated the behavior of the drain-source conductance g_{ds} and bulk transconductance g_{mb} as function of g_m/I_D. Subsequently, it is here fully developed the approach of the normalized quasi-static five intrinsic capacitances versus g_m/I_D, justifying its use -already presented by the authors but shortly discussed in [**? ?**]. The development of the used MOST model is applied, as for white and flicker noise electrical parameters. As this model is focused on radio-frequency analog blocks, a special discussion regarding the behavior of the MOS transition frequency, f_T versus g_m/I_D, for all the regions of operation is included. The quasi-static characteristic of the model enable the correct design of RF circuits with working frequencies below $f_T/10$; above this limit errors would be noticed. [1]

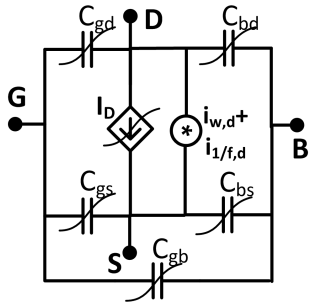

Figure 1: MOST topological model into consideration.

To sum up, the MOST presented model, for fixed length L_o = 60 nm, and gathered in LUTs,comprises: 1) a topological diagram of constitutive elements of transistor, depicted in Fig. **??**, and 2) a set of seven characteristics dependent at the first order of the gm/ID variable and practically independent of transistor size. This set has been listed bellow:

- Normalized current $i = I_D/(W/L_o) = f(g_m/I_D)$. The dependency of i with MOST W and V_{DS} is weak and in a first approximation it is here neglected.
- Bias gate source voltage $V_{GS} = f(g_m/I_D)$.The spread of V_{GS} with W and V_{DS} is low.
- $g_{ds}/I_D = f(g_m/I_D, V_{DS})$. The variation of g_{ds}/I_D with W is weak, however it is dependent of V_{DS} specially if this voltage is very small.
- $g_{mb}/I_D = f(g_m/I_D)$, as the variation of g_{mb}/I_D with W and V_{DS} is weak.
- Normalized intrinsic capacitances $c_{xx} = C_{xx}/(WL_o) = f(g_m/I_D)$, with xx={gs, gd, gb, bs, bd}. The spread of c_{xx} with W and V_{DS} is reasonably small to discard them in a first approximation.
- Thermal noise parameter $\gamma/\alpha = f(g_m/I_D)$. The variation of γ/α with W and V_{DS} is neglected.
- Flicker noise parameter $K_F = f(g_m/I_D)$. The dependency of K_F with W, V_{DS} and the working frequency is disregarded.

The actual independence of these characteristics with W is appealing for an RF designer because it can constraint the MOST model extraction to a very constrained set of W, or even, as shown in next sections, to use only one value of MOST width, with a reasonable level of error. All the assumptions

[1] The MOST model does not consider the temperature dependencies, being extracted for 25°C.

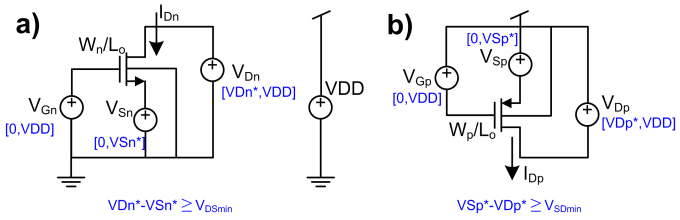

Figure 2: Test circuit used for acquisition of nMOS and pMOS characteristics.

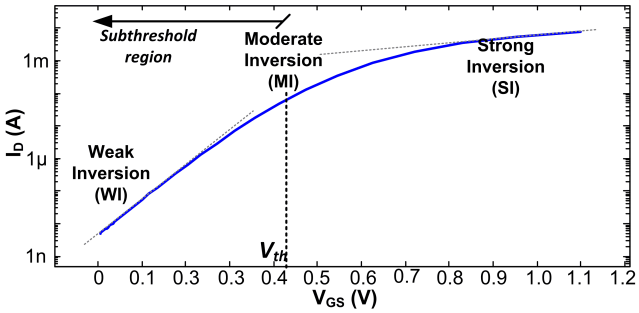

Figure 3: I_D versus V_{GS} for a nMOST with $W = 4\mu$m and $L_0 = 60$nm.

done in this work regarding the dependency of MOST characteristics with W are justified in next sections. It is specially needed for the designer in order to have clear guidelines to guide the MOST extraction and use. The final data of this reduced set of MOST is gathered together in the LUT Λ_{MOS}. The overall justifications to the above hypotheses are provided in next sections. Analogously, a discussion is presented for those MOST characteristics that depend on V_{DS} voltage.

This paper has the following organization. At the end of this section, the data acquisition scheme for all MOST characteristics is provided. Section **??** revisit the g_m/I_D characteristic with the inversion level i and its validity for our 65-nm technology. Section **??** discusses the MOST remaining conductances and transconductances. The study of the MOST normalized intrinsic capacitances is given in Section **??** and the discussion of the noise parameters is considered in Section **??**. Section **??** provides a set of CS-LNAs designs for two frequencies designed in Matlab using the MOST model here developed, including the validation via electrical simulations. Finally Section **??** concludes the work.

1.1. MOST data acquisition scheme

The designers' acquisition of MOST characteristics listed above in LUTs is proposed in the simple scheme of Fig. **??**. In it, MOST terminals gate, drain and source nodes are connected to dc voltage sources which vary conveniently, as seen in the figure. For each V_D and V_S values, V_G is swept. Two electrical analysis were done: 1) a dc sweep analysis to extract I_D, g_m, g_{ds}, g_{mb}, C_{xx} and 2) a noise analysis to obtain the flicker and white noise power spectral density seen at the drain terminal, $\overline{i^2}_{1/f,d}$ and $\overline{i^2}_{w,d}$, respectively.

The aforementioned data are easily extracted via typical SPICE-like analog electrical simulator of Cadence or Synopsys frameworks. When the characteristic consider is independent of W, the transistor used to perform the simulation can reasonably be a medium width MOST, for example W =50 μm. Otherwise, a convenient set of widths should be chosen; for the 65-nm technology here used this set can be {0.6, 1, 10 , 100} μm-. Extra technology data needed as effective SiO_2 permittivity and thickness of thin oxide to compute the normalized MOST oxide capacitance is easily obtained from technology files. For the 65 nm technology used, the MOST analytical model embedded in the electrical simulator utilized is BSIM4.

To help us to justify the hypotheses done regarding the dependence or independence of MOST characteristics with the MOST width W, an exhaustive sweep of W is performed . In all graphs, except when said, the range between $W = 0.6\mu$m to $W = 192\mu$m is reasonably covered, varying both the MOST number of fingers n_f and finger width W_f in $n_f = \{1, ..., 32\}$ and $W_f = \{0.6, ..., 6\}\mu$m. The same applies for the study of the drain and voltage ranges.

2. Drain current (I_D) and MOST transconductance (g_m) relation

As stated, throughout this paper, the MOST ratio g_m/I_D versus the normalized current $i = I_D/(W/L)$ is our variable used. The coefficient g_m/I_D is the slope of the drain current I_D versus V_G in a logarithmic scale [**?**], being I_D in a first approximation, a function of gate, source and drain voltages, its aspect ratio W/L, and second-order effects of L and W, as follows

$$I_D = \frac{W}{L} f_1(V_G, V_D, V_S; L, W), \tag{1}$$

with voltages referred to the bulk terminal. Function f_1 is usually called normalized current $i = I_D/(W/L)$. Their dependences with MOST length L and width W are explicitly noted for short or narrow channel MOS, respectively, as the variations are low.

In Figure **??** it is presented I_D versus V_{GS}. Its maximum slope is the maximum g_m/I_D ratio and, as expected, it is in the weak inversion region, when decreases until reaching the strong inversion region. As known, these zones are adequate for low and ultra-low power and efficient designs. From other point of view, in these regions, for gate voltage values V_{GS} (around 100 mV below the threshold voltage) the overdrive voltages $V_{OD} = V_G - V_{th}$ are very low, making these zones very adequate for low voltage supply operation. Finally, the g_m/I_D ratio is a measure of the efficiency to translate I_D into the transconductance g_m, because the greater g_m/I_D value the greater transconductance that can be obtained for a constant current value. As a rule of thumb [**?**], the inversion regions' limits can be approximated as: for g_m/I_D higher than 20 V^{-1} it is weak inversion; for g_m/I_D lower than 10 V^{-1}, it is strong inversion, and for g_m/I_D in the midst of this range, it is moderate inversion.

By applying the definition of transconductance g_m together with (**??**),

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L} \frac{\partial f_1(V_G, V_D, V_S; L, W)}{\partial V_G}. \tag{2}$$

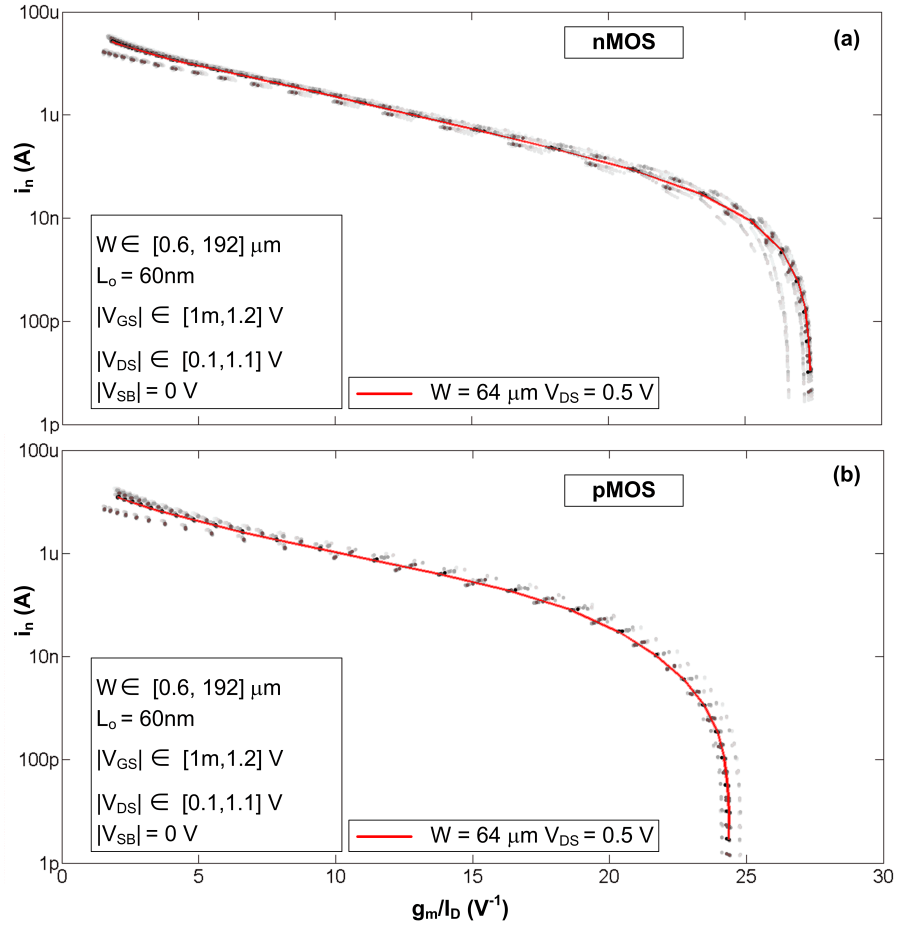

Figure 4: (a) nMOS and (b) pMOS curves of normalized drain current i versus g_m/I_D.

and from (**??**) and (**??**), the g_m/I_D ratio is

$$g_m/I_D = \frac{\partial f_1/\partial V_G}{f_1} = \frac{\partial(log f_1)}{\partial V_G} = \frac{\partial\big(log(I_D/(W/L))\big)}{\partial V_G}$$
$$= f_2(I_D/(W/L)) = f_2(i). \qquad (3)$$

Because ideally $i = f_1(V_G, V_D, V_S)$ does not depend on the transistor width W for MOS transistors with equal length, the g_m/I_D ratio is determined by i. In real world, i is slightly dependent of W, for L fixed, -because of the I_D dependence expressed in (**??**)-, thus, for different MOST W, small variations of g_m/I_D versus i are observed. From the above discussion, the curve g_m/I_D versus i is considered an inherent characteristic of each CMOS technology. This relation is strongly related to the performance of analog circuits, it gives an indication of the transistor region of operation and provides a tool for calculating transistor dimensions, as presented in [**?** **?**]. Since in our proposed model all MOST characteristics are written as function of g_m/I_D, the relation of (**??**) is flipped, and from now on the relation will be $i = f_3(g_m/I_D)$.

For the 65-nm CMOS technology studied here, previous assumptions are now verified. Figure **??** presents i versus g_m/I_D for more than forty MOST widths between 0.6 μm and 192 μm, $L = L_o = 60$ nm and for four $V_{DS} = \{0.1, 0.5, 0.8, 1.1\}$ V, either for nMOS and pMOS transistors. As expected, the observed spread of the values, when W is swept, is very tight. Hence, as said in the Introduction, for the final LUT, it is enough to extract this curve for one medium-value MOST width. Here, the same applies for V_{DS}. Because of the minor variations in these dependences with W and V_{DS}, the presented model is really useful for an analog designer.

2.1. f_T versus g_m/I_D

The intrinsic MOST transition frequency f_T gives the analog designer an idea of the frequency limits of nMOS and pMOS transistors. So, it is interesting to see the f_T response of the 65-nm nMOS and pMOS transistors for different inversion levels. To do so, lets study the definition of the transition frequency

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd} + C_{gb})} \qquad (4)$$

where C_{gs}, C_{gd} and C_{gb} are the intrinsic gate-source, gate-drain and gate-bulk capacitances of the MOST. For a fixed L_o, as g_m and the intrinsic capacitances are both proportional to W, it is expected that f_T is quasi-independent of W. With the extracted MOST data, it is observed that this hypothesis is reasonably valid for the 65-nm technology here used, as shown in Fig. **??**, for the previously stated set of W and V_{DS}.

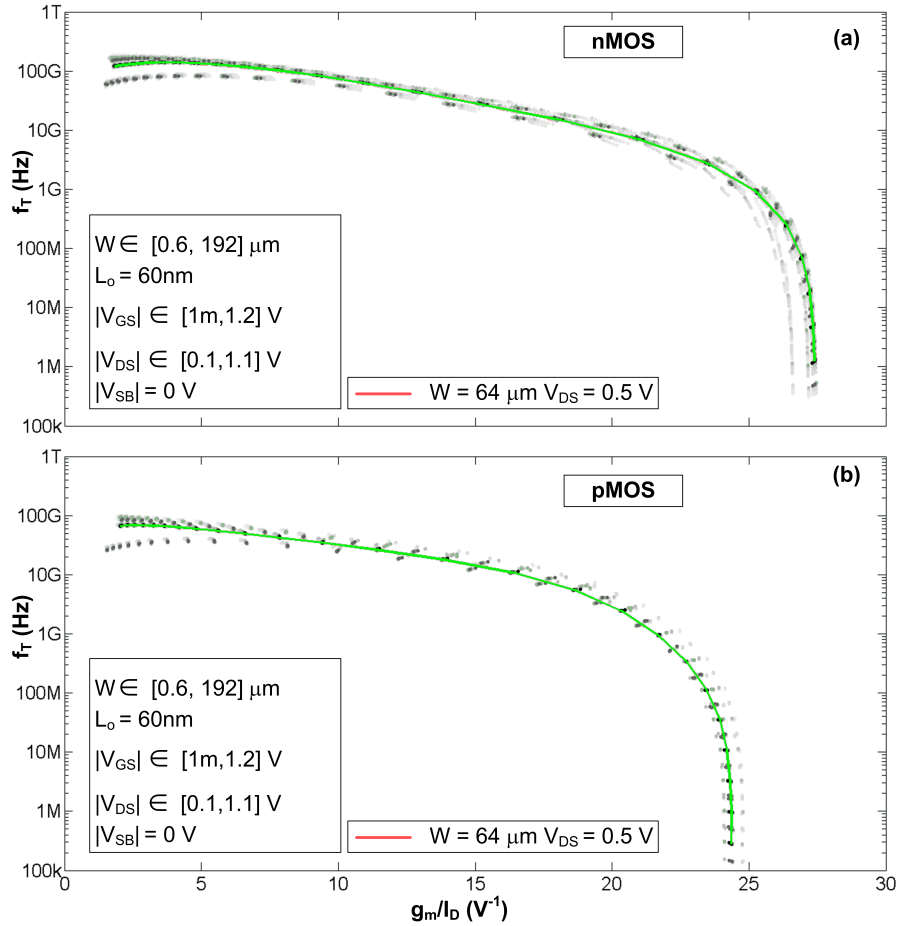

Figure 5: nMOS and pMOs transition frequency f_T versus g_m/I_D.

This figure shows that nMOS transistors biased in strong inversion achieve transition frequencies up to 200 GHz whereas pMOS transistors reach 100 GHz. In deep weak inversion those frequencies are reduced to levels below the gigahertz. Considering the very restrictive quasistatic limit in the working frequency f_0 of one tenth of f_T [**?**], for an nMOS transistor with a g_m/I_D equal to 5 V^{-1}, f_0 can be up to 20 GHz, whereas for a g_m/I_D of 25 V^{-1} f_0 should be around the 100 MHz. This simple check lets the designer know the limitations of the technology and of the used model in terms of frequency for each inversion level.

2.2. Bias Gate-Source Voltage (V_{GS}) versus g_m/I_D

From (**??**) and (**??**) it is derived that V_{GS} is function of g_m/I_D, as depicted in Fig. **??**. It means that the designer has a way of directly estimate the value of V_{GS} when the g_m/I_D ratio is fixed.

3. Other conductances and transconductances

3.1. Output conductance (g_{ds}) to I_D ratio (g_{ds}/I_D)

Another fundamental small-signal parameter required to describe the MOST behavior is the output conductance g_{ds}. It dramatically increases in nanometer transistors with respect to micrometer MOSTs due to the shortening of the channel length, as it is, in a first approximation, inversely proportional to the transistor length L [**?**]. Its increment should be considered because it would strongly distort the behavior of RF circuits. For example, in an LC tank-VCO, the MOST conductance g_{ds} affects the value of the final MOST transconductance chosen, and hence the bias current and the phase noise [**?**]; in an LNA a high g_{ds} value drastically reduces the maximum gain achieved by the amplifier [**?**].

For the 65-nm technology and $L = L_o$, the g_{ds}/I_D ratio is extracted as function of g_m/I_D for nMOS and pMOS transistors, as displayed in Fig. **??**. Behavior of these curves is practically linear in all g_m/I_D range when V_{DS} is relatively high ($V_{DS} \geq 0.5V$) and the values are comparatively small, moving from around $0.5V^{-1}$ to $2V^{-1}$, for all the range of W. Nevertheless a shift in the curves is observed when V_{DS} becomes small. A rapid growth is seen as we move simultaneously to low values of V_{DS} and to states of strong inversion. Linear behavior disappears because MOST enters in ohmic region. In fact, this information can be used to estimate the practical border from the MOST is clearly saturated. For example, for an NMOS with a fixed $V_{DS} \approx 0.2V$, the g_{ds}/I_D linear behavior correspond to an inversion range of $g_m/I_D > 10V^{-1}$; then, and according to the Fig. **??** the bias V_{GS} to ensure the saturation of NMOS

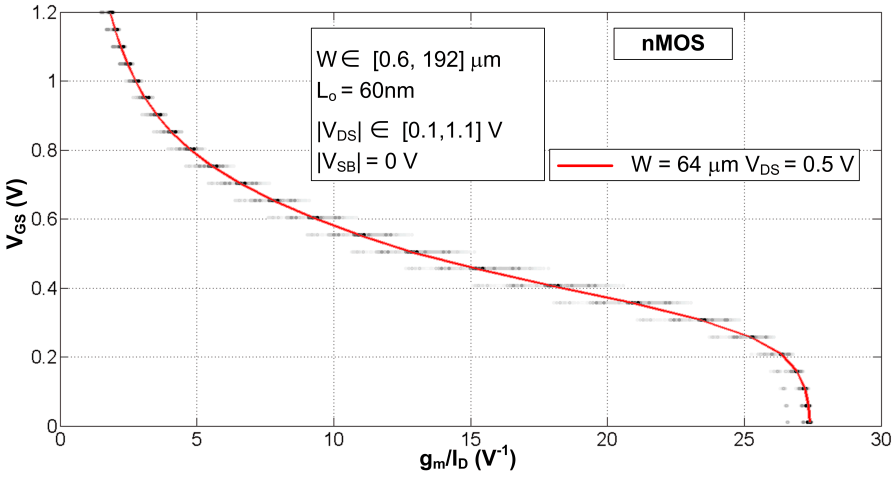

Figure 6: V_{GS} versus g_m/I_D for nMOS.

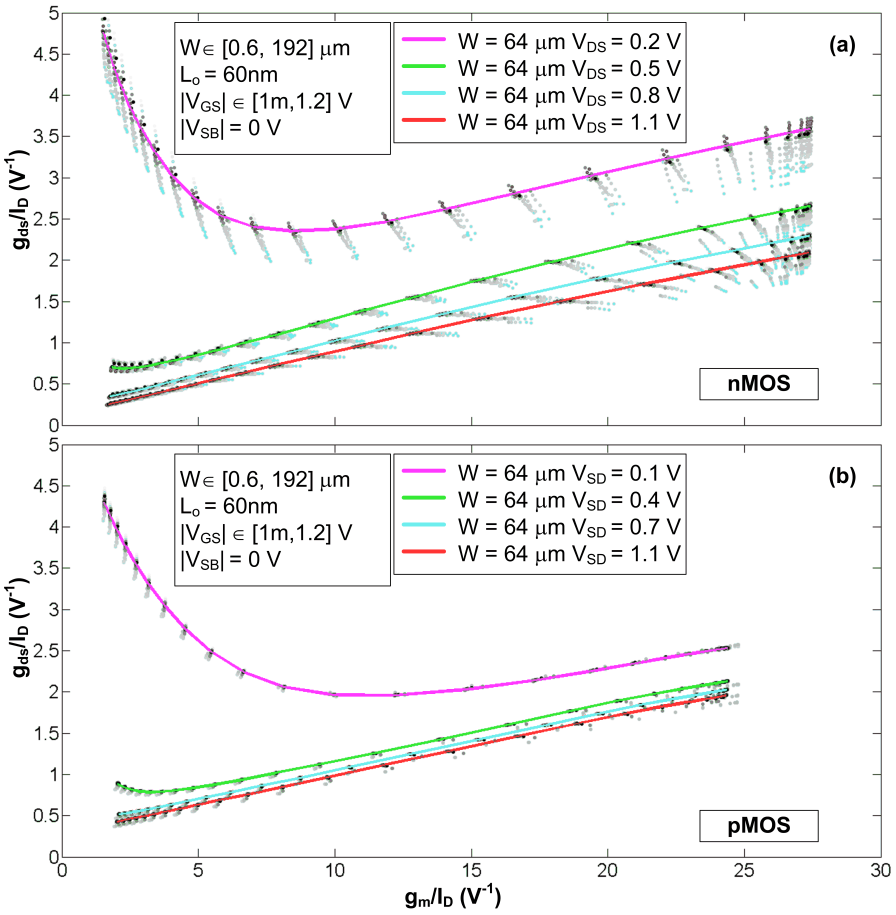

Figure 7: (a) nMOS and (b) pMOS curves of g_{ds}/I_D versus g_m/I_D.

should be $V_{GS} < 0.5V$. However, when the same transistor has a $V_{DS} > 0.5V$, bias range for saturated operation has to be $g_m/I_D > 3$ and $V_{GS} < 0.8V$.

The observed increase of g_{ds}/I_D ratio at a fixed V_{DS} when moving towards weak inversion, happens because $g_{ds}/I_D \cong 1/V_A$, where V_A is the Early voltage in first-order channel length modulation formula, and, as Tsividis stands, $V_{AW} < V_{AS}$, with V_{AW} and V_{AS} the Early voltage for weak and strong inversion regions, respectively [**?**].

To correctly use the LUTs of g_{ds}/I_D, the designer should have a rough idea of the range of values of V_{DS} of each of the MOST in the circuit. It is enough to know if the MOST would work in the ohmic or in the saturated region. For the latter, it is enough to considered the LUT associated to the medium value V_{DS} of

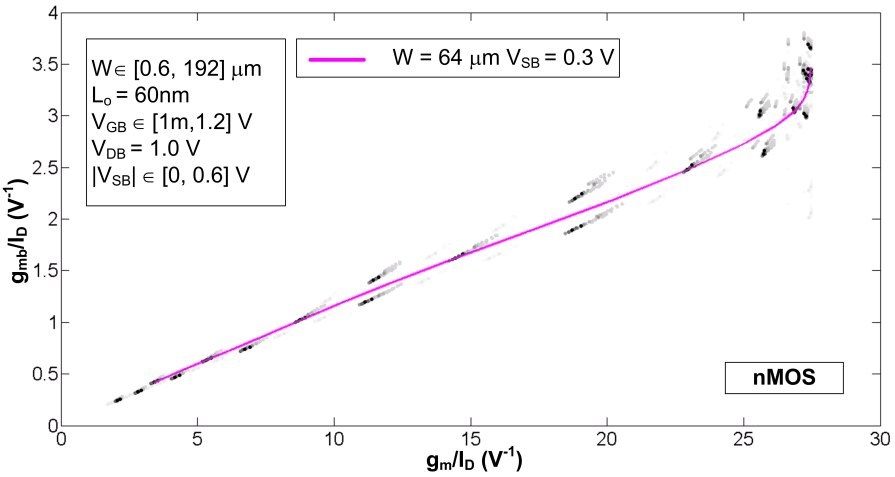

Figure 8: nMOS transistor g_{mb}/I_D ratio versus g_m/I_D.

the saturated range, i.e. $V_{DS} = 0.5V$. As seen in Fig. **??**, the maximum error made in g_{ds}/I_D would be below 25%, which is an acceptable value for this MOST characteristic.

3.2. Bulk transconductance (g_{mb}) to I_D ratio (g_{mb}/I_D)

If bulk and source terminals are not short-circuited, the transconductance g_{mb} should be considered, despite its value is generally smaller than g_m; otherwise, its effect is discarded. In this work it is studied the ratio g_{mb}/I_D against g_m/I_D. As g_{mb} is also proportional to the aspect ratio of the transistor [**?**], when it is divided by I_D, the g_{mb}/I_D should be a weak function of W. This fact is clearly appreciated in Fig. **??**, with $V_{SB} = \{0.0, 0.3, 0.6\}$ V. Also, little variation of g_{mb}/I_D with V_{SB} is observed.

4. MOST normalized intrinsic capacitances

Considering again that the working frequencies of the RF circuit into design are below one tenth of f_T, it is enough to consider in an RF design the well-known five intrinsic capacitances C_{xx} where xx=$\{gs, gd, gb, bs, bd\}$, disregarding the other capacitances and transcapacitances as well as non-quasistatic effects. These capacitances change with the inversion level, as Tsividis states [**?**]; and obviously they change with the transistor size. The intrinsic capacitances C_{xx} can be expressed as

$$\begin{aligned} C_{xx} &= C_{ox} f_{Cxx}(i; W, L) \overset{L=L_o}{=} W L_o C'_{ox} f_{Cxx}(i; W, L_o) \\ &= W L_o C'_{ox} f^*_{Cxx}(g_m/I_D; W, L_o). \end{aligned} \tag{5}$$

where the normalized thin-oxide capacitance C'_{ox} is equal to ϵ_{ox}/t_{ox}, being ϵ_{ox} the absolute oxide permittivity and t_{ox} the MOST thin oxide thickness. These capacitances are proportional to the gate area (WL_o) and for each C_{xx}, they are functions of the inversion level, i.e. of the g_m/I_D, and to a minor extend, of W and L_o. Thus, for the semi-empirical model here proposed, the normalized capacitances are

$$c_{xx} = \frac{C_{xx}}{WL_o} \tag{6}$$

This approach is valid if c_{xx} has a minor spread when W and V_{DS} vary.

Figure **??** presents the plots of the resulting five normalized capacitances of nMOS and pMOS transistor for the whole range of g_m/I_D, varying either V_{DS} and W. The curves have the expected form respect to the inversion region. The spread with V_{DS} and W is, in all cases, below 10%, hence for 65-nm MOST, the idea of using normalized capacitances in a design flow is a very good option [**?**].

5. Noise parameters

When modeling white and flicker noise (the MOST most noticeable noise sources), semi-analytical models are utilized, as the equations that model these effects are both very simple and wide known [**?**]. The noise current power spectral density (psd) of these two phenomenons together with the induced gate noise, referred at the drain of the MOS as $\overline{i_d^2}(f)$, are sketched in Fig. **??**. In it, three regions are recognized: the flicker noise zone, the white noise zone and the induced-gate noise zone. The frequency of the asymptotic limit between the flicker noise and the white noise zones, called corner frequency f_c is also shown. In this work, the induced gate noise is not studied, but a similar approach to the one followed with the other noise sources can be pursued to find it.

The white noise psd $\overline{i_{w,d}^2}$ is, for all inversion regions, expressed as [**?**]

$$\overline{i_{w,d}^2} = 4k_B T \frac{\gamma}{\alpha} g_m \tag{7}$$

where k_B is the Boltzmann constant and T is the absolute temperature. The white noise factor γ/α is extracted here as function of g_m/I_D, neglecting the effects of W and V_{DS}.

Concerning the flicker noise psd $\overline{i_{1/f,d}^2}$, it is written as

$$\overline{i_{1/f,d}^2} = \frac{K_F g_m^2}{C'_{ox} W L_o} \frac{1}{f^\eta} \tag{8}$$

where f is the frequency of study. The K_F is the flicker noise parameter and η is the flicker noise frequency exponent. The

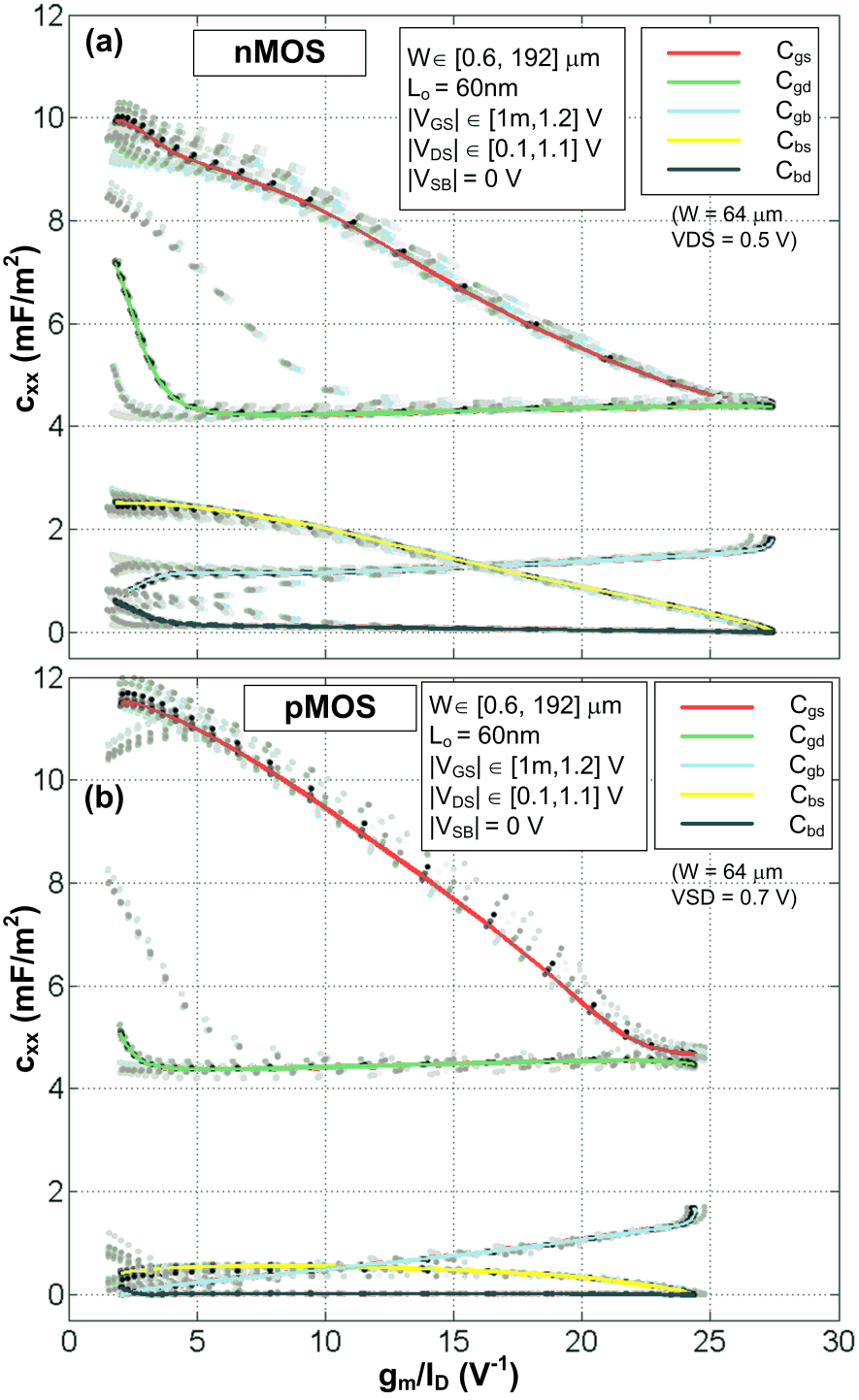

Figure 9: (a)nMOS and (b) pMOS curves of of c_{xx} versus g_m/I_D.

psd of the drain-noise current is $\overline{i_d^2} = \overline{i_{w,d}^2} + \overline{i_{1/f,d}^2}$ as no correlation is supposed to exist between the white noise and the flicker noise sources.

Equations (**??**) and (**??**) are taken as the noise semi-analytical models whose parameters γ/α and K_F are here described as function of g_m/I_D. The η parameter is derived by finding the flicker psd for a MOST with fixed W and bias conditions for two different frequencies f_1 and f_2, and solving for η, i.e.:

$$\eta = \frac{log\left(\frac{\overline{i_{1/f,d}^2}(f_1)}{\overline{i_{1/f,d}^2}(f_2)}\right)}{log(f_2/f_1)} \tag{9}$$

being $\eta_{nMOS} \cong 0.95$ and $\eta_{pMOS} \cong 1.1$.

For the defined set of MOST W and V_{DS}, the behavior of γ/α and K_F are depicted in Fig. **??**. Studying the evolution of γ/α,

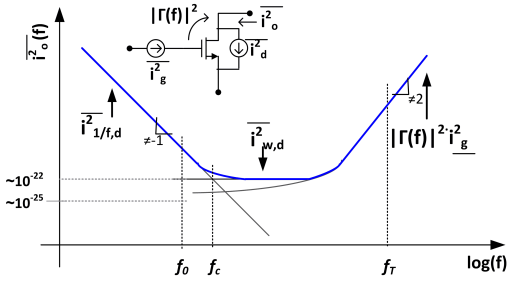

Figure 10: Sketch of MOST psd versus frequency, where $|\Gamma(f)|^2$ is the induced gate noise transfer function at the output.

it is observed that for moderate and weak inversion its value is constrained between 1.0 and 1.5; however for strong inversion this parameter could reach values up to 3.5. For K_F, in strong inversion the spread with W and V_{DS} is relatively high, whereas in weak inversion this parameter is almost independent of sizing and V_{DS}. So if a high level of accuracy is required in the flicker model, a set of W and V_{DS} should be considered; otherwise a mean value of K_F versus g_m/I_D can be used. In addition, the use of the exponent η reduces the error of K_f to less than 0.5%, at least for frequencies up to 10 MHz.

The corner frequency of a MOST f_c is obtained by making equal the psd expressions of white noise and flicker noise, (**??**) and (**??**), resulting in

$$f_c = \left(\frac{K_F}{4k_B T C'_{ox}} \frac{1}{\gamma/\alpha} \frac{g_m}{I_D} \frac{I_D}{WL_o} \right)^{1/\eta}$$

namely, it is a function of the MOST g_m/I_D and of i. From the logarithmic relation between i and g_m/I_D, it is demonstrated that the corner frequency drastically drops down at moderate-weak inversion, as seen in Fig. **??**.

6. CS-LNA design and validation

To present a strong justification of the utility and validity of the MOST model developed over a real analog RF circuit design, in this paper it is chosen the RF narrowband low-power common-source low noise amplifiers (CS-LNA), as the one sketched in Fig. **??**. The core of the CS-LNA comprises two active elements: the MOST amplifier M_1 and the MOST cascode M_2. Its passive elements are the gate inductor L_g, the external capacitor C_{ext} between MOST gate and source terminals, the source inductor L_s, the drain inductor L_d and the drain series and parallel capacitors C_{d1} and C_{d2}. The input source voltage has a series impedance of 50Ω impedance. The same applies for the output load, i.e.: $Z_L = R_L = 50\Omega$; the value of the choke resistance $R_{bias} = 10$ kΩ to reduce its effect in the total noise figure as well as to make it feasible on-chip.

As in these designs all LNA elements are on-chip, special attention must be paid to the inductors and its parasitics. As the resistive parasitics of the three inductors affect considerably the performance of the LNA, its inclusion in the design procedure is compulsory. The 65-nm technology here used has a database of on-chip inductors and is the utilized in the design procedure, otherwise methods as the one presented in [**?**] should be followed. A simplified model of the inductors is extracted: for each f_0 and each possible inductor provided by the technology, its equivalent impedance $Z_{ind}(f_0)$ is found; later the corresponding equivalent series resistance and impedance are found, i.e.: $Z_{ind}(f_0) = R_{s,ind} + j\omega_0 L_{ind}$, where $\omega_0 = 2\pi f_0$. Finally, a LUT Λ_L of the best inductors for the desired working frequency -in the sense of the best quality factor- is obtained, as depicted in Fig. **??**, and included in the Matlab design flow [**?**]. The quality factors of the MiM capacitors used here is so high for all f_0 that there are considered ideals. Otherwise, the same approach as the one followed in the inductors model can be followed.

6.1. Incorporation of the MOST model usage in the LNA design

The steps followed to design the CS-LNA, as studied in [**?**], are revisited here to specifically highlight the usage of the proposed MOST model. The LNA design synthesis uses the impedance matching approach either at the input and output of the LNA load, for the working f_0; MOST are considered as identical, having both the same g_m/I_D and I_D.

So, lets suppose that we choose a specific pair (g_m/I_D,I_D). The following data can easily be derived from the MOST:

- from data of Fig. **??**, given g_m/I_D, the value of i is determined. With this value and I_D, the MOST W is obtained. Also g_m is derived in this step.
- with data of Fig. **??**, MOST f_T is picked
- As transistors M_1 and M_2 are identical as well as its drain current, a first hypothesis is that $V_{D,M1} \cong V_{DD}/2$, so conductances g_{ds}, and g_{mb} are straight from Figs. **??** and **??** and applying the methodology presented at the end of Sect. **??**.
- all normalized MOST intrinsic capacitances are derived from Fig. **??**, and noise parameters K_F and γ/α come from Fig. **??** for the corresponding g_m/I_D.

Hence, with the whole set of MOST data, it is possible to compute the most important characteristics of the LNA, as gain G, noise figure NF or input third order intermodulation product $IIP3$. In the optimization process particularly presented in [**?**], its best LNA passive components are chosen to improve the input / output matching, and to minimize the NF while achieving maximum LNA gain G. The MOST characteristics listed above can be easily incorporated in the LNA expressions of NF and G, for example via a set of Matlab routines.

6.2. LNA designs

Firstly, six designs are computed for two RF frequencies $f_0 = \{2.5, 5.3\}$ GHz and three inversion regions, $g_m/I_D = \{6, 13, 20\}V^{-1}$. For each g_m/I_D value the MOS transistors drain current I_D is equal to 1.0 mA. For each g_m/I_D, the final design chosen is the one that obtains the lowest noise figure NF for each g_m/I_D and f_0 considered. The designs are computed with Matlab routines and simulated with SpectreRF simulator from Cadence.

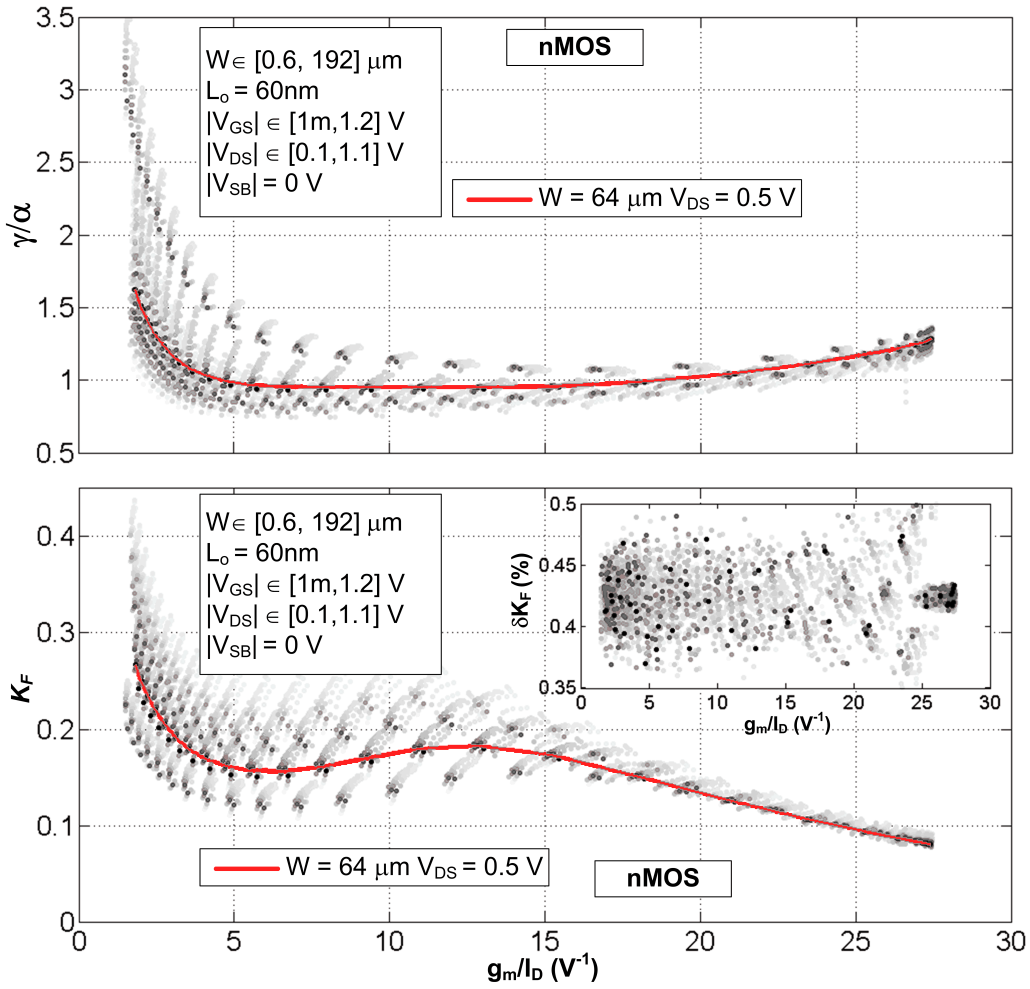

Figure 11: nMOS (a)γ/α and (b) K_F at 10Hz versus g_m/I_D; with K_F relative error in frequency up to 10MHz (inset).

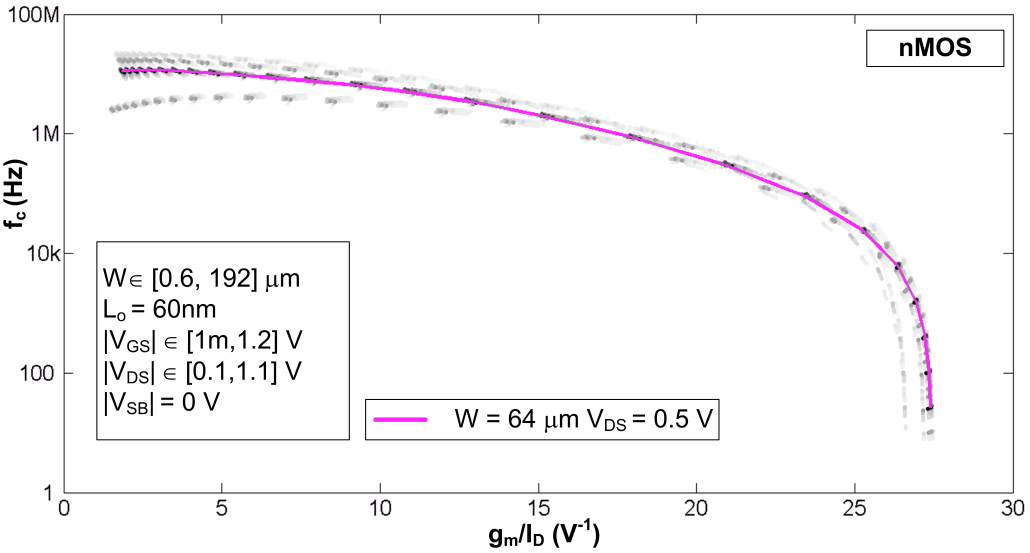

Figure 12: MOST corner frequency f_c.

Table 1: CS-LNA designs based on the MOST semi-empirical model here presented. Matlab computed and SpectreRF simulated data are provided for comparison.

Design	f_0	g_m/I_D	I_D	W	C_{ext}	L_s	L_g	L_d	C_{d1}	C_{d2}	G (dB)		NF (dB)		IIP3 (dBm)	
#	GHz	(1/V)	(mA)	(μm)	(fF)	(nH)	(nH)	(nH)	(fF)	(fF)	Calc.	Sim.	Calc.	Sim.	Calc.	Sim.
1	2.5	6	1.0	8.00	266	0.96	14.0	13.8	324	935	10.5	9.6	3.4	4.0	-6.8	-9.8
2	2.5	13	1.0	57.7	223	0.51	13.6	13.7	264	292	16.6	16.2	2.7	2.8	-8.4	-10.3
3	2.5	20	1.0	474	73	1.00	6.7	6.1	338	292	12.9	12.1	2.6	2.45	-7.8	-1.5
4	5.3	6	1.0	8.00	124	0.50	6.4	7.4	119	138	10.2	9.3	3.4	3.9	-6.8	-9.7
5	5.3	13	1.0	57.7	120	0.53	4.5	5.4	129	138	13.7	13.1	2.3	2.45	-6.6	-8.0
6	5.3	20	1.0	474	88	0.91	1.4	1.8	174	137	5.92	4.5	5.4	5.0	-7.5	-6.3

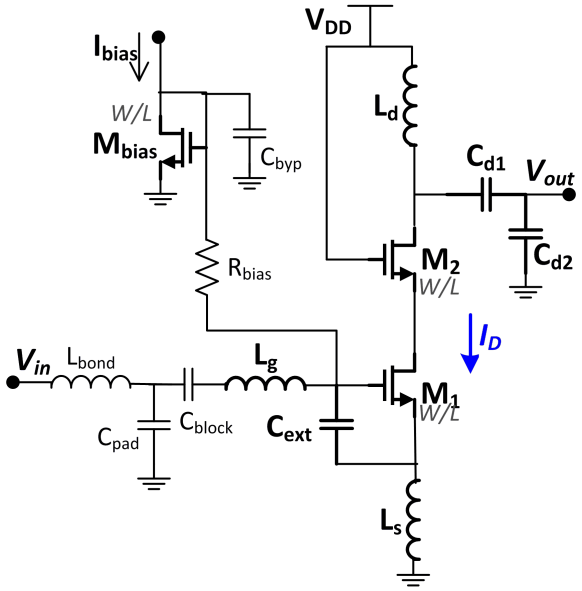

Figure 13: Schematic of cascode CS-LNA utilized in the semi-empirical model verification.

Noise figure NF, gain G and $IIP3$ of the computed and simulated results are compared. The designs are displayed in Table **??** as well as the computed and simulated gain G, noise figure NF and $IIP3$. Although the designs have been simulated without any retouch, NF errors are all below 0.6 dB and gain G errors are less than 1 dB except in design 6. For this design, a larger discrepancy is expected due to the fact that it

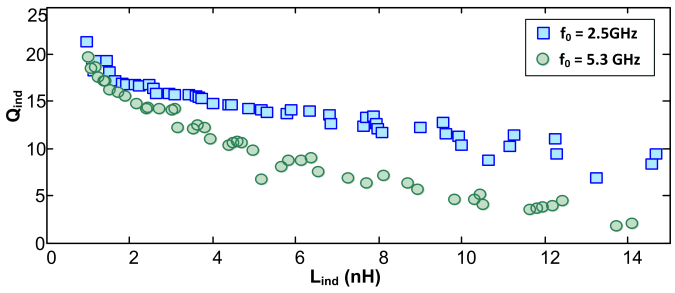

Figure 14: Best (maximal) quality factors versus the equivalent inductor value for $f_0 = \{2.5, 5.3\}$GHz.

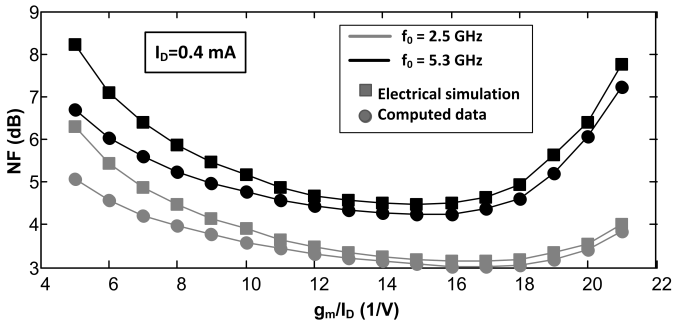

Figure 15: CS-LNA noise figure versus g_m/I_D for 2.5GHz and 5.3GHz.

is working away from the quasi-static regime. Also, a good match is achieved in $IIP3$ figures. As it is seen in Sect. **??** f_T is directly related to the g_m/I_D of the MOST. Using the data of Fig. **??** it is obtained that, for each $g_m/I_D = \{6, 13, 20\}V^{-1}$, $f_T = \{130, 45, 10.5\}$ GHz, respectively. It means that for designs 1, 2 and 4 we are under the hypothesis of working below one tenth of f_T, whereas design 5 is in the limit. But for designs 3 and 6 this ratio is less than 5 and 2, respectively, so errors due to disregarding non-quasistatic capacitances are expected.

Then, to see the behavior of the model for low drain currents, for $f_0 = \{2.5, 5.3\}$ GHz the g_m/I_D is swept in $[5, 21]V^{-1}$, in order to find the best LNA designs in the sense of the lowest NF, for a low drain current $I_D = 0.4$ mA. Figure **??** presents the final results, showing a very good agreement between computed and simulated data.

7. Conclusions

This paper presents a MOST semi-empirical model used for RF analog designs in all-inversion regions. The behavior of the fundamental MOST characteristics is described as function of the g_m/I_D ratio, as the inversion level i, the conductance and transconductance ratios g_{ds}/I_D and g_{mb}/I_D, the quasistatic normalized capacitances c_{xx} and the fundamental noise parameters. The semi-empirical modeling has been validated by designing a set of CS-LNAs for minimum noise figure and fixed low current, respectively, and comparing the computed data using the proposed semi-empirical models with electrical simulations. The reasonable agreement found between them corrobo-

rates the validity of using our semi-empirical model as convenient tool in RF analog design.

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