Design of a 1-V 90-nm CMOS adaptive LNA for multi-standard wireless receivers

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This paper presents the design of a reconfigurable Low-Noise Amplifier (LNA) for the next generation of wireless hand-held devices. The circuit, based on a lumped-approach design and implemented in a 90nm standard RF CMOS technology, consists of a two-stage topology that combines inductive-source degeneration with MOS-varactor based tuning networks and programmable bias currents, in order to adapt its performance to different standard specifications with reduced number of inductors and minimum power dissipation. As an application, the LNA is designed to cope with the requirements of GSM (PCS1900), WCDMA, Bluetooth and WLAN (IEEE 802.11b-g). Simulation results, including technology parasitics, demonstrate correct operation of the LNA for these standards, featuring NF$<$1.77dB, S_{21} $>$16dB, S_{11} $<$-5.5dB, S_{22} $<$-5.5 dB and IIP3$>$-3.3 dBm over the 1.85-2.48 GHz band, with an adaptive power consumption between 25.3 mW and 53.3mW. The layout of the LNA occupies an area of 1.18$\times$1.18 μm^2.

Keywords: Integrated circuits; field effect integrated devices; amplifiers.

En este artículo se presenta el diseño de un LNA (del Inglés *Low-Noise Amplifier*) configurable para la próxima generación de dispositivos digitales personales. El circuito, diseñado con la aproximación de circuitos concentrados e implementado en una tecnología CMOS, 90nm, de RF, consta de una topología formada por dos etapas que combina degeneración inductiva de fuente, redes de entonado basada en varactores, y circuitos de polarización programables para adaptar el desempeño a las diferentes especificaciones del estándar con reducido número de inductores y mínima disipación de potencia. Como aplicación, el LNA que se diseña satisface los requerimientos de GSM (PCS1900), WCDMA, Bluetooth y WLAN (IEEE 802.11b-g). Los resultados de simulación, incluyendo el efecto de los elementos parásitos, demuestran una correcta operación del para LNA los estándares mencionados, obteniendo NF$<$1.77 dB, S_21 $>$16dB, S_11 $<$-5.5dB, $S_2 2$ $<$-5.5 dB y IIP3$>$-3.3 dBm en la banda 1.85-2.48 GHz band, con un consumo de potencia entre 25.3mW y 53.3mW. El patrón geométrico del LNA ocupa un área de 1.18$\times$1.18 μm^2.

Descriptores: Circuitos integrados; dispositivos integrados con efecto de campo; amplificadores.

PACS: 85.40.-e; 85.30.Tv; 84.30.Le

1. Introduction

The fourth generation (4G) of wireless telecom systems will require low-power multi-standard chipsets, capable of operating over a number of different communication protocols, signal conditions, battery statuses, etc [1]. The efficient implementation of these chipsets calls for reconfigurable building blocks that can adapt to the different specifications with minimal power consumption and at a low cost [2]. Currently, one of the most challenging circuits is the LNA. The design of this circuit is especially critical due to its position at the receiver front-end, having to simultaneously match the antenna and to amplify weak input signals with minimal noise contribution, high linearity and isolation from the rest of the receiver chain [3]. This problem is aggravated in the case of multi-standard applications, in which LNAs must operate over different frequency ranges, while maintaining a reduced number of passives, *i.e.* capacitors and inductors to increase the integration [1-3].

In order to solve the above-mentioned problems, a number of circuits have been reported in the last few years to implement multi-standard CMOS LNAs [4-14]. Some of them are based on the use of switchable matching networks to select the resonant frequency, thus preserving immunity to out-of-band interferers, although only one signal band is received at any one time [5-8]. Besides, the use of switches forces a discrete frequency selection and introduces parasitic switch-on resistances that need to be reduced at the price of increasing the circuit noise. These limitations can be partially solved by using concurrent multi-band LNAs, which allow a simultaneous reception of multiple signal bands without using switches [4,13]. However, the spurs in one band may corrupt signals in another band due to the LNA non-linear operation [3].

A common issue in most reported multi-standard LNAs is the need for additional passive components for the input and output matching networks. This fact has motivated the exploration of other techniques, such as the use of wideband resistive-feedback topologies [11] that can achieve good performance in a wide signal bandwidth without using inductors [14], at the cost of increasing the circuit noise.

In order to offer an alternative multi-standard LNA that solves the above-described noise problems, the LNA presented in this paper adapts its performance to the require-

ments of four standards (GSM, WCDMA, Bluetooth and WLAN) without increasing the number of inductors as compared to the mono-standard case. The proposed circuit employs a two-stage topology to separately control the input impedance and the signal gain. A MOS-varactor tuning network is used in both stages in order to make the resonance frequency programmable without penalizing the LNA noise performance. SpectreRF simulations considering technology parasitic are shown to verify the operation of the LNA.

2. LNA Topology and analysis

Figure 1 shows the complete diagram of the proposed reconfigurable LNA. It consists of a two-stage topology with separate biasing circuits and tuning networks. Note that the input stage includes an LRC network needed to match the input impedance; the same is true for the output stage, where an LC network is included. The input stage uses an inductively degenerated common-source structure to provide a specified real part for the input impedance and signal gain at a given frequency, whereas the output stage provides higher gain without significantly degrading the noise performance.

Assuming that a saturated MOS transistor is modeled by a Voltage-Controlled Current-Source (VCCS), and considering that inductors L_g and L_s are ideal, it is easy to show that the input impedance of the LNA is given by

$$Z_{in}(s) = \frac{1}{sC_1} + \frac{s(L_g+L_s) + \frac{1}{sC_{gs}} + g_{mn1}\frac{L_s}{C_{gs}}}{1 + \frac{1}{R_{b1}\|R_{b2}}\left[s(L_g+L_s) + \frac{1}{sC_{gs}} + g_{mn1}\frac{L_s}{C_{gs}}\right]} \quad (1)$$

where $g_{mn1}$and C_{gsn1} are the small-signal transconductance and gate-source capacitance of M_{n1}. The magnitude of Z_{in}(**s**) is obtained if **s** is replaced by jω, where [ω]=rad/s. Since at the resonant frequency the input impedance must be purely ohmic, this parameter is chosen to be equal to the RF source resistance, R_s. Furthermore, if the equivalent resistance, R_{eq}=$R_{b1}||R_{b2}$, is chosen in such a way that the condition $R_{b1}||R_{b2} \gg 50\Omega$ is satisfied, (1) can be simplified as follows:

$$Z_{in}(s) \approx \frac{L_g+L_s}{s}\left[s^2 + \frac{1}{(L_s+L_g)(C_1+C_{gsn1})}\right] + \frac{g_{mn1}L_s}{C_{gsn1}} \quad (2)$$

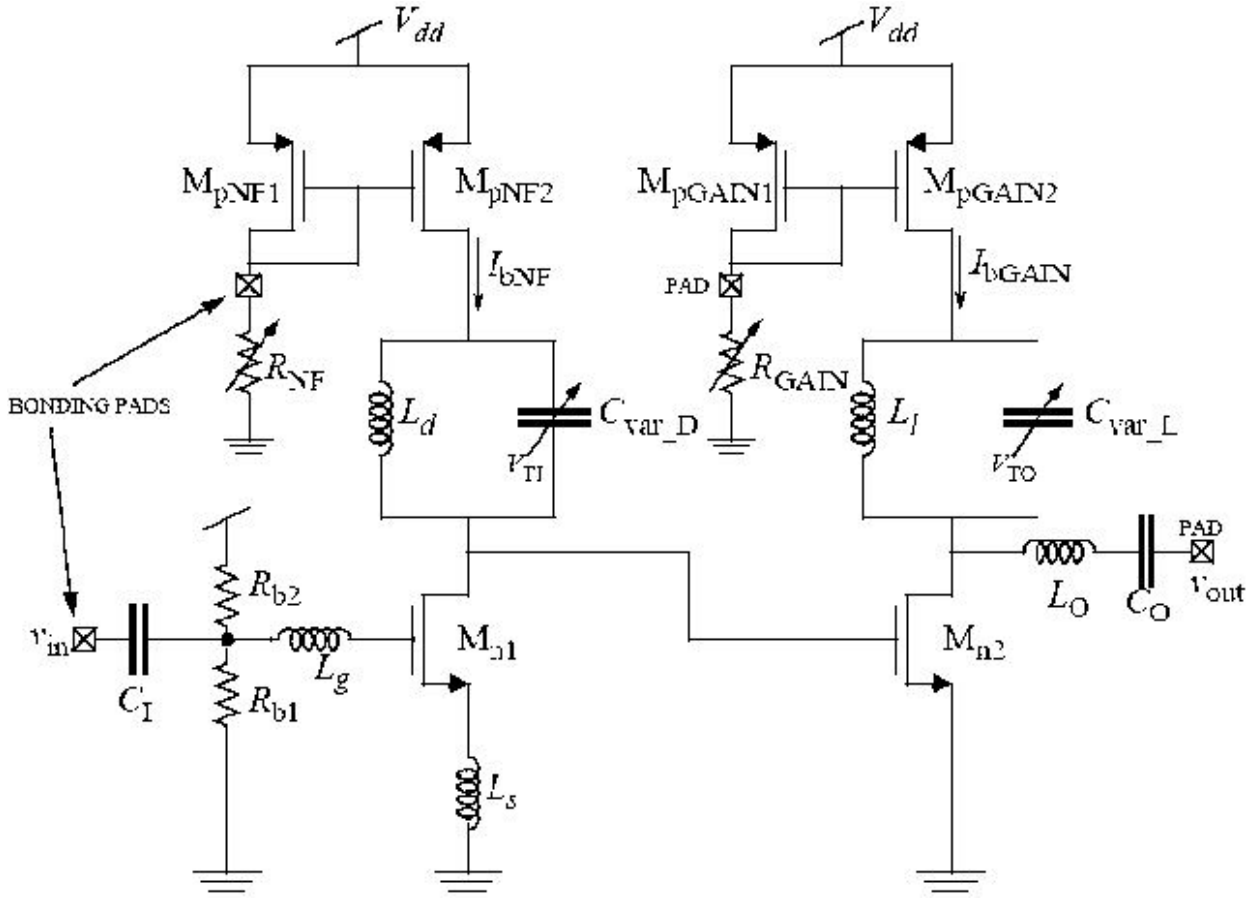

FIGURE 1. Diagram of the tunable LNA.

TABLE I. LNA Specifications

Standard	BW(GHz)	NF(dB)	$S_{21}(dB)$	IIP3 (dBm)
GSM	1.85-1.99	1.7	11.5	-2
WCDMA	1.92-2.17	3.7	18	-0.5
Bluetooth	2.4-2.4835	28	12.5	-12
WLAN	2.4-2.4835	4.5	19.6	-5.4

TABLE II. LNA Sizing and Biasing.

Transistors	W/L (μm/μm)	Capacitors (pF)	Inductors (nH)	Bias Currents (mA)
m_{n1}	180/0.1	$C_{I,O}$=7.7	L_d=1.6	I_{bNF}= (24.7-32.4)
m_{n2}	180/0.2	C_{var_D}=(2.7,4.3)	L_g=12.2	I_{bGAIN}= (0.9-20.4)
m_{pNF1}	1/0.1	C_{var_L}=(0.7,1.1)	L_s=0.1	
m_{pNF2}	300/0.1	Resistors (kΩ)	L_l=6.4	
m_{pGAIN1}	1/0.1	R_{b1}= 6	L_o=16.9	
m_{pGAIN2}	300/0.1	R_{b2}= 4		

TABLE III. Parameter Configuration for the Different Standards.

Standard	R_{NF} (kΩ)	R_{GAIN} (kΩ)	I_{bNF} (mA)	I_{bGAIN} (mA)	C_{var_D} (pF)	C_{var_L} (pF)
GSM	0.5	2.5	32.4	20.4	4.3	1.1
WCDMA	3.4	0.5	25.8	2.4	3.9	1
Bluetooth	4.1	0.5	24.7	0.9	2.7	0.7
WLAN	3.1	0.5	26.6	3.6	2.7	0.7

This result shows that the real part of Z_{in}(**s**) corresponds to $g_{mn1}L_s/C_{gsn1}$. In this work, as the LNA is fully integrated as a stand-alone circuit, a termination of 50Ω is needed not only at the input, v_{in}, but also at the output, v_{out}, terminals within the 1.85-2.48 GHz band. The latest is the bandwidth defined for the correct operation of the four above-mentioned standards. On the other hand, the tuning mechanism of the LNA is achieved by varying the resonance frequencies of the passive input/output tuning network. The resonant frequency, ω_r, is easily calculated by analyzing the equivalent impedance of the parallel connection of an LC network:

$$Z_{eq}(s) = sL \| \frac{1}{sC} = \frac{sL}{s^2LC+1} = \frac{s}{C}\left(s^2 + \frac{1}{LC}\right)^{-1} \quad (3)$$

From this result, it is easy to demonstrate that the input/output resonance frequency is given by (4), where $[L_{d,l}C_{var\_D,L}]=s^2$, and C_{var_D} and C_{var_L} are accumulation-MOS varactors provided by the 90-nm standard RF CMOS process used for the circuit implementation.

$$\omega_r = \frac{1}{\sqrt{L_d C_{var\_D}}} = \frac{1}{\sqrt{L_l C_{var\_L}}} \quad (4)$$

The capacitance of these varactors, controlled by voltages V_{TI} and V_{TO}, could be varied from 20fF to 10pF in accumulation mode, providing a resonance frequency of up to 20 GHz. Note that, as each varactor is connected at the transistor drains of both stages, its noise contribution is attenuated by the gain of M_{n1} and M_{n2}. Since the gain of these transistors depends on the transconductance value, different bias current mirrors are used for biasing both stages in order to control separately the gain of M_{n1} and M_{n2}. In this way, the Noise Figure (NF) and the voltage gain of the LNA are individually controlled by using bias currents I_{bNF} and I_{bGAIN}, respectively. The goal of the proposed LNA is twofold:

1) since these currents are adapted to achieve the required specifications for each standard, the operation of the LNA is done with the minimum power dissipation and,

2) using varactors instead switches reduces NF.

In this proposal, bias currents are generated by external off-chip variable resistors, R_{NF} and R_{GAIN} (see Fig. 1), in order to prove the concept. However, in a practical application, bias currents can be generated on-chip and controlled by the digital signal processor according to the required performance of the whole receiver. In addition to the bias currents, the gate of M_{n1} is biased by using a voltage divider made up of resistors R_{b1} and R_{b2}. These resistors, implemented by using non-silicide polysilicon, are sized to provide the required operating point without degrading NF.

A. Basics review

The analysis of the CMOS circuit shown in Fig. 1 has been used to obtain basic design models based on the so-called lumped approximation. Using the lumped approach it is assumed that each electronic component represents just a physical characteristic, which does not depend on external/internal effects. Hence, the LNA analysis was carried out with the help of both Kirchhoff's laws and the Ohm's law. The latter is expressed in the Laplace domain by v(s)=Z_e(s)i(s), where Z_e(s) is the equivalent impedance for each electronic component, which corresponds to R, **s**L, and (**s**C)$^{-1}$ for resistors, inductors, and capacitors, respectively.

In conjunction with the lumped approach, the MOS transistor has been modeled as a simple VCCS in order to fulfill both the design specifications and multi-standard requirements. Note that the simplicity of the analysis does not represent a weak proposal, but a practical one supported by physical laws suitable for developing a transistor-level design procedure. However, for obtaining the electrical performance of design variables over the 1.85-2.48 GHz band, a simulation process is needed to evaluate the effect of parasitics on the LNA's performance as well as to re-fine (if needed) the sizing of active/passive components. These characteristics obtained from simulation runs cannot be deduced via hand-work due to the complexity of both the whole LRC-g_{mn} equivalent circuit and the resulting high order s-matrix.

3. Circuit design

The reconfigurable LNA is designed to fulfill the requirements of a multi-standard wireless direct-conversion receiver for the following standards: GSM (PCS1900), WCDMA, Bluetooth and WLAN (IEEE 802.11b-g). These requirements, summarized in Table I, were extracted from a number of previously reported integrated receivers [2,3,9,15,16]. In addition to NF, Table 1 shows the specifications for the signal Band-Width (BW), the LNA gain (S_{21}) and the third-order intermodulation intercept point, IIP3. In order to cope with the different sets of specifications shown in Table I, the following design procedure has been followed:

- Passive elements of the input matching network (C_I, L_g, L_s) are derived from (2) in order to get the required input impedance, *i.e.* $|Z_{in}|$=50Ω.

- Transistors M_{n1} and $M_{pNF1,2}$, and R_{NF} are sized in order to achieve the minimum value required for NF in the signal bandwidth, while trying to achieve the maximum voltage gain possible with the least power dissipation through proper adjustment of R_{NF}. At this design step, the values of R_{b1} and R_{b2} are set to provide the operating point required at the gate of M_{n1}, considering both linearity and noise requirements. By neglecting the effect of bias resistors and technology parasitics of passive elements, the NF of the LNA shown in Fig. 1 is approximately the same as that of the well-known inductively-degenerated common-source LNA [3].

- Transistors M_{n2}, $M_{pGAIN1,2}$ and R_{GAIN} are sized in order to get the maximum voltage gain.

- L_O and C_O are calculated to get an output impedance matched to 50Ω.

- L_d, L_l, C_{var_D} and C_{var_L} are computed from (4) to get the required LNA tuning frequencies for each standard in Table 1.

- Technology parasitics are considered in an interactive electrical simulation process to re-fine the sizing and biasing obtained in the previous steps.

The outcome of the design procedure described above is the sizing and biasing of the LNA, summarized in Table II. The performance of the circuit is adapted to the different standard specifications by varying the values of R_{NF} and R_{GAIN}. These values together with the corresponding bias currents and varactors capacitances are shown in Table III.

4. Simulation results

The LNA in Fig. 1 has been powered with a single 1-V supply voltage. In order to consider parasitics of passive components, the LNA's performance has been extensively verified with the help of CADENCE SpectreRF. Fig. 2 represents the NF-frequency characteristic for all the standards under study. The overall minimum value of NF is 1.6dB, obtained at 1.85 GHz, which corresponds to the lowest limit of the GSM band. Figures 3 and 4 show, on the other hand, the forward-gain (S_{21}) and the input reflection coefficient (S_{11}), respectively. The minimum value of S_{21} within the band of interest is above 16dB, corresponding to Bluetooth, whereas S_{11} and S_{22} are below -5dB for all standards.

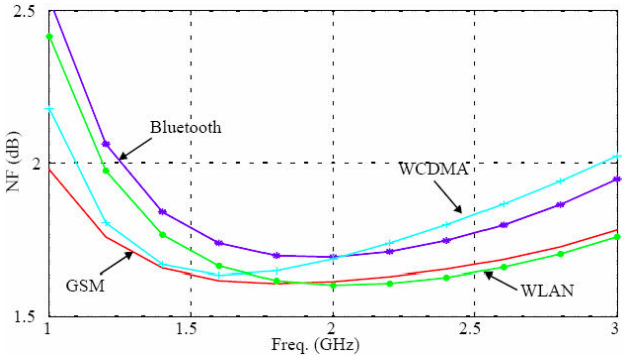

FIGURE 2. NF vs. input frequency for the different standards.

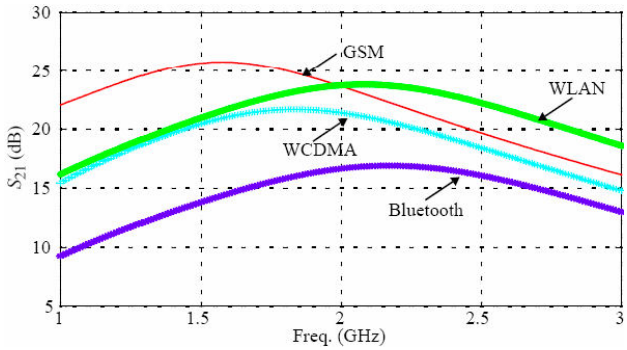

FIGURE 3. S_{21} vs. input frequency for the different standards.

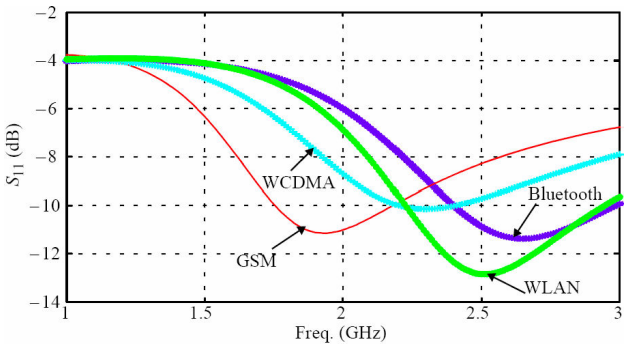

FIGURE 4. S_{11} vs. input frequency for the different standards.

The linearity of the LNA has been also taken into account in the design procedure. As shown in Fig. 5, the minimum and maximum values achieved are -3.3 dBm and 0.7 dBm for WLAN and GSM, respectively. Finally, Table IV sums up the simulated performance of the LNA by showing the worst-case values of the different figures for each standard. This performance is compared in Table V with previous reported multi-standard CMOS LNAs, by using the following Figures Of Merit (FOM) [17]:

$$FOM_1 = \frac{\text{Gain}}{(NF-1)\text{Power}} \tag{5}$$

$$FOM_2 = \frac{\text{Gain} \cdot \text{IIP3} \cdot f_c}{(NF-1)\text{Power}} \tag{6}$$

where f_c is the operating frequency of the LNA, [Power]=mW, [IIP3]=mW, [f_c]=GHz, and Gain and NF are dimensionless parameters. Note that the proposed circuit compares favorably to previous LNAs while covering a large number of standards. However, although the power consumption (especially in the GSM case) is higher than in some other designs, it should be noticed that this is a direct consequence of the reduced value of the NF reported. Indeed, depending on the receiver specifications, signal conditions and/or battery status of the receiver, etc., the proposed circuit can adapt its power consumption by reconfiguring its bias currents. This is illustrated in Fig. 6, where the NF-I_{bNF} characteristic is presented. Note that NF can be varied from around 1.55 to 4 by reducing I_{bNF} from ∼27mA to 17mA at the cost of reducing S_{21} by ∼6 dB. On the other hand, NF can be kept constant (around ∼1.6 dB) by increasing I_{bNF} if a higher gain value is needed.

5. Conclusions

The lumped-approach based design and electrical implementation of a multi-standard LNA in a 90-nm CMOS technology has been presented. Simulation results (CADENCE Spectre RF) demonstrate that the use of reconfigurable bias currents

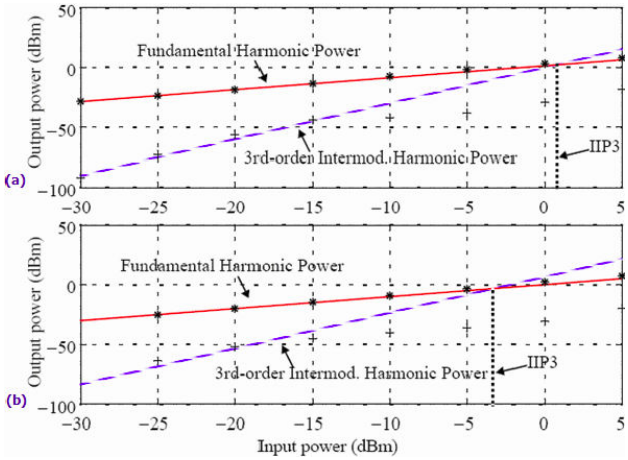

FIGURE 5. IIP3 for (a) GSM and (b) WLAN.

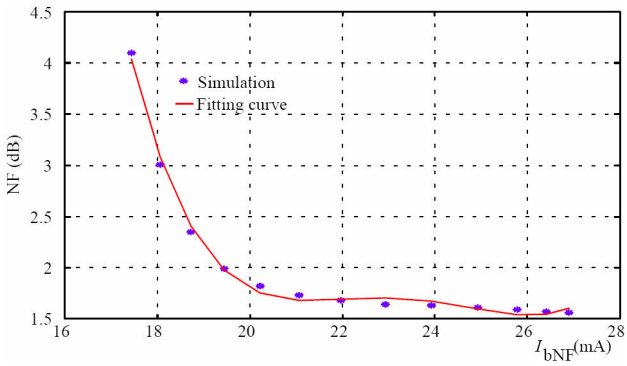

FIGURE 6. NF vs. I_{bNF}.

TABLE IV. Simulated Performance Summary of the LNA.

Standard (Band,GHZ)	NF (dB)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)	IIP3 (dBm)	Power (mW)
GSM (1.85-1.99)	<1.61	>24.7	<-10.9	<-16.7	0.7	53.3
WCDMA (1.92-2.17)	<1.73	>20.6	<-7.9	<-5.5	-0.15	28.5
Bluetooth (2.4,2.4835)	<1.77	>16.2	<-10	<-5.2	-0.6	25.3
WLAN (2.4,2.4835)	<1.64	>22.3	<-12.4	<-6.3	-3.3	30.5

TABLE V. Comparison with Reported Multi-Standard CMOS LNAs.

Ref.	Standard	NF (dB)	S_{21} (dB)	IIP3 (dBm)	f_c (GHz)	Pow. (mW)	FOM_1	FOM_2
[5]	Bluetooth	2.2	15	3	2.4	7.2	1.2	5.7
	DECT	2.3	17	0.5	1.9	14.4	0.7	1.5
[7]	WLAN 802.11b-g	2.3	14	-1.5	2.4	50	0.1	0.01
	WLAN 802.11a	4.4	13	-1.5	5.3	50	0.05	0.2
	W_1MAX	3.2	13.9	-10	3.5	50	0.09	0.2
[8]	WCDMA	3.9	23.3	-6.3	2.1	9	1.1	0.5
	GSM	2.6	24.9	-21.6	0.95	9	2.4	0.02
[9]*	DCS1800	5.2	28.5	-7.5	2.1	24	0.5	1
	WCDMA	5.6	23.4	0	2.4	24	0.2	0.2
	WLAN	5.8	23.4	-4.8	1.8	24	0.5	0.2
[13]*	GSM	4.6	18	-12.8	1.9	32.4	0.1	0.02
	WLAN	4.4	24	-15.3	2.4	32.4	0.3	0.02
	Bluetooth	4.4	24	-15.3	2.4	32.4	0.3	0.02
[14]*	0.3-2 GHz	4.5	12	-16	1.15	18	0.1	0.003
This	GSM	1.61	24.7	0.7	1.92	53.3	0.7	1.6
Work	WCDMA	1.73	20.6	-0.15	2.04	28.5	0.8	1.5
	Bluetooth	1.77	16.2	-0.6	2.44	25.3	1.5	1.1
	WLAN	1.64	22.3	-3.3	2.44	30.5	0.9	1.1

and MOS-varactor based tuning networks effectively allows the LNA to adapt its performance to the specifications of GSM, WCDMA, Bluetooth and WLAN standards. Transistor-level simulations including technology parasitics verify a correct performance showing a good comparison with previous reported designs. It is important to mention that, although some LNAs in Table V (including this proposal) do not report experimental results, they are included in the comparison study for the sake of completeness. Those references market with an asterisk (*) in Table V correspond to integrated circuits showing experimentally measured performance.

From data shown in Table II, the design of the LNA at the layout level has been developed, and occupies an area of 1.18×1.18 μm^2. The chip prototype is currently under fabrication.

Acknowledgements

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