Assessing application areas for tunnel transistor technologies

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Abstract— **Tunnel transistors are one of the most attractive steep subthreshold slope devices currently being investigated as a means of overcoming the power density and energy inefficiency limitations of CMOS technology. In this paper, projected tunnel transistor technologies are evaluated and compared to LP and HP versions of both conventional and FinFET CMOS in terms of their power and energy in different application areas.**

Keywords— Tunnel transistors, Steep subthreshold slope, Low power, Energy efficieny, Low supply voltage

I. INTRODUCTION

One major difficulty encountered when scaling CMOS tecnhnology is the fact that the 60 mV/decade minimum subthreshold slope (SS) of CMOS devices makes it impossible to lower the threshold voltage without producing unacceptable off-state leakage currents. Consequently, supply voltage cannot be reduced without significantly degrading circuit speed. This results in power density problems for high performance applications requiring nominal supply voltages and energy inefficiency in low voltage applications. The later is related to the large delay increments which rise energy associated to leakage current so much that any advantages obtained by scaling dynamic power with supply voltage are cancelled out. Intensive research is being conducted into devices with steeper subthreshold slopes (SS < 60mV/dec). A smaller SS makes it possible to lower threshold voltage while keeping leakage current under control, facilitating low voltage operation with acceptable speed and thus generating savings in power and energy.

Tunnel transistors are one of the most attractive steep subthreshold slope devices 0, [2]. Subthreshold swing under 60mV/dec has been experimentally obtained in different material systems. Research on III-V TFETS has been advancing rapidly in recent years since this type of transistor has higher ON currents than TFETs made from group IV materials (Si or Ge). The limited ON current is, in fact, one of the major uncertainties of these devices. However, projections now exist for ON currents of 1900μA per micrometer of channel width with 0.4 V supply voltage [3], which would be competitive with respect to high performance MOSFETs. The state of the art in TFET development is reviewed in [4], [5].

Emerging devices need to be evaluated at circuit level for a number of reasons. Benchmarking is necessary to evaluate gains over CMOS and thereby identify the devices which are the most promising candidates for replacing or complementing CMOS under different metrics or in different application areas. Several works have shown TFETs to offer significant power and energy reductions [6]-[11]. Many of them have compared realizations of a given circuit implemented with TFETs with its CMOS counterpart, often producing application dependent figures of merit. Others evaluate the impact of reducing V_{DD}, but again a single TFET versus a single CMOS. However, it would be very interesting to carry out a broader comparison, taking into account not only different application scenarios (high performance, low stand-by power …) but also CMOS devices targeting different objectives (HP, LP) operated at nominal and reduced supply voltages.

In this paper we build up and quantitatively compare power versus frequency curves and energy-delay representations for the FO4 inverters in four different tunnel transistors and four CMOS transistors.

II. EXPERIMENT DESCRIPTION

A. Transistors

Four different tunnel transistor models have been used in this work. All of them are available from the NANOHUB webpage. Two of them have been derived by Pennsylvania State University and the other two by Notre Dame University. They are briefly described below.

TFET models from Pennsylvania State University [12] *:* These are look-up table based Verilog-A models for III-V interband Tunnel Field Effect Transistors based on calibrated TCAD Sentaurus device simulations. The calibrated TCAD TFET models serve as an approximation of full-band atomistic calculation of TFET band diagram and band-to-band tunneling current to generate the DC characteristics. The gate-source and gate-drain capacitance characteristics obtained from the TCAD small-signal simulation are validated with measured transient characteristics of TFETs. For p-channel transistors drive-currents identical to those of the n-channel are assumed. The gate-capacitance characteristic is obtained from a TCAD simulation of a symmetrical device structure as an n-type parameter. Models with gate lengths of 20nm are available for both an InAs Homojunction TFET (TFET_PEN_Homo) and a GaSb-InAs Heterojunction TFET (TFET_PEN_Hete).

TFET models from Notre Dame University [13], [14]*:* The current model, based on the Kane-Sze formula for tunneling, is valid in all four operating quadrants of the TFET. It uses a simple analytic model of the gate drain capacitance. Model parameters derived for different TFET structures showed good

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agreement with atomistic or TCAD device simulations. P-channel transistors assume identical drive-on currents and capacitances. Gate length for both transistors is 20nm. In this work, we use a model for a planar InAs double-gate TFET (TFET_ND_Homo), and a GaN/InN single gate TFET (TFET_ND_Hete).

Four different CMOS transistors have been also evaluated for comparison purposes. All of them are predictive models obtained from the PTM web page [15]. The ones selected were those with channel lengths similar to the available TFETs, namely: conventional 22nm devices for both high performance (Conv_HP, nominal V_{DD} =0.8V) and low power (Conv _LP, nominal V_{DD} =0.95V) applications, and FinFET 20nm transistors for HP (FinFET_HP, nominal V_{DD} =0.9V) and for LSTP (FinFET_LP, nominal V_{DD}=0.9V).

Table I depicts characteristic parameters for the n type transistors from each of these technologies.

TABLE I
NMOS TRANSISTOR CHARACTERIZATION

	I_{OFF} Nom.V_{DD} (nA/μm)	I_{ON} Nom.V_{DD} (μA/μm)	I_{OFF} V_{DD} 0.5V (nA/μm)	I_{ON} V_{DD} 0.5V (μA/μm)	I_{OFF} V_{DD} 0.3V (nA/μm)	I_{ON} V_{DD} 0.3V (μA/μm)
PEN_Homo			1.5	140	1.2	32
ND_Homo			0.3	74	0.4	14
PEN_Hete			8	606	6	206
ND_Hete			9	183	9	83
Conv_HP	121	1382	17	311	5	7
Conv_LP	0.03	599	0.01	1.5	0.001	0.005
FinFET_HP	99	1240	37	379	22	74
FinFET_LP	0.1	722	0.04	82	0.02	0.6

B. *Circuits and measurements*

Inverters load with four identical inverters (FO4 inverters) have been evaluated using the eight transistor types. They were sized using minimum gate length for all the transistors. N-type transistors width is also the minimum allowable in each case (one finger for the FinFETs). CMOS p-type transistors were widened (to twice the minimum value) to compensate for mobility differences. Minimum p-type TFET transistors were used since the models already assumed identical drive-on currents. The Inverters have been characterized in terms of delay and power by simulation in order to take into account the effect of distinctive characteristic of these transistors that impact performance [16].

High_to_low and low_to_high propagation delays have been measured for different supply voltages (V_{DD} from 0.2V to 0.6V for tunnel technologies and up to the nominal supply voltages for CMOS). As a figure of merit, we use the average of these delays referred to as FO4_delay.

Static power has been measured for both constant 0-input and 1-input for the same V_{DD} values and their average has been calculated. Total power for switching input at different supply voltages has also been simulated.

We have calculated average power versus frequency curves, with switching activity (α) as a parameter, using the simulation data obtained.

Also energy per operation has been calculated assuming the inverter was working at the maximum operating frequency determined by its FO4_delay and the circuit logic depth, LD.

The power versus frequency curves and energy versus FO4 curves obtained are presented and discussed in the following sections.

III. POWER VERSUS FREQUENCY

Figure 1 shows the power versus frequency curves for α =0.01. Figure 1a uses a logarithmic scale for both axes and Figure 1b applies a linear scale to better appreciate the maximum operating frequency data. Results are shown for the five tunnel transistors at a supply voltage of 0.5V. Results are also shown for the CMOS transistors, although in this case only the transistor with the best performance in each application area (HP, LP) was selected in order to reduce the number of curves. Curves are therefore shown for the Conv_HP transistors at both nominal supply voltage (0.8V) and at 0.5V, and for the FinFET_LP at 0.9V (nominal supply voltage) and at 0.5V. Maximum operating frequency was calculated assuming a logic depth (*LD*) equal to 50*FO4.

The shape of the curves is as expected, and in accordance with [11]. The flat regions obtained for low frequencies correspond to the dominance of static power. Power increases linearly with frequency once dynamic power starts to dominate. The frequency at which this happens depends on switching activity, supply voltage and also on technological parameters. The off current determines static power while capacitance impacts dynamic power. As expected, the lower the static power, the lower the frequency at which dynamic power dominates.

In Figure 1, it can be observed that at frequencies less than 1 MHz the FinFET_LP is the best in terms of power. From 1 MHz to 100 MHz the only tunnel transistor technology with lower power than the CMOS options displayed is TFET_ND_Homo. From 100 MHz to around 1000MHz, all four tunnel transistors consume less power than CMOS. In Figure 1b, it can be observed that tunnel transistors would also be candidates for power savings from 1.2GHz to around 3GHz. These frequencies are beyond the reach of CMOS at 0.5V but they can be achieved with one of the tunnel transistors. Operating CMOS with higher V_{DD} to raise operating frequency would increase power, and it is clear from the figure that this would be worse than the tunnel transistor technologies. Finally, it can clearly be seen in Figure 1b that HP CMOS at nominal supply voltage has a higher operating frequency than the analyzed tunnel transistor at 0.5V. This analysis assumes supply voltage = 0.5V: TFETs, however, allow larger reductions of supply voltages. This initial comparison therefore needs to be further extended in order to consider different V_{DD} values other than 0.5V.

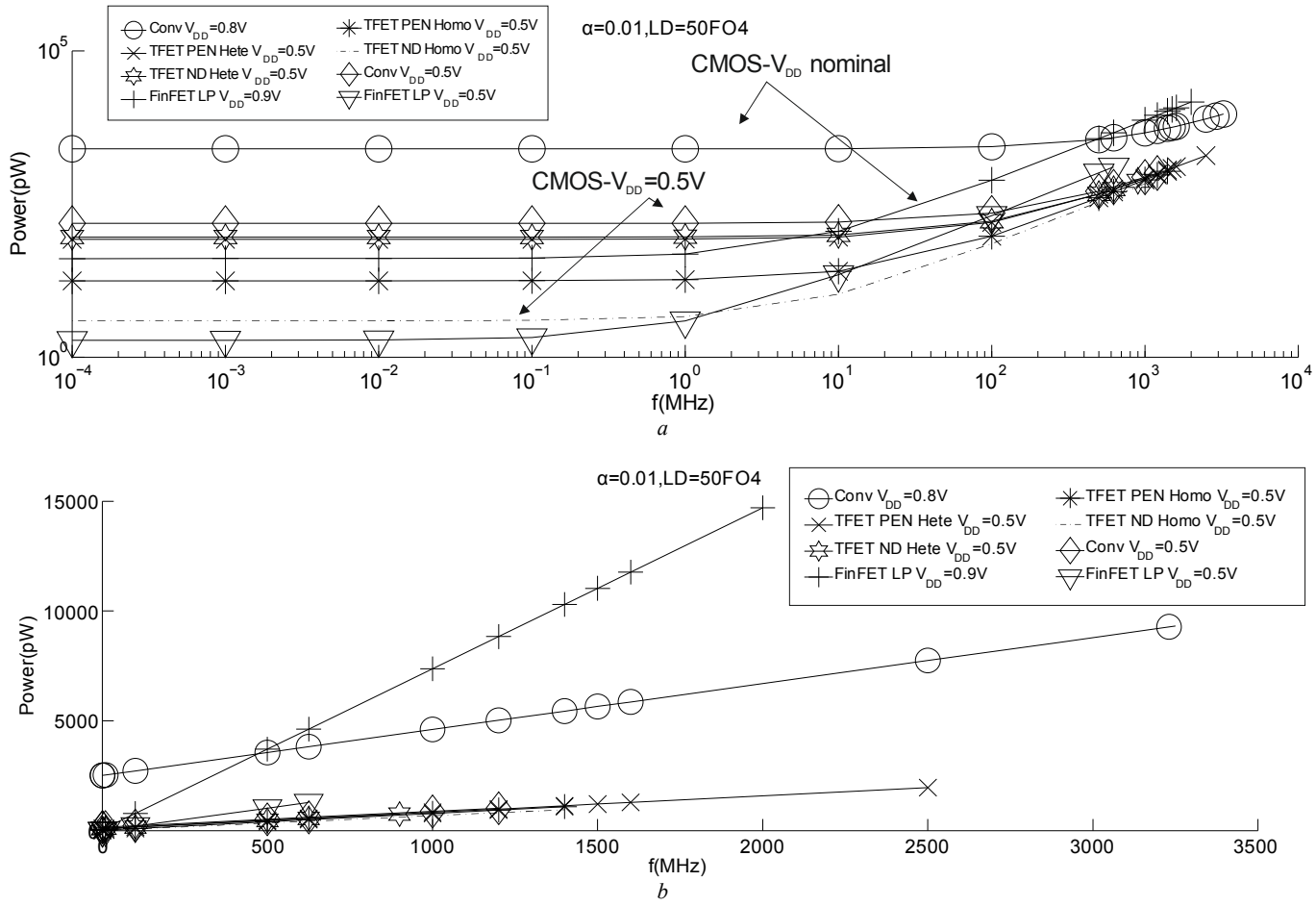

Fig. 1 *Power versus frequency*. CMOS (squares), PEN (triangles), ND (circles). Solid lines (HP, Hete), dashed lines (LP, Homo). TFETS supply voltage 0.5V a) Logaritmic scale. b) Linear scale.

Figure 2 shows the power – frequency curves obtained using V_{DD} = 0.2V for TFET_PEN_Hete and TFET_ND_Hete transistor technologies and V_{DD} =0.3V for TFET_PEN_Homo and TFET_ND_Homo. It shows that the whole operating frequency range covered by CMOS at 0.5V can be achieved with significantly reduced supply voltage using one of the tunnel transistors, producing larger power savings than those observed in Figure 1. Note that up to around 100 MHz less power is obtained with homojunction transistors operated at 0.3V than with heterojunction transistors operated at a further reduced supply voltage equal to 0.2V. Above this frequency, dynamic power, which is proportional to the square of V_{DD}, dominates and heterojunction transistors would be more power efficient. The maximum operating frequency of the TFET_PEN_Hete is higher even at the lower supply voltage (Fig. 2b).

Power savings depend not only on frequency but also on switching activity, and the evaluation of tunnel transistors must therefore also take into account this factor. A larger value of α increases dynamic power consumption, producing larger power values. The differences are appreciable at those frequencies at which this power component dominates. Crossover points on the power versus frequency curves defining suitable frequency regions for each transistor are determined by the switching activity, as are the exact power savings.

To complete the comparison, we analyze power savings assuming given target frequencies and two very different switching activity values. The target frequencies are 1 MHz, 100 MHz and 1.2GHz. For each frequency and transistor technology we selected the lowest supply voltage (starting at 0.2V) at which that frequency was achievable and evaluated the power. Table II shows the results for the four tunnel transistor models for LD=50FO4 with α = 0.01 and α = 0.5. The calculated power data was normalized with respect to the best CMOS inverter (HP or LP) for each frequency. For target frequencies of 100 MHz and 1.2 GHz, the HP CMOS inverter consumed less power. For a 1 MHz target frequency, the LP CMOS inverter obtained better performance in terms of power. For the highest analyzed frequency, power decreased by around one order of magnitude in the TFET_PEN_Hete for both α values. For 1 MHz, no power savings were obtained using any of the tunnel transistors. In fact, very large penalties were obtained at 1 MHz and α = 0.01 for the heterojunction transistors. These penalties were overestimated due to the fact that the minimum V_{DD} value explored was 0.2V, but at such low target frequencies further reduction of supply voltage

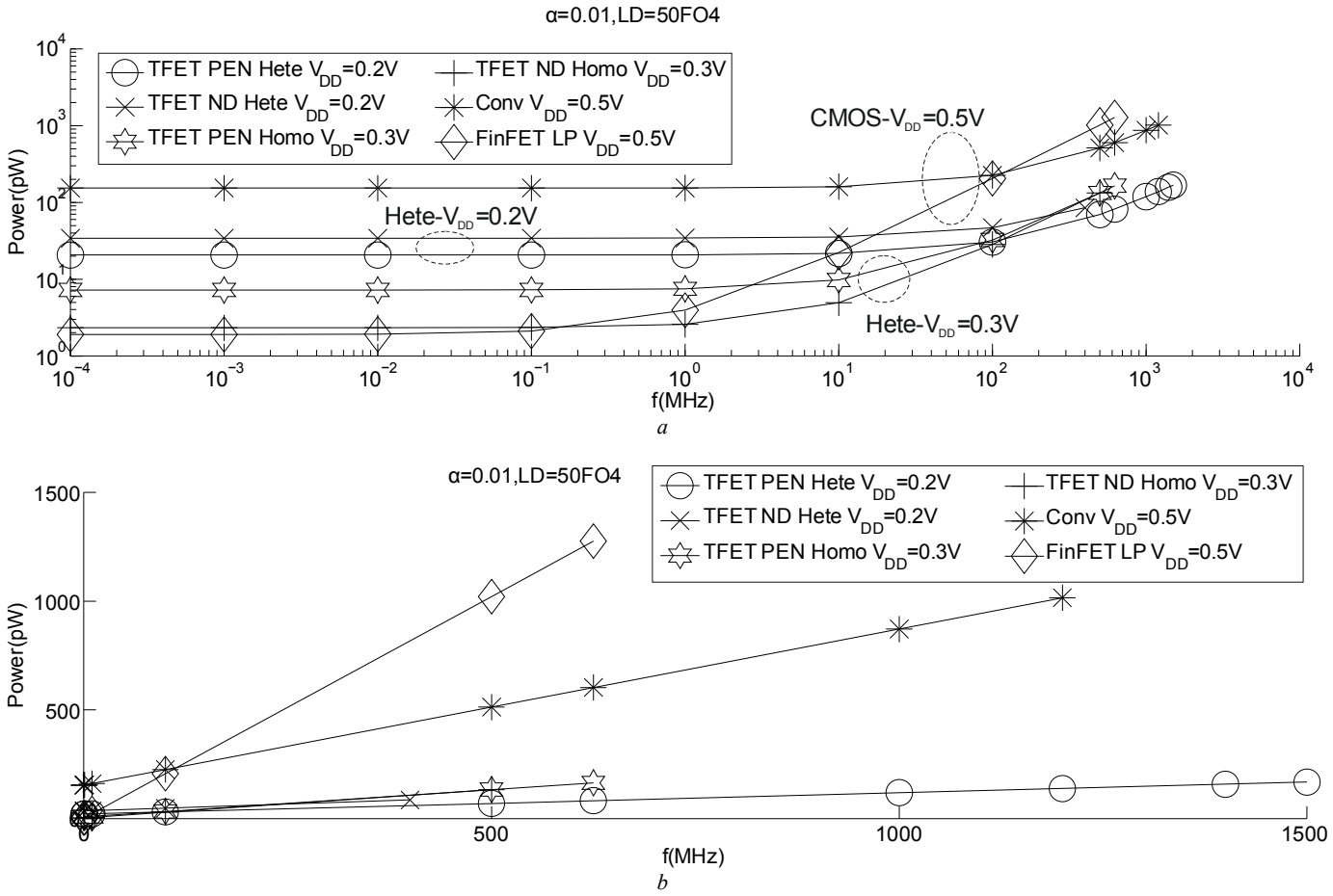

Fig. 2 *Power versus frequency curves*. a) Logarithmic scale. b) Linear scale.

could be possible. In terms of power, therefore, FinFET_LP is competitive within the KHz range of frequencies and with very small switching activities.

TABLE II
NORMALIZED POWER AT DIFFERENT FREQUENCY TARGETS AND SWITCHING ACTIVITIES

	1.2 GHz		**100 MHz**		**1 MHz**	
α	**0.01**	**0.5**	**0.01**	**0.5**	**0.01**	**0.5**
PEN_Homo	0,92	1,06	0,13	0,22	1,72	0,14
ND_Homo	0,80	0,94	0,27	0,56	1,12	0,23
PEN_Hete	0,14	0,14	0,28	0,22	8,93	0,39
ND_Hete	1,68	1,82	0,44	0,29	14,79	0,61

IV. ENERGY VERSUS FO4 CURVES

Figure 3a shows static energy per operation versus FO4 assuming LD = 50FO4 and operation at maximum possible frequency. Note that only one PTM CMOS technology (FinFET_LP) is displayed since this technology produced the best performance in terms of static energy regardless of the operating frequency. In fact, the minimum Conv_HP energy value obtained in this experiment is over 1E-19 J. It can be observed that for low operating frequencies (large FO4 values), the best results with regard to minimum energy were obtained using the FinFET_LP technology. Again, the heterojunction transistor from PEN is competitive for operating frequencies beyond the reach of FinFET_LP. TFET_PEN_Homo offers no advantages and TFET_ND_Homo is the best option for a specific range of FO4 values.

Figure 3b shows total energy per operation versus FO4 calculated assuming LD=50FO4 and α=0.01. Here, Conv_HP is the best CMOS option. It is clear from the figures that in application areas for which energy is the primary design criteria the four tunnel transistors are competitive with regard to CMOS, except for their very low operating frequency and switching activity. The heterojunction transistor from PEN offers much better energy – speed tradeoffs than the others. These transistors can work at a significantly higher frequency with similar energy per operation and so could probably benefit from further supply voltage scaling.

V. CONCLUSIONS

Four projected tunnel transistor technologies have been evaluated and compared to LP and HP versions of both conventional and FinFET CMOS in terms of power versus frequency and energy per operation versus FO4 inverter delay. Advantages were evident not only at low clock frequencies but

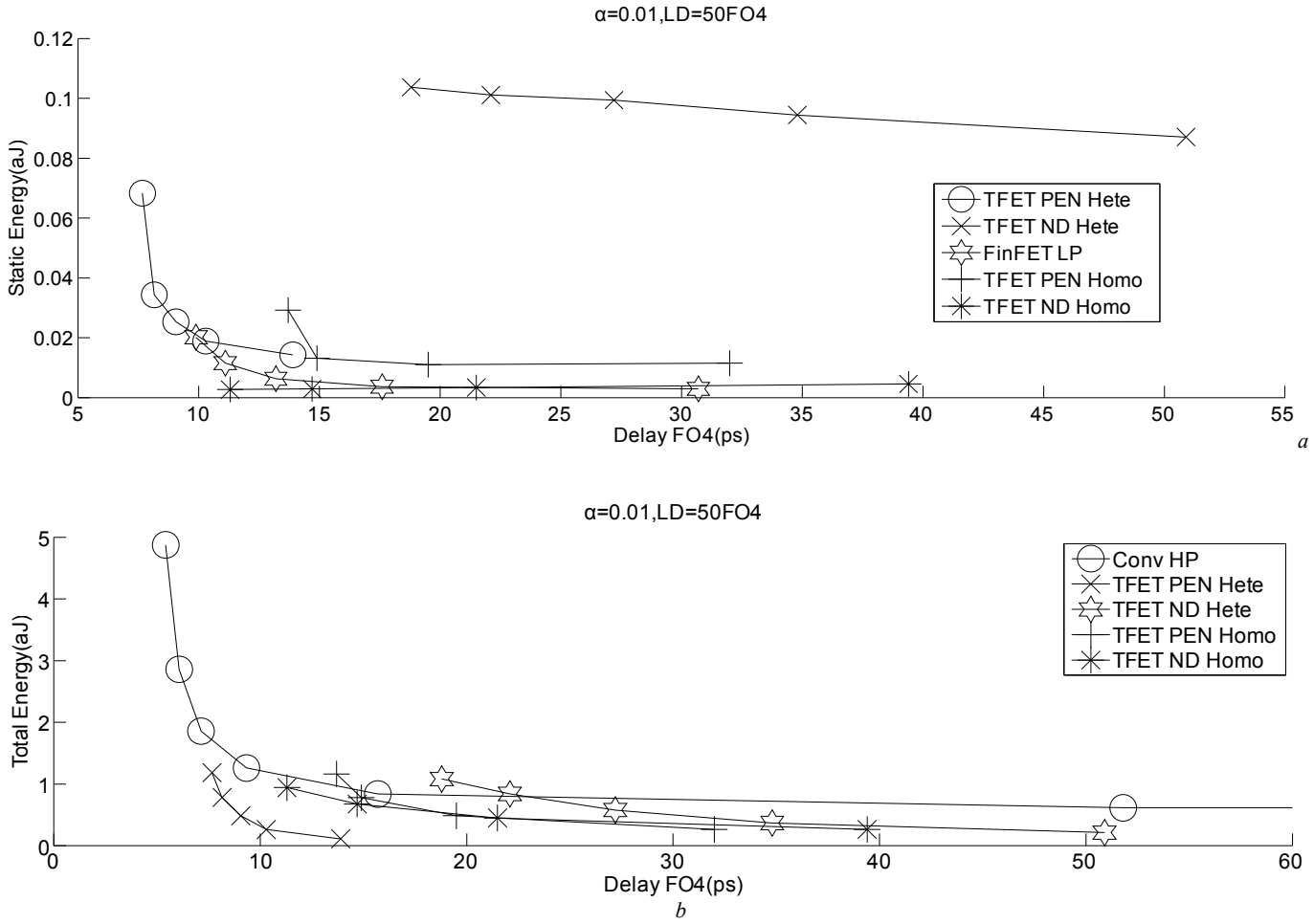

Fig. 3 *Energy versus FO4*. a) Static. b) Total.

also within the GHz range of operation. However, none of the analyzed technologies is competitive in both of those application areas. TFET_PEN_Hete has much better power-speed and energy – speed tradeoffs, while for very low frequency and switching activity applications TFET_ND_Homo technology is the most competitive of all the tunnel transistors studied. Even so, heterojunction transistors with a lower OFF current would be preferable, and we therefore plan to evaluate a Notre Dame-produced model of an AlGaSb/InAs with I_{OFF}=0.001nA/μm.

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