Resonation-based cascade ΣΔ modulator for broadband low-voltage A/D conversion

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This letter presents a novel cascade ΣΔ modulator architecture that employs inter-stage resonation to increase its effective resolution compared to traditional cascades while presenting very relaxed output swing requirements and, subsequently, high robustness to non-linearities of the amplifiers. In addition, the use of loop filters based on Forward-Euler integrators, instead of Backward-Euler integrators as proposed in earlier approaches, simplifies the switched-capacitor implementation and makes the proposed architecture very suited for wideband A/D conversion.

Introduction: The increasing demand for high data-rate A/D converters for the next generation of telecom systems implemented in nanometer CMOS technologies is motivating the exploration of new topologies of wideband ΣΔ Modulators (ΣΔMs) [1]-[3]. Among others, the use of unity Signal Transfer Function (STF) [2] and/or local resonation [3] are demonstrating to be good candidates for low-voltage implementation. On the one hand, by making the STF unity, the integrators ideally process quantization error only, thus relaxing their requirements of amplifier gain non-linearity and output swing. On the other hand, loop-filter resonation allows to optimally distribute the zeroes of the quantization Noise Transfer Function (NTF), such that the in-band noise can be reduced without increasing the number of integrators.

Recently, a new kind of resonation strategy, named *global resonation*, has been applied to cascade ΣΔMs [1]. This new approach, illustrated in Fig. 1 for a fourth-order cascade architecture, is obtained by feeding back the quantization error from the last stage to the previous one. Resonation is achieved through the global path that feeds back a scaled version of the last-stage quantization error at the input of the first-stage quantizer. Note that Backward-Euler (BE) or non-delayed integrators, with a transfer function $H_{BE}(z) = 1/(1-z^{-1})$, are required, which makes its Switched-Capacitor (SC) implementation more difficult. In addition, it uses an extra inter-stage Digital-to-Analog Converter (DAC) —in the path marked with ⊗ in Fig. 1 for clarity.

This letter presents a novel topology of cascade ΣΔM intended for high-speed and low-voltage applications. It combines unity STF with global resonation in an efficient mode and uses only Forward-Euler (FE) integrators, with no extra DAC required, thus circurventing the issues presented in former resonation-based cascade architectures.

Proposed ΣΔM architecture: Fig. 2 shows a modified version of the cascade modulator in Fig. 1. If a linear model is considered for the embedded quantizers, the NTF of both modulators is given by:

$$NTF(z) = \frac{-(1-z^{-1})^2 \cdot [1-(2-K)\cdot z^{-1}+z^{-2}]}{d} \quad (1)$$

where d stands for the inter-stage gain. Note that the zeroes of $NTF(z)$ are a function of K,

whose value can be optimally chosen to maximize the Signal-to-(Noise+Distortion) Ratio (*SNDR*). The modulator in Fig. 2 presents two main advantages with respect to that in Fig. 1:

- The first one is the implementation of global resonation using only FE integrators —with a transfer function $H(z) = z^{-1}/(1-z^{-1})$— instead of using BE integrators, thus simplifying the circuit-level implementation.
- The second one is the use of analog feedforward paths in both stages in order to implement a unity STF, with the subsequent relaxed requirements for the output swings and non-linearities of the amplifiers.

The price to pay for the aforementioned advantages is that an extra analog delay (highlighted in Fig. 2) is required and that an additional DAC is still needed as in Fig. 1 [1]. However, note that these drawbacks can be circumvented as explained below.

If the *Z*-transform of the modulator in Fig. 2 is analysed considering a linear model for the quantizer, it can be shown that the input, x_4, and the output, i_2, of the second integrator in the last stage are respectively given by:

$$\begin{aligned} X_4(z) &= -z^{-1} \cdot (1-z^{-1}) \cdot E_2(z) \\ I_2(z) &= -z^{-2} \cdot E_2(z) \end{aligned} \tag{2}$$

Note from (2) that the delayed version of the last-stage quantization error, $E_2(z)$, can be

directly obtained as

$$X_4(z) + I_2(z) = -z^{-1} \cdot E_2(z) \tag{3}$$

Considering the above relation, the modulator in Fig. 2 can be modified yielding the proposed architecture depicted in Fig. 3. Note that this strategy avoids the use of both an extra analog delay and an inter-stage DAC. This simplifies the electrical implementation and reduces the sensitivity to circuit non-idealities.

Simulation results: The performance of the proposed modulator (Fig. 3) has been compared to a traditional 2-2 cascade $\Sigma\Delta$M and to the resonation-based modulator in Fig. 1 by behavioral simulation using SIMSIDES, a Simulink-based time-domain simulator for $\Sigma\Delta$Ms [4]. All topologies operate with 4-bit internal quantizers, an inter-stage gain (d) of 1, a 1-V reference voltage and a very reduced oversampling ratio of 4. In addition, all the following simulations include kT/C noise sampled by 0.25-pF capacitors at the first integrator. Also, the embedded DACs are assumed to be linear.

Fig. 4 depicts how the in-band quantization noise varies with the inter-stage coefficient K in the proposed topology for an oversampling of 4. As shown in this figure, the rounded optimal feedback coefficient that causes the resonation is $K = 0.4$, resulting in a shift of two zeroes of $NTF(z)$ from 0 to $0.8 \pm 0.6j$. Consequently, the resolution of the proposed architecture increases by roughly 11dB within the whole input range compared to a traditional cascade.

Furthermore, Fig. 5 compares the effect of resonation on the output spectrum of the proposed topology to that of a traditional 2-2 cascade (MASH) for an input level 6dB below full scale (-6dBFS). Note that, thanks to global resonation, a notch —clearly visible in Fig. 5(a)— is introduced close to band limit in the proposed topology.

Another advantage of the proposed architecture as compared to the one in [1] comes from the use of unity STFs, yielding to the subsequent reduction of the amplifiers' output swing. This is illustrated in Fig. 6 by plotting the histograms of the integrator outputs in the architecture proposed in this letter and those corresponding to Fig. 1. Note that the output swing requirements for the proposed modulator —only 0.15V for the 1st and 3rd amplifiers; and 0.1V for the 2nd and 4th ones— are considerably smaller than the ones for the modulator in Fig. 1. This facilitates the low-voltage implementation of the proposed architecture and also translates into a robustness to non-linearities in the amplifiers which is larger than that for the modulator in [1].

Conclusions: A novel topology of cascade $\Sigma\Delta$M has been proposed. It combines a resonation-based loop filter with a unity STF to achieve very reduced output swing requirements for the amplifiers, whereas increasing the modulator resolution and its robustness with respect to non-linearities as compared to previous approaches. These characteristics make the proposed modulator very appropriate for the implementation of low-voltage wideband A/D conversion.

References

1 Sánchez-Renedo, M., Patón, S., and Hernández, L.: 'A 2-2 Discrete Time Cascaded ΣΔ Modulator With NTF Zero Using Interstage Feedback'. Proc. 2006 Int. Conf. on Electronics, Circuits and Systems, 2006, pp. 954-957.

2 Silva, J., Moon, U., Steensgaard, J., and Temes, G.C.: 'Wideband low-distortion delta-sigma ADC topology', *Electron. Lett.*, 2001, **37**, (12), pp. 737–738

3 Markus, J., and Temes, G.C.: "An efficient Delta-Sigma ADC architecture for low oversampling ratios". *IEEE Trans. on Circuits and Syst. I*, 2004, **51**, (1), pp. 63-71.

4 Ruíz-Amaya, J., de la Rosa, J.M., Fernández, F.V., Medeiro, F., del Río, R., Pérez-Verdú, B., and Rodríguez-Vázquez, A.: 'High-level synthesis of switched-capacitor, switched-current and continuous-time ΣΔ modulators using SIMULINK-based time-domain behavioral models', *IEEE Trans. Circuits Syst. I*, 2005, **52**, (9), pp. 1795–1810.

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Figure captions:

Fig. 1 Fourth-order cascade ΣΔM with global resonation [1].

Fig. 2 Cascade ΣΔM with unity STF and global resonation topology.

Fig. 3 Proposed modulator architecture.

Fig. 4 Variation of the in-band quantization noise with coefficient K.

Fig. 5 Modulator spectrum: (a) with and (b) without resonation.

Fig. 6 Histogram of the integrator outputs: a) Global resonation ΣΔM in [1], and b) Proposed ΣΔM (-6dBFS input level).

Fig. 1

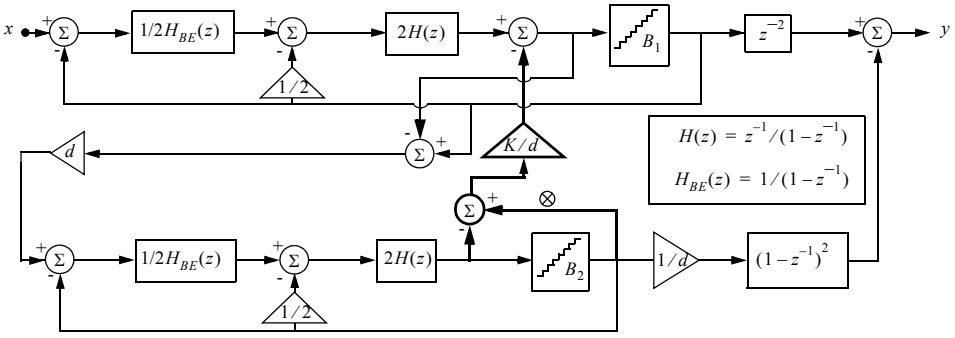


Fig. 2

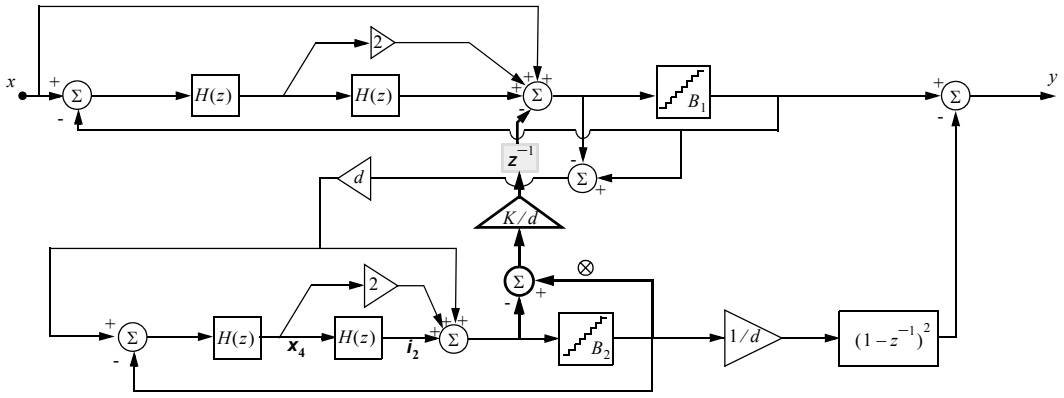


Fig. 3

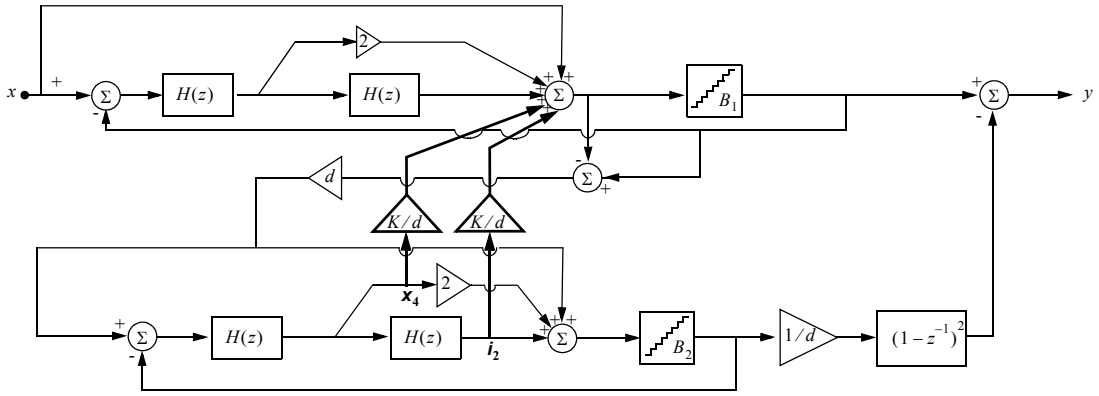


Fig. 4

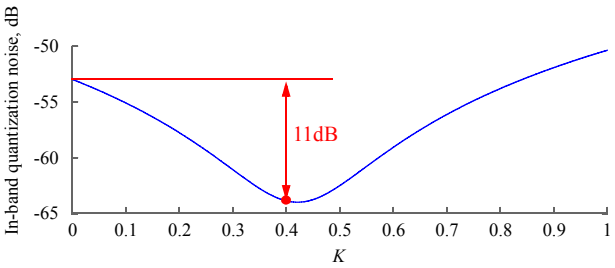

In-band quantization noise, dB
-50
-55
-60
-65
11dB
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
K

Fig. 5

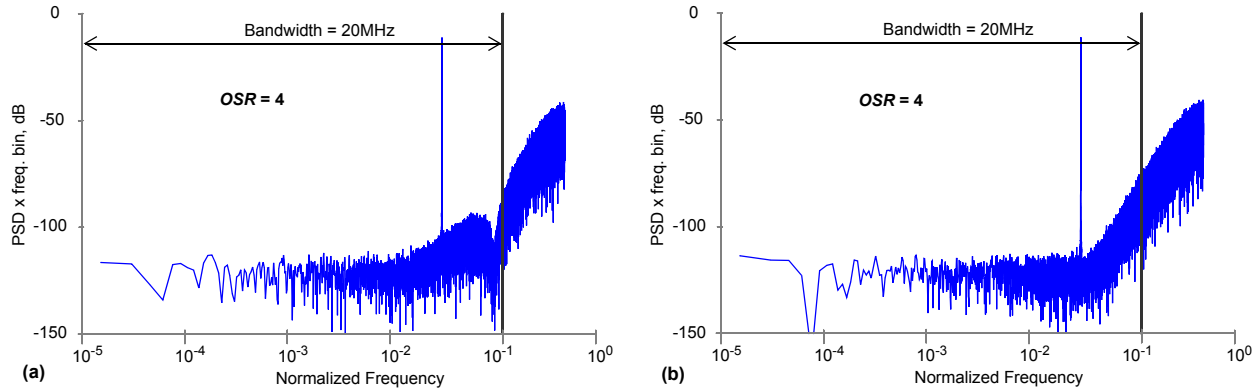
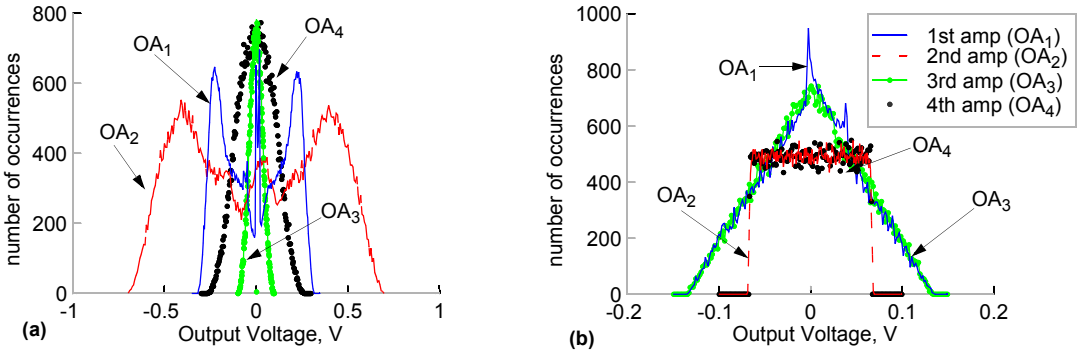

Bandwidth = 20MHz
OSR = 4
PSD x freq. bin, dB
0
-50
-100
-150
10-5
10-4
10-3
10-2
10-1
100
Normalized Frequency
(a)
Bandwidth = 20MHz
OSR = 4
PSD x freq. bin, dB
0
-50
-100
-150
10-5
10-4
10-3
10-2
10-1
100
Normalized Frequency
(b)

Fig. 6


number of occurrences
Output Voltage, V
OA1
OA2
OA3
OA4
(a)
(b)
1st amp (OA1)
2nd amp (OA2)
3rd amp (OA3)
4th amp (OA4)