Introduction to the special issue on Radio Frequency Integrated Circuits (RFIC) Design Techniques

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The growing demand for new and more complex wireless communication devices is pushing continuous innovation in the design of Radio Frequency Integrated Circuits. New and stronger performance requirements are to be met in shorter times-to-market, using technologies which are not always RF-friendly, making the design of these circuits a challenging job.

Miniaturization and cost have driven CMOS technologies as attractive candidates for the design of RF integrated circuits. Furthermore, the scaling of these technologies down to the nanometric regime has pushed their frequencies of operation well into the millimeter-wave region. Currently, CMOS coexists with other high-performance technologies, like SiGe, providing the RF designer with a wide catalog of alternatives for the optimal system design considering a variety of aspects like size, cost, power consumption, performance, etc.

One the most important challenges of RF design is the lack of good simulation and modeling tools that can combine the electrical characteristics of the different devices (active and passive) with their electromagnetic properties when operating at GHz frequencies. The development of new simulation methodologies and mathematical modeling for RFIC are crucial aspects for designing RF circuits that fulfill the requirements of the communication standards and effectively reduce the design time.

In this scenario, the aim of this special issue is to provide researchers in the area with a unique framework where the progress in different aspects of RF integrated circuit design are presented. We sincerely think that this objective has been achieved, with 16 papers covering important topics in the fields of design methodologies and design techniques.

The first paper, by R. Liu, L. Pileggi and J.A. Weldon, presents a wideband harmonic rejection RF receiver that uses a design and calibration method called extended statistical element selection to achieve best-in-class 2nd to 6th order harmonic rejection ratio (HRR).

A detailed study of the impact of technology scaling on the tuning range and phase noise of mm-wave CMOS LC-VCOs is presented by S. Elabd and W. Khalil, where CMOS process nodes from 130nm to 45nm have been studied.

The paper "Layout-Aware Design Methodology for a 75 GHz Power Amplifier in a 55nm SiGe Technology" by D. del Río et al. introduces a method to design mm-wave Power Amplifiers by modeling the electromagnetic behavior of all the passive structures and the layout interconnections using a 3D-EM solver. This is a very important topic in RF design that is also considered by the paper presented by F. Eshghabadi et al. where the die-level electromagnetic interaction between components and parasitic interconnection extraction are evaluated and compared with the measurement results of a 130nm RF CMOS low-noise amplifier (LNA). The aim of this work is to achieve first-pass silicon fabrication success to avoid costly and time-consuming additional fabrications.

R. Fiorelli and E. Peralias present the theory, method of extraction and validation of a simple but accurate semi-empirical RF MOS transistor model for CMOS 65nm technologies that uses as fundamental variable the MOS transistor transconductance to current drain ratio.

A hybrid methodology for the evaluation of the sensitivity of integrated inductors against technological/geometrical parameter variations is proposed by A. Sallem, P.Pereira, MH. Fino and M. Fakhfakh. The results are then used in an optimization-based design environment to guarantee that obtained solutions are robust against parameter variations.

R. Póvoa, I. Bastos, N. Lourenço and N. Horta present the automatic synthesis of RF front-end blocks using multi-objective evolutionary techniques. The sizing of the three circuits is carried out by AIDA (Analog IC Design Automation), a multi-objective multi-constraint simulator based automatic IC design tool, which optimizes analog circuits through the usage of evolutionary computation.

A new method for computing the amplitude and frequency of differential ring oscillators (ROs) is proposed by H. Ghonoodi, H.M. Naimi and M. Gholami in "Analysis of Frequency and Amplitude in CMOS Differential Ring Oscillators".

J. Casoleira, L.B. Oliveira and I.M. Filanovsky investigate the capacitive coupling in quadrature RC-oscillators. The results show an improvement in phase noise with a marginal increase in power requirements. The theory is validated by measurements on a 2.4GHz circuit prototype fabricated in a 130nm CMOS technology.

J. Alves Torres and J. Costa Freire present two monolithic active inductors, aimed at 30GHz operation, implemented on a 0.25μm SiGe technology with 4 metal layers and HBTs with f_T=120GHz. The proposed structures have Q values larger than 30 and peak values above 100 and 200, depending on the active inductor selected.

A. Salimi, R. Dehghani and A. Nabavi present a novel predistortion assisted supply modulator suitable for envelope tracking power amplifiers. A digitally-controlled linear power amplifier is used to compensate the switching noise ripples of the switching modulator.

An interesting low cost system for measurement of AM/AM and AM/PM distortion curves of RF Power Amplifiers (PAs) is presented by J.C. Núñez-Cruz et al. The system, which is based on the phase to amplitude conversion principle, uses an FPGA development board and DSP Builder.

In "Active Inductor-Based Tunable Impedance Matching Network for RF Power Amplifier Application", by A. Saberkari, S. Ziabakhsh, H Martínez and E. Alarcon, a new structure of active inductor, named cascoded flipped-active inductor (CASFAI), is used in a T-type high-pass tunable output matching network of a class-E RF power amplifier (RFPA) to control the output power and enhance the efficiency.

Bastos et al. present a balun LNA designed in a 130nm CMOS technology for biomedical applications with high gain and low noise figure that uses active loads. A double feedback structure is used for gain enhancement and noise figure.

An inductor-less differential Common-Gate Low Noise Amplifier (CGLNA) for the ZigBee standard is introduced by A. Karimlou; R. Jafarnejad and J. Sobhi in "An Inductor-less Sub-mW Low Noise Amplifier for Wireless Sensor Network Applications". The circuit uses shunt feedback and Dual Capacitive Cross Coupling to reduce power consumption

Active inductors are also key elements in the last paper "gm-Boosted Flat Gain UWB Low Noise Amplifier with Active Inductor-Based Input Matching Network" by A. Saberkari, S. Kazemi, V Shirmohammadli and M.C. Yagoub. The proposed circuit consists of three stages and has been designed in a 180nm CMOS technology and operates at a voltage supply of 1.8V.

Finally, we would like to thank all the reviewers that have generously helped in this special issue for their important and valuable work. We would also like to thank the Editor-in-Chief of Integration, The VLSI Journal, for his continuous support and the opportunity to act as guest editors of this special issue. We expect that Integration readers will enjoy this issue as much as we did in its preparation.