

Comparison of TFETs and CMOS using optimal design points for power-speed trade-offs

Juan Núñez and María J. Avedillo

Abstract— Tunnel transistors are one of the most attractive steep subthreshold slope devices currently being investigated as a means of overcoming the power density and energy inefficiency limitations of CMOS technology. In this paper, the evaluation and the comparison of the performance of distinct fan-in logic gates, using a set of widely accepted power-speed metrics, are addressed for five projected tunnel transistor (TFET) technologies and four MOSFET and FinFET transistors. The impact of logic depth, switching activity and minimum supply voltage has been also included in our analysis. Provided results suggest that benefits in terms of a certain metric, in which a higher weight is placed on power or delay, are strongly determined by the selected device. Particularly, the suitability of two of the explored TFET technologies to improve CMOS performance for different metrics is pointed out. A circuit level benchmark is evaluated to validate our analysis.

Keywords— Tunnel transistors, Steep subthreshold slope, Energy efficiency, Low supply voltage, Optimal design points.

I. INTRODUCTION

Tunnel transistors (TFETs) are currently receiving a lot of attention as potential candidates to substitute or complement CMOS devices [1]-[4]. They are one of the most attractive steep subthreshold slope devices. Steep subthreshold slope (SS) enables low voltage operation with acceptable speed leading to power and energy savings. Thus, they are being explored to overcome the power density and energy inefficiency problems exhibited by CMOS due to its 60mV/decade minimum subthreshold slope [5], [6].

Many works have addressed benchmarking of TFETs at the circuit level with different aims, including the extraction of information useful to guide device design [7], the identification of circuit design challenges or opportunities due to the distinguishing features of these transistors [8]-[10], or the comparison to CMOS to evaluate obtained gains and assessing which applications are candidate for replacing or complementing CMOS with TFETs. In particular, there are a lot of works comparing TFET transistors versus CMOS ones for logic applications [11]-[18].

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Juan Núñez and María J. Avedillo are with the Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/Universidad de Sevilla), Av. Américo Vespucio s/n, 41092, Sevilla, Spain. e-mail: {jnunez/avedillo}@imse-cnm.csic.es.

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The latter comparative analyses also follow very different approaches and methodologies. On one hand, some of them rely on analytical expressions using a reduced set of technological parameters such as *on* current, *off* current, input capacitance and supply voltage (V_{DD}). Others uses simulations in order to take into account the great impact of specific features of the TFET transistors including super-linear onset, unidirectional conductance, enhanced Miller Capacitance or dominant gate to drain capacitance on their performance [19], [20].

There are also differences in terms of the circuits considered, from the typical *FO4* inverter to system level benchmarks. Finally, there are many distinct criteria on which basis tunnel and CMOS technologies are evaluated. Each allows illustrating some aspects of the differences among both types of transistors. In several cases, realizations of a given circuit implemented with TFETs are compared with their CMOS counterpart at iso-performance or iso-power points. This is interesting for the practical scenery of designing circuits under operating frequency targets or under power budgets. In other works [18], [11], [21], the minimum energy point is used as a figure of merit to summarize the energy advantages. That is, energy optimized designs are compared. However, energy is just one metric of the generalized family of metrics of the form $P^m D^n$ [22] which represents different trade-offs between power and delay. There is a fundamental relationship between the optimal operating points of a design and the generalized design metrics.

In this paper, a comparative analysis in terms of optimization of a set of widely accepted power-delay design metrics is carried out. Main outstanding key point in our simulation based study is the broad set of technologies which are evaluated: five projected TFET technologies and four CMOS, including MOSFETs and FinFETs, designed for both high performance and low power applications. In addition, switching activity, logic depth and minimum supply voltage are taken into account in our analysis. Using V_{DD} as a design parameter, the average energy per operation (E), energy-delay (EDP) product and power-energy product (PEP) have been obtained and their minimum values evaluated and compared.

The rest of the paper is structured as follows. Section II describes the experiments we have carried out. Results obtained are shown and discussed in Section III. In Section IV, 8-bit adders are evaluated and compared. Finally some conclusions are given in Section V.

II. EXPERIMENT DESCRIPTION

A. Transistors

Five different tunnel transistor models have been used in this work. All of them are available from the nanoHUB website [23]. Two of them have been derived by Pennsylvania State University and the other three by Notre Dame University. They are briefly described below.

TFET models from Pennsylvania State University [24]

These are look-up table based Verilog-A models for III-V interband TFETs based on calibrated Synopsys TCAD device simulations. The calibrated TCAD TFET models serve as an approximation of full-band atomistic calculation of TFET band diagram and band-to-band tunneling current to generate the DC characteristics. The gate-source and gate-drain capacitance characteristics obtained from the TCAD small-signal simulation are validated with measured transient characteristics of TFETs. For p -channel transistors drive-currents identical to those of the n -channel are assumed. Its gate-capacitance characteristic is obtained from a TCAD simulation to take into account that density of states of electrons and holes can be quite different in III-V materials. Models with gate lengths of 20nm are available for both a double gate InAs Homojunction TFET (PSU_{HOMO}) and a double gate GaSb-InAs Heterojunction TFET (PSU_{HETE}).

TFET models from Notre Dame University [25], [26]

The current model, based on the Kane-Sze formula for tunneling, is valid in all four operating quadrants of the TFET. It uses a simple analytic model of the gate drain capacitance. Model parameters derived for different TFET structures showed good agreement with atomistic or TCAD device simulations. p -channel transistors assume identical drive-on currents and capacitances. Gate length for both transistors is 20nm. In this work, we use a model for a planar InAs double-gate TFET (ND_{HOMO}), an AlGaSb/InAs double gate TFET (ND_{HETE,1}) and a GaN/InN single gate TFET (ND_{HETE,2}).

CMOS transistors

Four different CMOS transistors have been also evaluated for comparison purposes. All of them are predictive models obtained from the PTM web page [27]. The ones selected were those with channel lengths similar to the available TFETs, namely: 22nm MOSFET devices for both high performance (MOSFET_{HP}, nominal V_{DD} =0.8V) and low power (MOSFET_{LP}, nominal V_{DD} =0.95V) applications, and 20nm FinFET transistors for high performance (FinFET_{HP}, nominal V_{DD} =0.9V) and for low stand by power (FinFET_{LP}, nominal V_{DD} =0.9V).

B. Circuits and measurements

Fig. 1 shows the circuit used to evaluate and compare logic gates with different fan-in. An inverter, a two-input NAND gate (NAND2) and a three-input NAND (NAND3) gate have been evaluated (in blue). Note that gates under test have been loaded with the parallel connection of four minimum inverters and their inputs were not ideal but generated with chains of inverters.

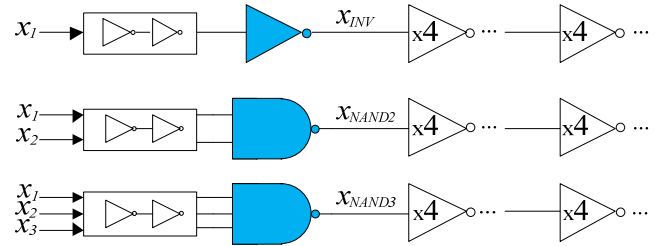


Fig. 1 Circuits used to evaluate the performance of logic gates with different fan in.

Transistor sizing

In all benchmarking circuits transistors have been sized using minimum gate length. n -type transistors width is also the minimum allowable in each case (one finger for the FinFETs). MOSFET p -type transistors have been widened (to twice the minimum value) to compensate for mobility differences. Minimum p -type TFET transistors have been used since the models already assumed identical drive-on currents.

Applying typical scaling rule, n -type transistors have been doubled (multiplied by three) in width in the NAND2 (NAND3) gates to keep similar rise and fall characteristics in all technologies except for FinFETs circuits for which a single finger has been used for all gates.

Measurements

The benchmarking circuits have been characterized by simulation at different supply voltages in order to take into account the effect of distinctive characteristic of these transistors that impact performance, as mentioned above. Specifically, V_{DD} has been varied from 0.05V to 1V (with voltage step equal to 0.05V) for CMOS transistors and from 0.05V to 0.7V for TFET devices. For each circuit and technology, minimum allowable V_{DD} has been determined as the minimum supply voltage at which correct functionality is observed with maximum logic swing degradation of 10%. Worst case high-to-low and low-to-high propagation delays have been measured (at $V_{DD}/2$) and the average of these delays, $\Delta_{FO4}(V_{DD})$, has been used to calculate $f_{MAX}(LD, V_{DD})$, the maximum achievable frequency at a given V_{DD} ($f_{MAX}(LD, V_{DD})=1/(LD \cdot \Delta_{FO4}(V_{DD}))$).

Evaluation and comparison in terms of optimization of a set of widely accepted power-delay design metrics, which are members of the generalized family of metrics of the form $P^m D^n$ [22], have been carried out. Thus, different weights are assigned to power and delay depending on which specification is the most relevant concern.

The average energy per operation (E) has been calculated as $E=P(\alpha, f_{MAX})/f_{MAX}$, which corresponds to $m=1$ and $n=1$ in the generalized form of the power-delay metrics. $P(\alpha, f_{MAX})$ is the average power consumption for certain values of switching activity (α) and f_{MAX} (and, thus, of LD and V_{DD}).

We have also evaluated the energy-delay product (EDP) and the power-energy product (PEP) in order to estimate trade-offs between power and speed performances. EDP and PEP

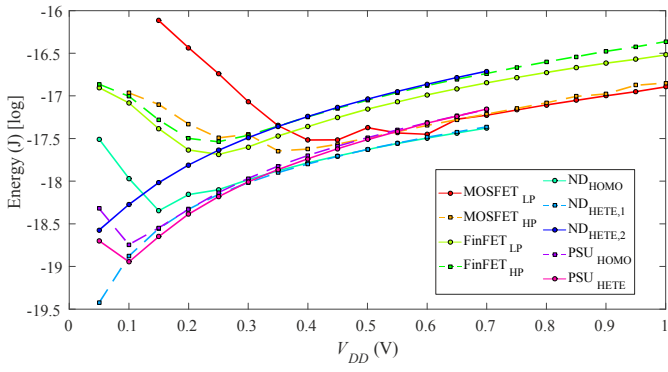


Fig. 2 Energy versus V_{DD} curves for $LD=50$ and $\alpha=0.1$.

have been calculated as follows: $EDP=P(\alpha, f_{MAX})/f_{MAX}^2$ ($m=1$, $n=2$) and $PEP=P(\alpha, f_{MAX})^2/f_{MAX}$ ($m=2$, $n=1$).

III. EVALUATION OF POWER-DELAY METRICS

In this Section, the performances in terms of energy, EDP and PEP of the circuits shown in Fig. 1 are evaluated and compared. For each figure of merit (described in subsections III.A-III.C), results are firstly discussed in detail for the $FO4$ inverter and subsequently provided for NAND2 and NAND3 gates.

A. Energy

Average energy per operation (E) of the $FO4$ inverter versus V_{DD} curves are shown in Fig. 2 for $LD=50$ and $\alpha=0.1$. The minimum energy for each technological node does not necessarily correspond to the lowest V_{DD} . Critical V_{DD} value for minimum energy ($V_{DD,OPT}$) is much lower in TFET than in MOSFET/FinFET in agreement with previous works [18], [11], [21], because the *on/off* current ratio in tunnel technologies is larger (steeper SS) for low values of V_{DD} . In this context, it should be noted that $ND_{HETE,1}$ and $ND_{HETE,2}$ curves have no elbows. It can be also observed that TFET inverters exhibit smaller values of minimum energy than CMOS ones.

The impact of LD and α on the energy performance has been illustrated in Fig. 3. In Fig. 3a, LD has been reduced to 25, without significantly modifying the energy curves but for slight differences in $V_{DD,OPT}$. On the other side, a downward shift of the energy is observed when the switching activity factor is decreased by 10, as shown in Fig. 3b for $\alpha=0.01$. Note that in Fig. 3a LD was only divided by 2 (doubling frequency for a given V_{DD}), which explains the more remarkable impact of α variation with respect to the experiment in which LD is varied.

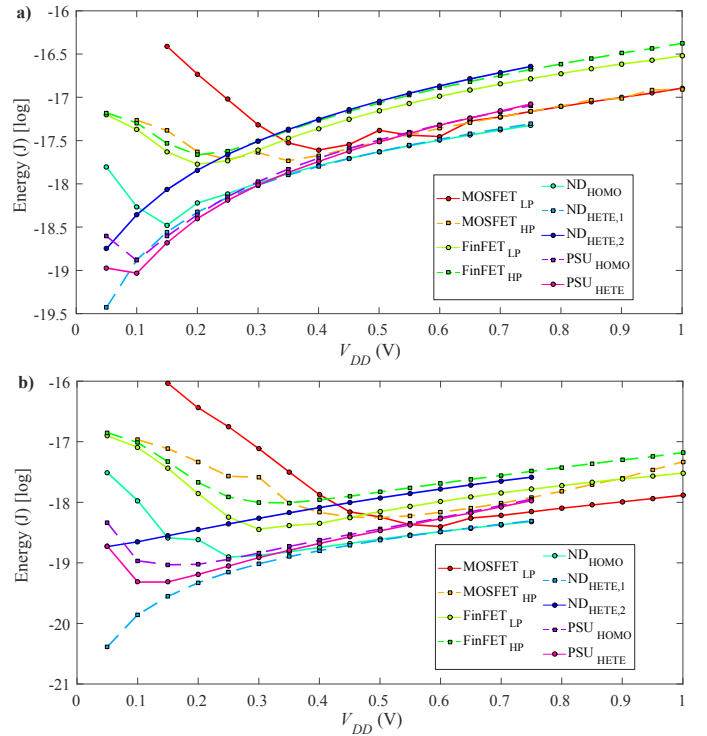


Fig. 3 Impact of LD and α in energy versus V_{DD} curves. (a) $LD=25$, $\alpha=0.1$. (b) $LD=50$, $\alpha=0.01$.

To complete the analysis, minimum average energy per operation has been evaluated for six LD and α combinations and each technology. Results are reported in Table I.

Minimum energies among all the technologies are observed in $ND_{HETE,1}$ inverters (marked in red in the Table) for $\alpha=0.01$ and $\alpha=0.1$. However they are obtained for low frequencies: 1.09MHz ($LD=50$) and 2.18MHz ($LD=25$) and at the minimum V_{DD} . For $\alpha=0.5$, PSU_{HETE} is the most efficient design. The minimum energy is achieved at 14.07MHz ($LD=50$) and 28.14MHz ($LD=25$) with $V_{DD}=0.05V$.

Fig. 4 depicts minimum energy versus frequency of the previous experiments for all CMOS technologies and $ND_{HETE,1}$ and PSU_{HETE} devices. For each technology, we have highlighted the area described by the six solutions. As expected, minimum energy at low frequencies is obtained for $ND_{HETE,1}$. On the other hand, PSU_{HETE} would be the best option to achieve high-frequency operation with the lowest energies. Note that $MOSFET_{HP}$ node exhibits the largest energy values for a wide frequency range and, thus, being not competitive regarding tunnel technologies. Technologies that have not been depicted in Fig. 4 (ND_{HOMO} , $ND_{HETE,2}$ and PSU_{HOMO}) cover the medium energy/frequency range.

TABLE I. MINIMUM E , EDP AND PEP VALUES FOR $FO4$ INVERTER

Technology	(LD, α)					
	(25,0.01)	(25,0.1)	(25,0.5)	(50,0.01)	(50,0.1)	(50,0.5)
MOSFET _{LP}	0.3737	2.4606	8.8567	0.3980	3.0362	10.3631
	0.0008	0.0075	0.0376	0.0015	0.0151	0.0751
	0.1846	0.2971	0.3177	0.2585	0.5891	0.6095
MOSFET _{HP}	0.4055	1.8506	2.4745	0.5561	2.2638	4.8003
	0.0002	0.0011	0.0049	0.0004	0.0025	0.0102
	10.0510	10.2191	10.9841	20.0841	20.2521	21.0061
FinFET _{LP}	0.2993	1.6818	4.5602	0.3590	2.0569	6.3455
	0.0005	0.0055	0.0273	0.0011	0.0109	0.0546
	0.2018	0.2686	0.2825	0.2674	0.5339	0.5476
FinFET _{HP}	0.6313	2.1621	4.5993	0.9795	2.9028	7.7446
	0.0003	0.0023	0.0111	0.0008	0.0048	0.0224
	218.2801	191.3001	92.9201	390.0901	412.1501	300.5821
ND _{HOMO}	0.0994	0.3317	0.5844	0.1246	0.45	1.1171
	0.0002	0.0022	0.0110	0.0004	0.0044	0.02130
	0.15931	0.2712	0.2997	0.2718	0.5356	0.5635
ND _{HETE.1}	0.0039	0.0373	0.1856	0.0041	0.0375	0.1858
	0.0003	0.0028	0.0140	0.0006	0.0056	0.0281
	0.00003	0.0030	0.0752	0.00002	0.0015	0.0377
ND _{HETE.2}	0.0972	0.1785	0.5397	0.18551	0.2668	0.6279
	0.0008	0.0032	0.0128	0.0022	0.0079	0.0283
	0.3985	1.3425	12.2671	0.7248	1.4988	8.3036
PSU _{HOMO}	0.0570	0.1299	0.3287	0.0929	0.1801	0.4995
	0.0004	0.0030	0.0143	0.0008	0.0061	0.0289
	0.0927	0.1239	0.2165	0.1607	0.2283	0.3112
PSU _{HETE}	0.0278	0.0928	0.1571	0.0483	0.1133	0.1707
	0.00003	0.0002	0.0011	0.00008	0.0005	0.0021
	0.2532	0.3179	0.6943	0.4381	0.5621	0.8841
Key	E [aJ] EDP [aJ· μ s] PEP [aJ ² / μ s]					

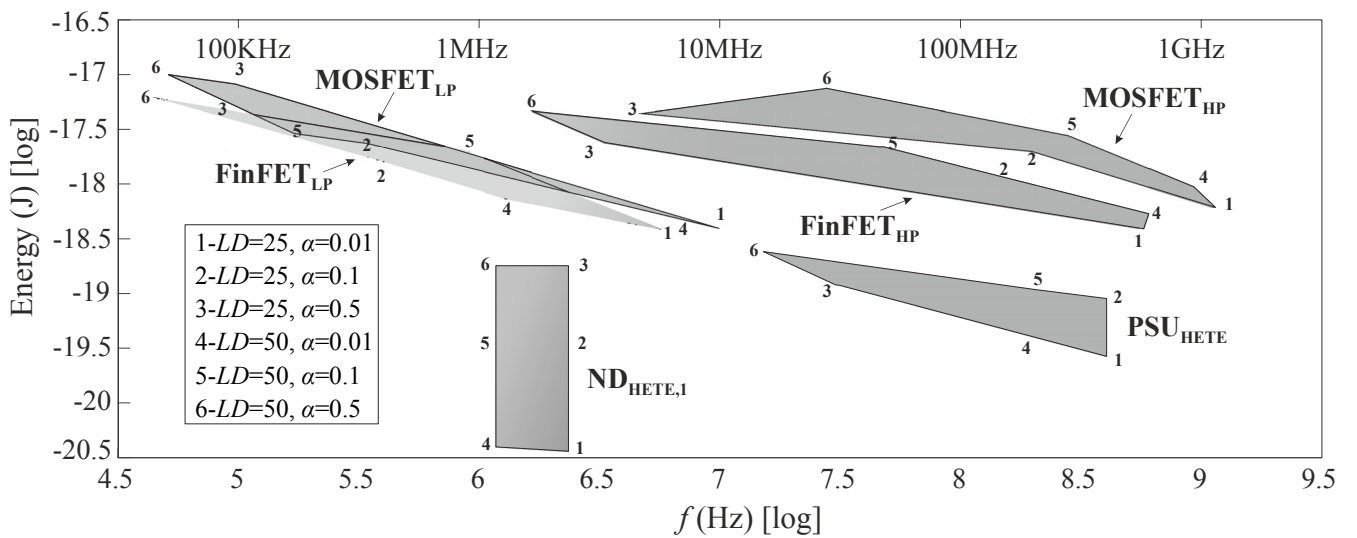


Fig. 4 Minimum energy versus frequency regions for $LD=\{25,50\}$ and $\alpha=\{0.01,0.1,0.5\}$

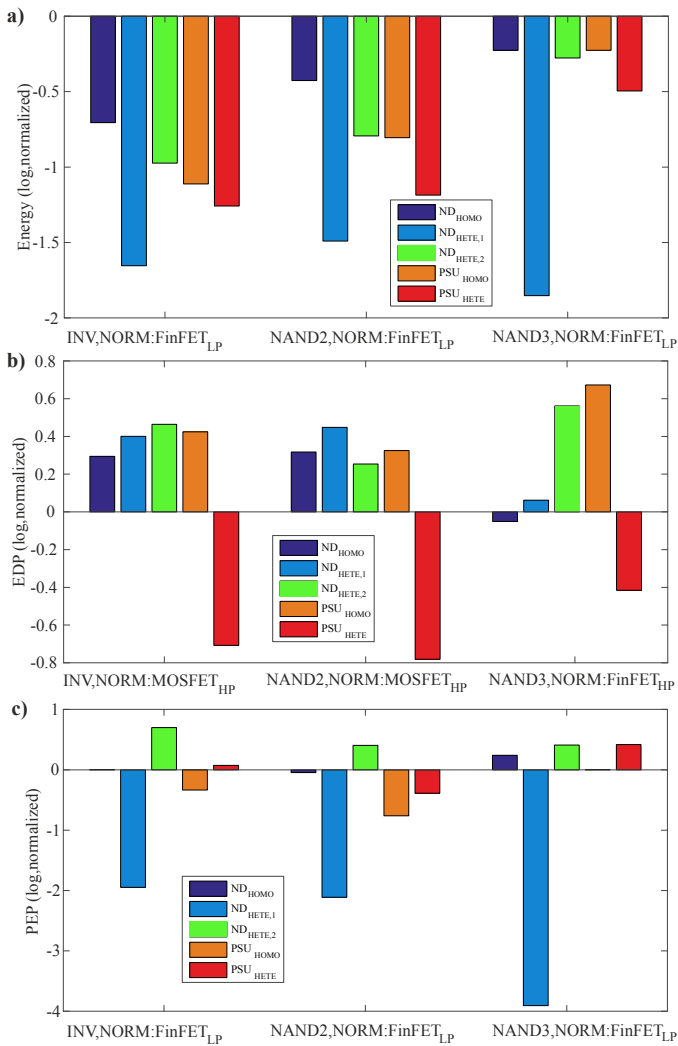


Fig. 5 Bar plots for power-energy metrics for $LD=25$ and $\alpha=0.1$. (a) Minimum energy. (b) Minimum Energy-Delay Product (EDP). (c) Minimum Power-Energy Product (PEP).

Fig. 5a depicts minimum energy of each tunnel technology, normalized with respect to the best CMOS one, for $LD=25$ and $\alpha=0.1$. Results are provided for the three gates. All values have been represented in logarithmic scale, so that negative values correspond to TFET technologies exhibiting better performance than the best CMOS. Note that, in terms of energy, all TFET inverters are more efficient than the best CMOS technology, FinFET_{LP}. As expected, ND_{HETE,1} is the most energy-efficient technology, being 71 (NAND3) to 30 (NAND2) times better than FinFET_{LP}. Results could indicate that advantages in terms of the stack factor could be better in this technology than in FinFET_{LP}. This has been also reported in [7].

It has been also observed that ND_{HETE,1} energy savings are slightly higher for larger values of LD . For $LD=50$ it varies from 75 (NAND3) to 33 (NAND2), both compared again to their FinFET_{LP} counterparts. On the other hand, they are reduced when α increases; i.e. for $\alpha=0.5$ ratios are between 13 (with respect to FinFET_{LP} inverter) and 55 (FinFET_{LP} NAND3).

B. Energy-delay product (EDP)

Results for $FO4$ inverter minimum EDP in Table I show that PSU_{HETE} inverter exhibits the best trade-off in terms of EDP for all scenarios (marked in green), in which frequencies between 376MHz ($LD=25$, $\alpha=0.01$) and 1.58GHz ($LD=25$, $\alpha=0.01$) are achieved at $V_{DD} \leq 0.20V$.

Results in Fig. 5b ($LD=25$, $\alpha=0.1$) show that, in terms of EDP , PSU_{HETE} is the most competitive technology for the three gates, being between 6 times (MOSFET_{HP} NAND2) and 2.6 times (FinFET_{HP} NAND3) better than the best MOSFET/FinFET. Note that, as expected, HP CMOS technologies are now the best for the three gates. However, FinFET_{HP} is the best one only for the NAND3 gate. This result can be explained on the basis of the sizing strategy (described in Section III.B), in which wider pull-down transistors are used in MOSFET and TFET gates when the fan-in is increased (stacked transistors) but identical in the FinFET gates. Unlike the inverter and the NAND2, in which normalized EDP results are quite similar, FinFET_{HP} is the most competitive CMOS technology for the NAND3, which explains the apparent degradation of this figure of merit.

None of the other TFET devices in any of the simulated gates are able to improve best CMOS technology but for ND_{HOMO} in the NAND3. Finally, it has been verified PSU_{HETE} is the most efficient for the explored (LD, α) design space, where no significant variations on the EDP ratios are observed.

C. Power-energy product (PEP)

As shown in Table I for the $FO4$ inverter, ND_{HETE,1} is the best technology in terms of minimum PEP (highlighted in blue) for all (LD, α) pairs. In fact, minimum energy designs are also optimum in terms of PEP for $\alpha=\{0.01, 0.1\}$. Normalized PEP ratios are depicted in Fig. 5c for the three gates with $LD=25$ and $\alpha=0.1$. Again ND_{HETE,1} is the most efficient technology (compared to FinFET_{LP}) for the inverter (88 ratio), NAND2 (129) and NAND3 (8040). Again, benefits due to the stack factor compared to FinFET_{LP} are observed, as described above for energy results.

The impact of LD and α variations is very similar to that exhibited for energy results. That is, PEP ratio of ND_{HETE,1} (compared to FinFET_{LP}) increases (decreases) when LD (α) does.

D. Effect of the variation of $V_{DD,MIN}$

The impact of $V_{DD,MIN}$ on these figures of merits has been analyzed for ND_{HETE,1} (in Fig. 6a) and PSU_{HETE} (Fig. 6b) technologies. Similar behavior are observed for both devices: energy savings regarding MOSFET_{HP} are reduced for larger values of $V_{DD,MIN}$ because, as shown in Fig. 3a, advantages of TFET technologies for low V_{DD} are exploited to a lesser extent. A similar trend is obtained for PEP when $V_{DD,MIN}$ is increased since, for those technologies, also power advantages due to their operation at ultra-low power are weakened. However EDP does not exhibit significant variations because, for both TFET technologies, V_{DD} for minimum EDP is 0.2V and, thus, only for the $V_{DD,MIN} = 0.25V$ scenario the performance is slightly reduced.

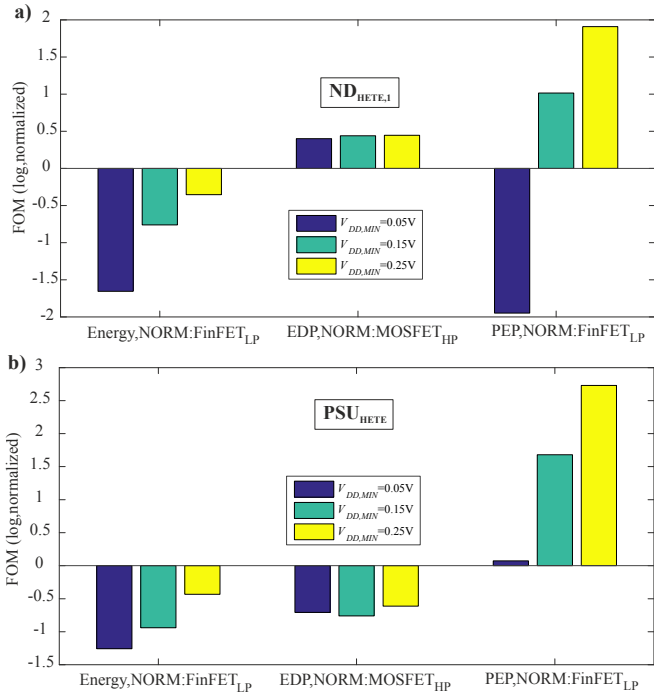


Fig. 6 Impact of $V_{DD,MIN}$ on normalized energy, EDP and PEP for the FO4 inverter designed with ND_{HETE,1} and PSU_{HETE} transistors.

IV. CARRY PROPAGATION ADDER RESULTS

A circuit level benchmark was also included, included in order to take into account some issues, which had not appeared in previous experiments, but which could have an impact on speed or power. These phenomena includes glitches due to the propagation of signals through paths with different delays, leading to extra power, and sustained noise voltage pulses due to capacitive coupling and the asymmetric conduction exhibited by TFET devices, leading to delay degradation [8], [10]. An 8-bit ripple carry adder (RCA) was chosen for this circuit level analysis. An RCA is built by interconnecting full-adders (FA). Fig. 7a shows the logic diagram we used for the FA. Note that it comprises inverters and NAND gates. Average E , EDP and PEP versus V_{DD} curves have been derived for the RCA, similarly to the gate level experiment, and using the ranges of V_{DD} voltages for each technology of the previous experiment. Simulations required to obtain them apply 100 random input combinations.

Fig. 7b shows minimum energy, EDP and PEP for the 8-bit RCA adders implemented with the three heterojunction TFET technologies. The homojunction TFETs are omitted, since they were not shown to be competitive in any of the comparisons carried out at gate level in the previous sections. Results have been normalized with respect to the best CMOS device.

These experiments exhibit significant differences regarding those performed at gate level. Logic paths from the inputs to the outputs are now a combination of different gates (inverter, NAND2 and NAND3) and with different switching activity values. LD is given by the own architecture of the circuit. Note that, since random inputs are applied, large values of α are

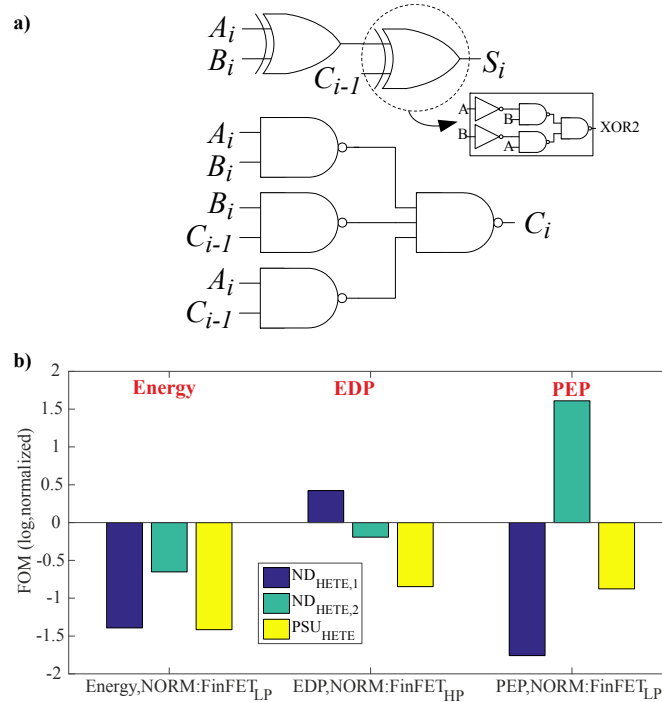


Fig. 7 (a) Logic diagram of one of the full-adders (FA) of an 8-bit ripple-carry adder (RCA). (b) Normalized energy, EDP and PEP of the designed 8-bit RCA implemented using the three heterojunction tunnel technologies.

expected. Nonetheless, good agreement with the results obtained at gate level is observed.

Again, all TFET technologies exhibit better energy performance than the CMOS device, being ND_{HETE,1} and PSU_{HETE} the most efficient technologies. Note that the significant differences between ND_{HETE,1} and PSU_{HETE} in Fig. 5a are not observed now. This is due to the distinct switching activity in both experiments. Increasing α has a larger impact in the minimum energy value for ND_{HETE,1} than for PSU_{HETE}. This can be observed in Fig. 4 from the shapes of the drawn regions for both technologies. In fact, comparing points 3 (the largest α value represented) for both technologies, it is clear the similarity of the minimum energy values. In terms of EDP , PSU_{HETE} exhibit the best performance, keeping the relative differences with respect to the other TFET devices. Finally, for PEP , ND_{HETE,1} is still the best TFET device, whereas similar trends for the other tunnel devices are observed.

V. CONCLUSIONS

In this paper, we evaluate a set of metrics which provides a measure of the performance of distinct circuits implemented using CMOS and TFET technologies. Thus, limitations of a simple estimation of TFET energy savings, achieved by reducing V_{DD} with respect to CMOS technologies, can be overcome. Those metrics include power and delay (frequency) since they are the two most important design specifications. Moreover, we have discussed the impact of switching activity, logic depth or minimum supply voltage on the performance and advantages of TFETs devices.

As in conventional CMOS technologies, a single TFET device is not competitive to optimize a design to achieve a minimum

value for any metric. Among the five explored TFET technologies in this work, two of them have been identified as candidates to improve CMOS performance. Specifically, $ND_{\text{HETE},1}$ transistors exhibit significant advantages for both energy and PEP with respect to CMOS (even regarding LP devices) since power is weighted equal or higher than frequency. On the other hand, the PSU_{HETE} has shown to be greatly advantageous in terms of EDP , for which frequency is the primary concern. It is also competitive in terms of energy with respect to $ND_{\text{HETE},1}$ for high switching activity applications. In the circuit level example, only PSU_{HETE} exhibits advantages in the three analyzed figures of merit compared to CMOS technologies.

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