TFET-based Well Capacity Adjustment in Active Pixel Sensor for Enhanced High Dynamic Range

J. Fernández-Berni, M. Niemier, X. S. Hu, H. Lu, W. Li, P. Fay, R. Carmona-Galán and Á. Rodríguez-Vázquez

We present a Tunnel Field-Effect Transistor (TFET)-based pixel circuit for well capacity adjustment that does not require subthreshold operation on the part of the reset transistor. In CMOS, this subthreshold operation leads to temporal noise, distortion and Fixed Pattern Noise (FPN), becoming a primary limiting performance factor. In the proposed circuit, we exploit the asymmetric conduction associated with TFETs. This property, arising from the inherent physical structure of the device, provides the selective well adjustments during photo-integration which are demanded for achieving High Dynamic Range (HDR). A GaN-based heterojunction TFET has been designed according to the specific requirements for this application.

Introduction: The foreseeable end of CMOS scaling is a well-known motivator for the exploration of alternative transistor technologies. As a first step, it is expected that beyond-CMOS devices might perform specialized functions in chips that are still primarily comprised of CMOS transistors [1]. This Letter fits into such scenario, with a Tunnel FET (TFET) playing a performance-boosting role in a standard Active Pixel Sensor (APS) circuit used in various imaging chips. Among beyond-CMOS devices discussed in the literature, TFET stands out as a leading candidate for low-power logic applications [2]. This arises from the projected ability to achieve sub-60-mV/dec subthreshold swings at room temperature. Its physical operating principles have been extensively discussed [3]. Notably, ambipolar conduction and drain-source asymmetry associated with TFETs are two features that can lead to a significant departure from design techniques employed for CMOS technologies. While different materials and configurations have been proposed for its realization, an embodiment providing the device designer with a large flexibility to render diverse I-V characteristics is the III-nitride heterojunction TFET [4]. This flexibility comes from the ability to tune the band diagram via polarization engineering of the heterointerfaces. Polarization-enhanced tunneling has been experimentally demonstrated in GaN/InGaN/GaN and GaN/AlGaN/GaN tunnel junctions [5], proving the practical feasibility of this approach. In our case, the device has been tuned to sharpen the drain-source asymmetry. Specifically, we present a direct application of TFET asymmetric conduction for the benefit of a mixed-signal circuit that is highly dependent on subthreshold operation in CMOS realizations. The exploitation of TFET physics enables a more precise and effective operation where subthreshold conduction plays no limiting role.

Pixel Circuit for Well Capacity Adjustment: A standard 3T APS is shown in Fig. 1(a) where the reset transistor M_{rst} becomes a lateral overflow gate during photointegration. This gate enables excess photocharge generated by highly illuminated pixels to flow into its drain according to the successive potential barriers set by $r(t)$. This is a well-known technique that increases the available well capacity per pixel. This in turn increases the dynamic range of the sensor, which is a key figure of merit for many image sensor applications. Advantages of this technique include simplicity, large pixel fill factor, and excellent low light performance [6]. Conversely, it suffers from added temporal noise and a large pixel-to-pixel performance variation due to the fact that the overflow gate exploits its subthreshold region to drain the excess photocharge. This technique can be equally applied to 4T APS. However, we focus on a 3T pixel in order not to add unnecessary elements to the simulations, specifically the charge transfer process, which could distort the analysis of the TFET performance. As a reference for the nominal operation of this HDR technique in CMOS, we have simulated a photointegration period for photocurrents ranging from 10fA to 600fA with a minimum-size nMOS reset transistor from the UMC 0.13µm CMOS Image Sensor (CIS) process. In order to analyze the influence of the lateral overflow gate on the targeted behavior, both the source follower M_{sf} and the row selector M_{row} are removed from the simulations. Likewise, we consider an ideal sensing capacitor C_{pd} and a photodiode modeled as an ideal current source I_{pd}. The simulation results are depicted in Fig. 1(b). Two potential barriers are set at $V_{b_1} = 0.85$V and $V_{b_2} = 0.6$V. According to these barriers, over-illuminated pixels should be ideally clipped at exactly $V_{px_1} = V_{b_1} - V_{th}$ and $V_{px_2} = V_{b_2} - V_{th}$ respectively, where V_{th} is the threshold voltage of the reset transistor. However, it can be observed that the resulting response deviates from the expected dynamics. The transition of the overflow gate from off to its subthreshold region depends on both the pixel signal and the barrier established. In order to evaluate this deviation, we have built a behavioral model where we allow for V_{th} to vary according to the specific barrier established. In other words, this model encompasses the distortion caused by the body effect. Over-illuminated pixels are therefore clipped at $V_{px_1} = V_{b_1} - V_{th_1}$ and $V_{px_2} = V_{b_2} - V_{th_2}$ in our model. After applying least squares to fit this model into the simulations in Fig. 1(b), we obtain that $V_{th_1} = 0.12$V and $V_{th_2} = 0.07$V. Finally, we have calculated the error in terms of signal range percentage between the final pixel voltages, i.e. $V_{px}(t = 30\text{ms})$, from the dynamics in Fig. 1(b) and from our behavioral model. The results are plot in Fig. 1(c). The maximum error is 4.88% at $I_{pd} = 190$fA whereas the average error is 1.26%.

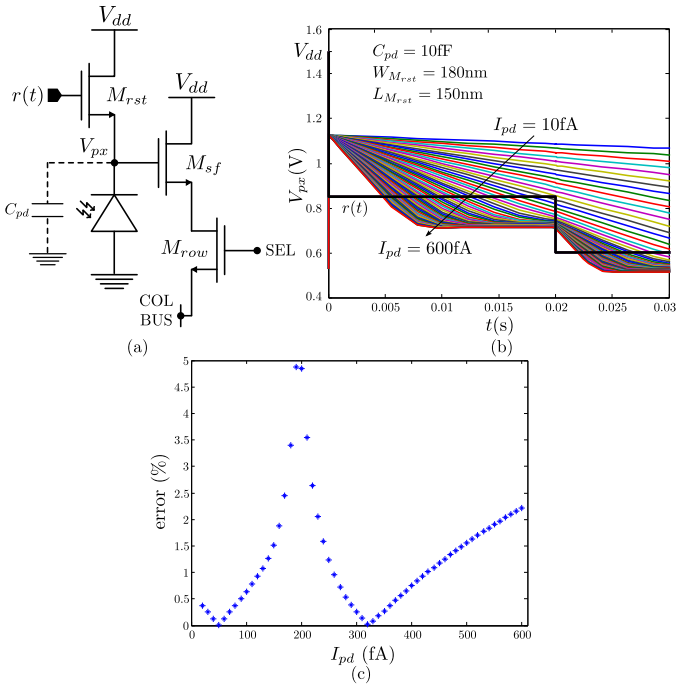

Fig. 1 *(a) Standard 3T APS where the lateral overflow gate is adjusted during photointegration in order to increase the available well capacity; (b) Simulation results with a minimum-size nMOS reset transistor from the UMC 0.13µm CIS process; (c) Error in terms of signal range percentage with respect to an ideal behavioral model.*

TFET-based Well Capacity Adjustment: To overcome the dependence on subthreshold operation in CMOS, we propose the scheme depicted in Fig. 2(a). Our strategy is based on the exploitation of the inherent rectifier nature of TFETs rather than their subthreshold region. The gate signal becomes now digital, periodically switching T_{rst} on in order to drain excess photocharge only if $r(t) > V_{px}(t)$. Otherwise, the built-in, asymmetric conduction of the TFET ideally prevents current from being injected into the pixel node. Note that this draining scheme cannot be used in CMOS as MOSFETs feature symmetric conduction. This symmetric conduction would force $V_{px}(t)$ to evolve towards $r(t)$ regardless of their particular values when the overflow gate were switched on. In practice, some current will flow through the nTFET for negative V_{DS}. The physical design of the device must be tuned to ensure that this current is low enough for an accurate circuit operation. Likewise, the on-current for positive V_{DS} must be able to drain the excess photo-charge in a timely manner. A III-nitride heterojunction TFET has been designed per these specifications (see Fig. 3(a) inset). Device design was performed using Synopsys Sentaurus. Since ultra-low off-current is crucial for this application, the simulations included the non-idealities which give rise to leakage, such as gate oxide tunneling, radiative recombination and Shockley-Read-Hall (SRH) recombination.

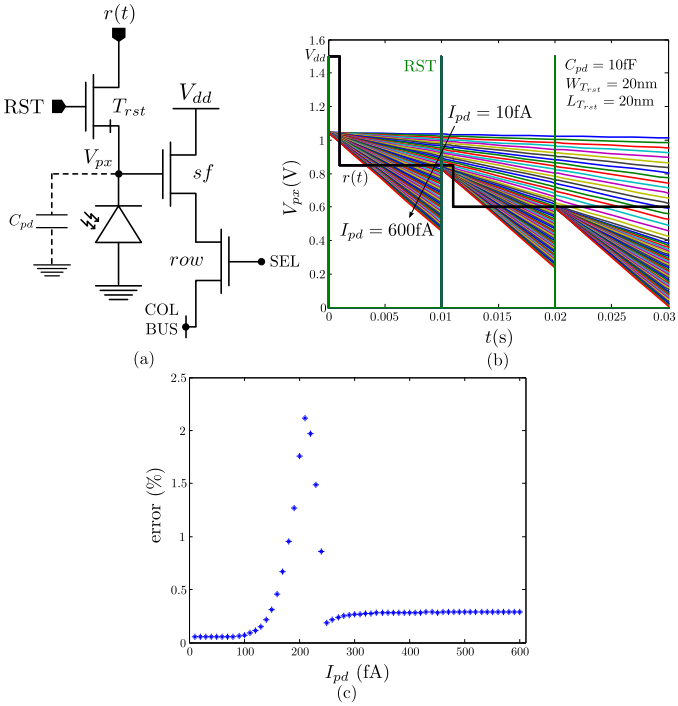

Fig. 2 *(a) 3T APS where the lateral overflow gate is implemented by exploiting the drain-source asymmetry of TFETs; (b) Simulation results with the GaN TFET in Fig. 3; (c) Error in terms of signal range percentage with respect to an ideal behavioral model.*

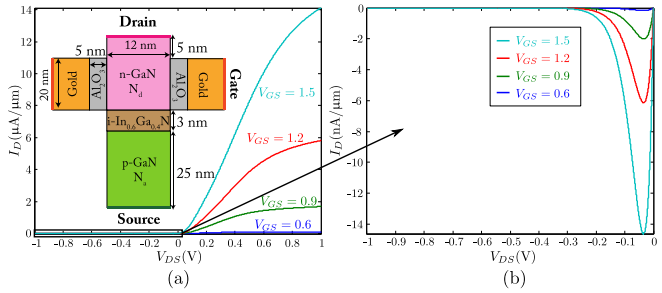

Fig. 3 *III-nitride heterojunction TFET for implementation of well capacity adjustment based on drain-source asymmetric conduction.*

To minimize the current for negative V_{DS}, the InGaN polarization-engineered interlayer is both thicker (3nm) and has a lower indium composition (60%) than in devices targeting high-performance digital logic [4]. This results in a "straddling" rather than "broken" effective band alignment in the device. Under forward bias operation ($V_{DS} > 0$, $V_{GS} > V_{th}$) this design selection reduces the on-current density due to lower inter-band tunneling probability. Under reverse conditions ($V_{DS} < 0$, $V_{GS} > V_{th}$), this strongly suppresses drain current as the full GaN band gap (3.4eV) appears as the thermionic barrier to reverse current. Fig. 3(a) reports the resulting drain current vs. drain-source voltage obtained after fitting TCAD simulations into the universal analytic model from [7]. Fig. 3(b) depicts a more detailed representation of the negative V_{DS} region. The drain current for negative V_{DS} is notably small over a wide signal range, reaching a maximum absolute value of 14.62nA/μm at $V_{DS} = -0.035$V, $V_{GS} = 1.5$V. For positive values of V_{DS}, the drain current is smaller when compared to design targets for TFET digital switches. However, this is quite acceptable due to the small capacitance to be driven. Furthermore, the APS application has more relaxed timing requirements when compared to those associated with digital designs.

In order to compare a design based on the TFET just presented with the CMOS design previously described, the same conditions are set for simulation. The source follower and the row selector are removed, the same ideal sensing capacitor is used and the same sweep of photocurrents is applied. The excess photocharge is drained according to the same potential barriers as well, namely $V_{b_1} = 0.85$V and $V_{b_2} = 0.6$V. Unlike the gradual draining in the CMOS circuit as the overflow gate gets into its subthreshold region, draining in the TFET circuit takes place abruptly when T_{rst} is switched on by the digital gate signal RST. The results are depicted in Fig. 2(b). A first advantage of the TFET-based approach is that over-illuminated pixels are ideally reset at exactly the prescribed voltages of the barriers for each adjustment of the well capacity. No threshold voltage fitting is thus required. We have built a behavioral model that incorporates this ideal resetting. A second advantage of employing the proposed TFET is the extended signal range thanks to the absence of an overdrive voltage directly involved in the well adjustment. The pixel swing in Fig. 1(b) is constrained to [0.51V,1.06V] whereas the swing in Fig. 2(b) is [0.004V,1.01V]. Finally, TFET operation gives rise to smaller error than its CMOS counterpart. As we did in Fig. 1(c), Fig. 2(c) depicts the error in terms of signal range percentage between the final pixel voltages from the dynamics in Fig. 2(b) and the final pixel voltages provided by the aforementioned behavioral model based on exact reset of over-illuminated pixels. The maximum error in this case is 2.12% at $I_{pd} = 210$fA with an average error over the photocurrent sweep of 0.38%.

Two final comments: first, note that we have focused our analysis exclusively on the nominal operation of both circuits. The reason is that we do not have reliable data yet concerning mismatch, temporal noise etc. for the TFET device. Nevertheless, the exploitation of inherent physical properties of TFETs in this application makes us confident about them also outperforming MOSFETs when those parameters can be taken into account. Second, the light responsivity of III-nitride TFETs differs greatly from that of silicon, preventing this particular embodiment from being considered as a drop-in replacement for APS in typical planar realizations. However, due to the large band gap of the III-nitride based TFET, these devices can be readily integrated with GaN-based photodiodes for solar-blind imaging applications [8]. For visible or IR imaging applications, integration with Si CMOS imaging arrays or type II superlattice detectors through wafer bonding or conventional flip-chip integration – as used in conventional mid-IR imaging arrays integrated with Si-based read-out ICs – can be employed.

Conclusions: Most research on beyond-CMOS devices is focused on digital logic applications. While obviously important, there are other ways in which characteristics of devices under study can lead to significant benefits when compared to CMOS counterparts – e.g., for enhanced high dynamic range image sensing discussed here. Comprehensive simulations suggest that TFETs can improve the performance of a standard CMOS technique.

Acknowledgment: This work has been funded by the Spanish Government through project TEC2015-66878-C3-1-R MINECO (co-funded by ERDF-FEDER), by Junta de Andalucía through project TIC 2338-2013 CEICE, by the Office of Naval Research (USA) through grant N000141410355 and by the National Science Foundation (USA) through grant 1344531.

J. Fernández-Berni, R. Carmona-Galán and Á. Rodríguez-Vázquez (*Institute of Microelectronics of Seville, CSIC-Universidad de Sevilla, Spain*)

E-mail: berni@imse-cnm.csic.es

M. Niemier, X. S. Hu, H. Lu, W. Li and P. Fay (*Center for Nano Science and Technology, University of Notre-Dame, United States*)

References

1 Nikonov, D. and Young, I.: 'Overview of Beyond-CMOS devices and a uniform methodology for their benchmarking', *Proc. IEEE*, 2013, **101**, (12), pp. 2498-2533

2 Kim, J. *et al.*: 'Vertical type double gate tunnelling FETs with thin tunnel barrier', *Electron. Lett.*, 2015, **51**, (9), pp. 718-720

3 Seabaugh, A. and Zhang, Q.: 'Low-voltage tunnel transistors for Beyond-CMOS logic', *Proc. IEEE*, 2010, **98**, (12), pp. 2095-2110

4 Lu, H. *et al.*: 'Polarization-engineered III-nitride heterojunction tunnel field-effect transistors', *IEEE J. on Exploratory Solid-State Computational Devices and Circuits*, 2015, **1**, pp. 28-34

5 Yan, X. *et al.*: 'Polarization-induced zener tunnel diodes in GaN/InGaN/GaN heterojunctions', *Applied Physics Letters*, 2015, **107**, 163504

6 Fowler, B.: 'Solid-state image sensors', in *Handbook of Digital Imaging*, M. Kriss, Ed., 2015, John Wiley & Sons

7 Lu, H., Esseni, D. and Seabaugh, A.: 'Universal analytic model for tunnel FET circuit simulation', *Solid-State Electronics*, 2015, **108**, pp. 110-117

8 Razeghi, M. and Rogalski, A.: 'Semiconductor ultraviolet detectors', *J. Appl. Phys.*, 1996, **79**, 7433