Resonation-based Hybrid Continuous-Time/Discrete-Time Cascade ΣΔ Modulators – Application to 4G Wireless Telecom

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ABSTRACT

This paper presents innovative architectures of hybrid Continuous-Time/Discrete-Time (CT/DT) cascade ΣΔ Modulators (ΣΔMs) made up of a front-end CT stage and a back-end DT stage. In addition to increasing the digitized signal bandwidth as compared to conventional ΣΔMs, the proposed topologies take advantage of the CT nature of the front-end ΣΔM stage, by embedding anti-aliasing filtering as well as their suitability to operate up to the GHz range. Moreover, the presented modulators include multi-bit quantization and Unity Signal Transfer Function (USTF) in both stages to reduce the integrator output swings, and programmable resonation to optimally distribute the zeroes of the overall Noise Transfer Function (NTF), such that the in-band quantization noise is minimized for each operation mode. Both local and inter-stage (global) based resonation architectures are synthesized and compared in terms of their circuit complexity, resolution-bandwidth programmability and robustness with respect to circuit non-ideal effects. The combination of all mentioned characteristics results in novel hybrid ΣΔMs, very suited for the implementation of adaptive/reconfigurable Analog-to-Digital Converters (ADCs) intended for the 4th Generation (4G) of wireless telecom systems.

Keywords: Sigma-delta modulators, hybrid discrete-time/continuous-time circuits, A/D converters.

1. INTRODUCTION

The fourth generation (4G) of wireless communication technologies involves two main conceptions that go beyond a simple linear extension of the capabilities of the third generation (3G). On the one hand, 4G will significantly increase the data rates as compared with 3G, providing very high speeds, that can exceed 100 Megabits/s (Mb/s) point-to-point download transmission speed while mobile and 1Gigabit/s when walking or stationary. On the other hand, 4G will enable the convergence of cellular (non-IP-based) wireless networks – like GSM and UMTS – with IP-based wireless networks – like WLAN, providing an optimum delivery via the most appropriate network available, in a *concurrent* and *always-best-connected* mode, and allowing smoothly transitions between different networks[1-4] .To that purpose, 4G hand-held terminals and chips must operate over a variety of standard specifications, including different frequency bands, multiple access techniques, duplex methods, number of channels, modulation schemes, data rates etc. For instance, only considering the GSM standard, there are different operating frequency and bands, from 890MHz to 1.9GHz depending on the version that is considered, i.e GSM, EDGE or PCS1900. A similar situation is found in WLAN, where depending on the standard considered (IEEE 802.11 a/b/g/n) the frequency band changes from 2.4 to 5.0 GHz. The same happens with the channel bandwidth, which spans from hundreds of kHz (for instance 200kHz in GSM) to hundreds of MHz or even GHz (500MHz in UltraWideBand, UWB)[5].

Therefore, the future generation of hand-held terminals must incorporate digital transceiver chip-sets, capable to work with *multi-standard* support features [6]. One of the most challenging building blocks in these systems is the Analog-to-Digital Converter (ADC), because of the varying sampling rates and resolutions required to handle the wide range of signals corresponding to each individual operation mode [7].

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The majority of reported multi-standard ADCs use the ΣΔ Modulation (ΣΔM) technique and are implemented with Discrete-Time (DT) circuits [8]. Although changing the oversampling ratio has been the most commonly reconfiguration strategy, the increasing demand for high data rates in new 4G standards restricts oversampling to low values, because of the prohibitive unity-gain frequency requirements of the amplifiers in Switched-Capacitor (SC) integrators [9]. This has motivated the use of Continuous-Time (CT) circuits for the implementation of ΣΔM ADCs. Among other features, CT ΣΔMs provide faster operation than SC ΣΔMs, while keeping acceptable resolution with low power consumption and implicit anti-aliasing filtering. However, a drawback of CT ΣΔMs is their higher sensitivity to some circuit errors, particularly clock jitter and time constant tolerances[10]. Although these problems have been partially solved in a number of mono-standard Integrated Circuits (ICs), they constitute a critical factor in multi-standard applications with so diverse ADC specifications, what explains the few multi-standard CT-ΣΔMs reported so far [11-12].

The mentioned problems have prompted to explore the so-called Hybrid CT/DT ΣΔMs (H-ΣΔMs), that try to take advantage of both CT and DT circuit implementations [9,13-17]. Most reported H-ΣΔMs use CT circuits at the modulator front-end. In addition to increasing the digitized signal bandwidth, this solution benefits of the CT nature of both ΣΔM loop filter, embedding antialiasing filtering, as well as their ability to operate up the GHz range to simplify radio receivers (in terms of circuit complexity and building blocks) because some functionalities (for instance mixing process and filtering) can be merged into the baseband in a more simple way than using DT ΣΔMs.

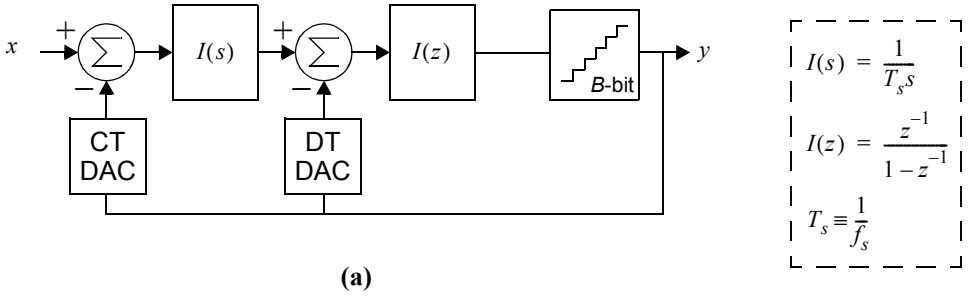
In spite of the mentioned advantages, very little has been done in the design of reconfigurable H-ΣΔMs[17]. This paper contributes to this topic and presents novel two-stage cascade H-ΣΔMs made up of a front-end CT stage and a back-end SC stage. All topologies include programmable resonation to optimally distribute the zeroes of the overall Noise Transfer Function (NTF) such as the in-band quantization noise is minimized for each operation mode. In addition, all stages incorporate unity Signal Transfer Function (STF) to reduce the integrator output swings[18]. The combination of all these strategies result in new hybrid ΣΔMs very appropriate for the implementation of multi-standard ADCs. In order to illustrate the benefits of the proposed ΣΔMs, realistic time-domain simulations are shown that cover a wide range in the resolution-bandwidth plane, corresponding to 4G wireless telecom applications.

2. BACKGROUND ON HYBRID CONTINUOUS-TIME/DISCRETE-TIME ΣΔ MODULATORS

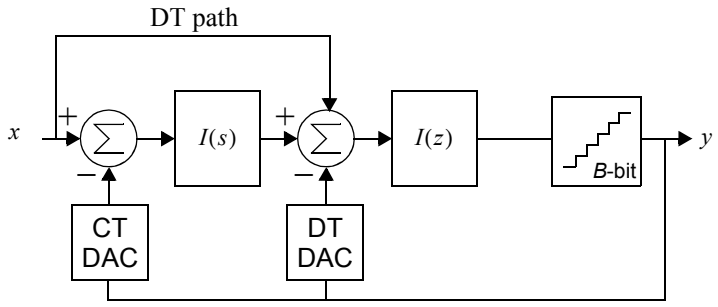
As stated in the introduction, several H-ΣΔM ICs have been demonstrated using both single-loop [15-16] and cascade topologies [9]. In the former case, the most common situation in practice consists of using a CT front-end integrator whereas the remaining integrators in the modulator loop are implemented using DT techniques. This is illustrated in Fig.1 where two different cases of 2nd-order H-ΣΔMs architectures are shown[15-16]. In both cases, the first integrator is CT whereas the second one is DT. However, the modulator in Fig.1(b) uses an additional feedforward DT path from the analog input to the second integrator that forces the CT first stage to process only shaped noise [16]. This technique allows a dynamic range scaling of the first stage that results in a significant reduction in the integrating capacitor size compared to the non feed-forward topology. Note that both modulators use multi-bit quantization. This forces using *scrambling techniques* in order to reduce the effect of non-linearities due to mismatches in the feedback multibit DAC[††].

H-ΣΔM ICs have also demonstrated using cascade topologies. Fig.2 shows the block diagram of the first implemented IC of a cascade H-ΣΔM demonstrating experimental results [9]. It consists of a cascade of a second-order CT-ΣΔM (using RC-active integrators) with a first-order DT (SC) ΣΔM and 4-bit quantization in both stages. This modulator was integrated in a 90-nm CMOS technology achieving a Dynamic Range (DR) of 77-dB in a signal bandwidth of 7.5-MHz, thus demonstrating the feasibility of H-ΣΔMs for the implementation of broadband ADCs. However, in order to make H-ΣΔMs competitive and suitable for the implementation of ADCs in 4G systems, they must significantly increase their conversion speed. Moreover, H-ΣΔMs used in 4G terminals must include reconfiguration capability in order to adapt their performance to the different specifications required for each standard and operation mode. This is the main objective of this work, that proposes new ideas to incorporate the mentioned characteristics in H-ΣΔMs such that they can be used in future 4G transceiver chips.

[††] As in any ΣΔM, practical implementations of CT-ΣΔMs with multi-bit feedback DAC require to incorporate *Dynamic Element Matching* (DEM) techniques to compensate for the non-linearities due to mismatch. These techniques consist basically in changing the elements employed to build each quantization level from cycle to cycle, in a dynamic way, such that non-linear errors are randomized[10].



(a)



(b)

Figure 1. Hybrid CT-DT ΣΔMs proposed by [15] (a) and [16] (b).

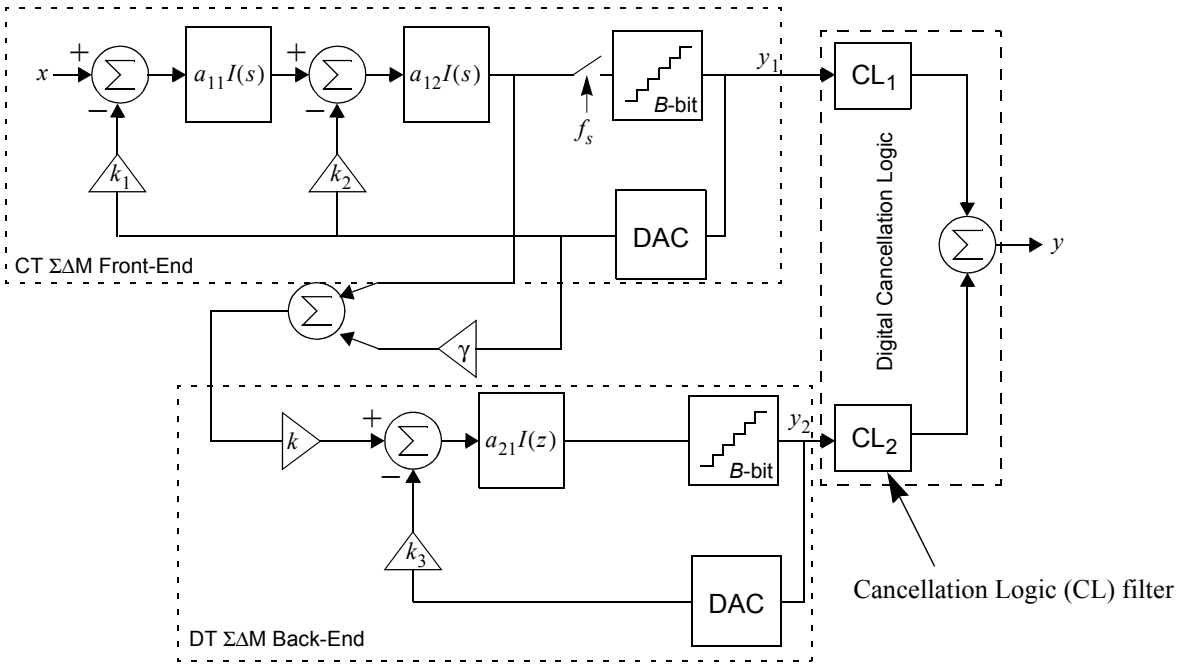


Figure 2. Cascade 2-1 H-ΣΔM proposed in [9].

3. PROPOSED MODULATOR ARCHITECTURES

Fig.3 shows the conceptual block diagram of a two-stage cascade resonation-based H-ΣΔM. The circuit nature of the different modulator blocks, either CT or DT, is highlighted in the figure. Note that the front-end stage is assumed to be implemented completely using CT circuits, instead of using mixed CT/DT circuits, whereas the rest of the modulator is implemented using DT, either analog or digital, circuits. This solution maximizes the anti-aliasing filtering, where minimizes the settling requirements and power consumption [9].

Conceptually speaking, the modulator in Fig.3 operates as a conventional two-stage cascade architecture. Both stage outputs are processed in the digital domain and combined by the Cancellation Logic Transfer Functions (CLTFs) so that ideally only the quantization error of the last stage remains, and it is shaped by a NTF whose order equals the sum of the respective orders of the two stages in the cascade.

The zeroes of NTF can be optimally distributed by including resonators in the modulator loop filters in order to minimize the in-band quantization noise power. In the case of a cascade modulator, there are two non-exclusive ways of implementing resonation: local [19] or global [20] resonation. The former is implemented by including resonators inside the loop filters of the different modulator stages (see Fig.3). Although both stages can theoretically implement local resonation, this is usually done only at the back-end stage in order to reduce the complexity of the CLTFs. Inter-stage global resonation is obtained by feeding back the quantization error from the back-end stage to the previous one. This is conceptually implemented by adding a FeedBack (FB) inter-stage mixed-signal path in the cascade as illustrated in Fig.3.

Fig.4 shows the proposed H-ΣΔM architectures, which are based on the conceptual scheme in Fig.3. All modulators are fourth-order 2-2 cascade topologies and include Unity STF (USTF) and multi-bit quantization in both stages[†††]. These strategies are combined with resonation to increase the effective resolution as compared to conventional cascade modulators. Fig. 2(a) uses DT local resonation at the second-stage. This is the simplest way to implement local resonation in a H-

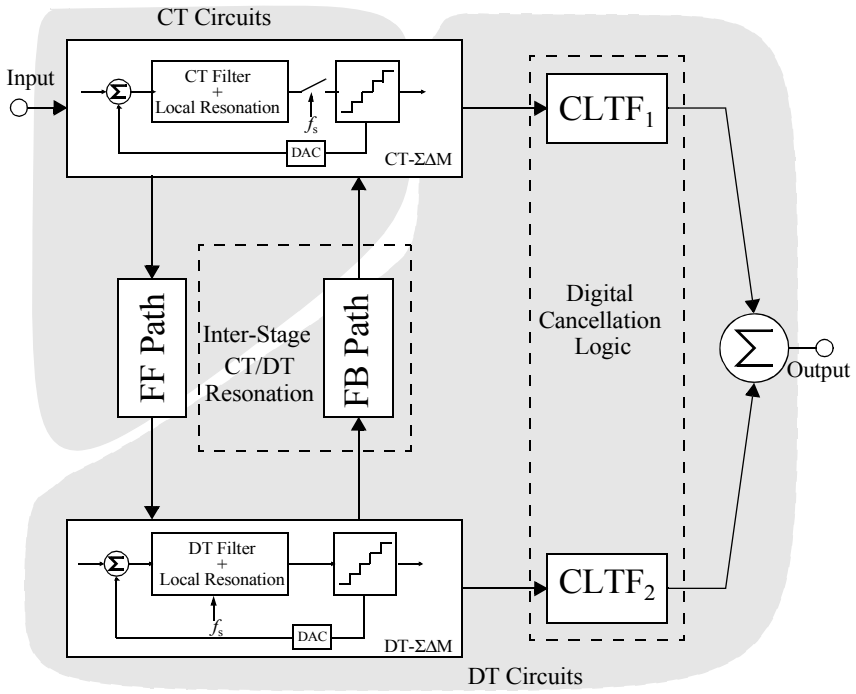
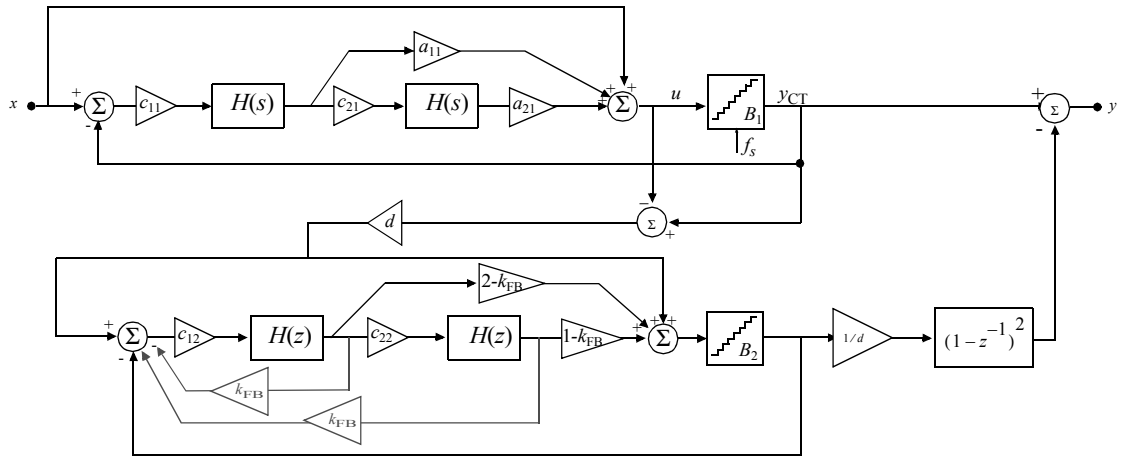
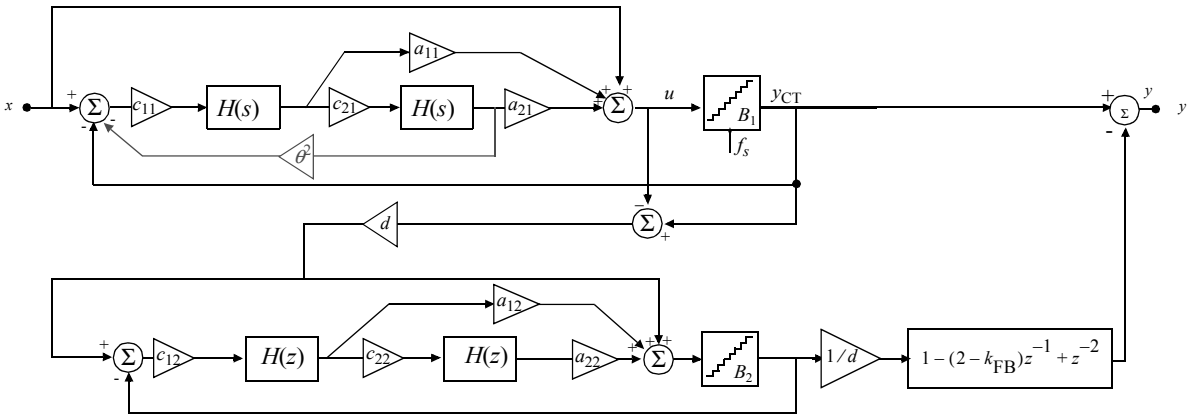


Figure 3. Conceptual block diagram of a cascade H-ΣΔM.

[†††] Practical implementations of Fig.4 should incorporate Dynamic Element Matching (DEM) algorithms as discussed earlier. Also, an extra DAC path between the output and the input of the front-end quantizer must be included to compensate for the excess loop delay Fig.4 [10]. These two blocks are not included in Fig.4 for the sake of simplicity.



(a)



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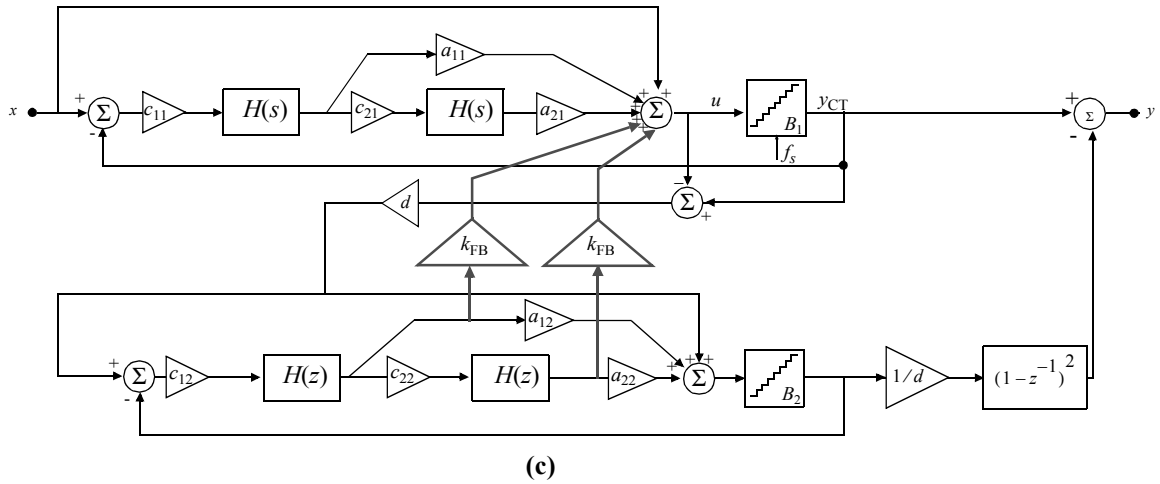


(c)

Figure 4. Proposed H-ΣΔMs. (a) DT Local Resonation (DTLR). (b) CT Local Resonation (CTLR). (b) CT/DT Global Resonation (CT/DT GR).

ΣΔM because the CLTFs are the same as that of a conventional cascade. In addition, the proposed topology uses only DT Forward-Euler (FE) integrators, with a transfer function $H(z) = z^{-1}/(1-z^{-1})$, instead of Backward-Euler (BE) or non-delayed integrators, as has been proposed in previous approaches[20]. This solution results in a more robust and simple electrical implementation. Resonation is achieved by adding two extra feedback paths, with gain, k_{FB}. This gain can be made programmable in order to adapt the modulator performance to different requirements in multi-mode multi-standard applications.

Resonation programmability can take advantage of the CT circuits in order to achieve a continuous tuning of the NTF zeroes within the required operation band. This can be done by placing the local resonation in the CT-ΣΔM front-end stage of the H-ΣΔM, as shown in Fig.4(b), where resonation coefficient, θ^2, can be continuously tuned in practice by using programmable transconductances. The main drawback of this modulator is that the resulting front-stage loop filter and the associated CLTFs are much more complicate and difficult to implement by practical circuits.

A good trade-off between circuit complexity and resonation programmability can be obtained by using the architecture in Fig.4(c). In this case, both the in-loop filters and CLTFs are the same as in a conventional cascade modulator, whereas includes global inter-stage mixed-signal CT/DT resonation, implemented by two feedback paths with gain, k_{FB}. Although no fully continuously programmable resonation is possible, this feedback path may benefit from the advantages of both CT and DT circuit techniques to achieve program ability, together with robustness with respect to circuit non-idealities.

All the architectures in Fig.4 have been synthesized using a DT-CT transformation method. Thus, starting from an fully DT-ΣΔM, a DT-to-CT transformation is applied to the CT part of the modulator in order to obtain the equivalent H-ΣΔM [14]. This DT-to-CT equivalence can be guaranteed because of the DT nature of the transfer function from the front-end quantizer output, y_{CT}, to the sampled quantizer input, $u(nT_s)$, defined as [10]:

$$LF(z) \equiv Z\left[\left.\frac{u(nT_s)}{y_{CT}(nT_s)}\right|_{x=0}\right] \tag{1}$$

where Z stands for the Z-transform, $T_s \equiv 1/f_s$ is the sampling time, with f_s being the sampling frequency.

Considering a Non-Return-to-Zero (NRZ) feedback DAC in the CT front-end modulator, and transforming $LF(z)$ from Z-domain to Laplace S-domain, the corresponding $LF(s)$ transfer functions are obtained. These functions are shown in Table 1 for the different modulators in Fig.4 together with the corresponding filter coefficients. Note that the resulting $LF(s)$ are linear combinations of the CT integrator transfer function, $H(s) = f_s/s$.

Assuming a linear model for the embedded quantizers, it can be shown that the NTF of the architectures in Fig.4 is given by:

$$NTF(z) = \frac{(1-z^{-1})^2[1-(2-K_{FB})z^{-1}+z^{-2}]}{d} \tag{2}$$

Table 1: LF Transfer functions and coefficients of the modulators in Fig.4

LF Transfer Function							
H-ΣΔM Topology	Z-Domain			S-Domain			
DT LR / GR	$LF(z) = -a_{11}c_{11}\frac{z^{-1}}{1-z^{-1}}\left(1+c_{21}\frac{z^{-1}}{1-z^{-1}}\right)$			$LF(s) = -\frac{c_{11}f_s}{s}\left[a_{11}-a_{21}c_{21}\left(\frac{1}{2}+\frac{f_s}{s}\right)\right]$			
CT LR	$LF(z) = \frac{z^{-2}-(2-k_{FB})z^{-1}}{1-(2-k_{FB})z^{-1}}$			$LF(s) = \frac{a_{11}f_s s - a_{21}f_s^2}{s^2+f_s^2\theta^2}$ $\begin{cases} a_{11} = \theta\frac{\cos(2\theta)-\cos(\theta)}{2\sin(\theta)[1-\cos(\theta)]} \\ a_{21} = \theta^2\frac{\sin(2\theta)-\sin(\theta)}{2\sin(\theta)[1-\cos(\theta)]} \\ \theta = \operatorname{acos}\left(1-\frac{k_{FB}}{2}\right) \end{cases}$			
Loop Filter Coefficients							
a_{11}	a_{12}	a_{21}	a_{22}	c_{11}	c_{12}	c_{21}	c_{22}
3/2	2	1	1	f_s	1	f_s	1

where d stands for the inter-stage gain. Note that two of the NTF zeroes are a function of the resonation coefficient, K_{FB}, whose value can be optimally chosen to maximize the *S*ignal-to-(*N*oise+*D*istortion) *R*atio (*SNDR*). On the contrary, K_{FB} can be chosen to maximize the digitized signal BandWidth, BW, for a given *SNDR* as detailed below.

4. APPLICATION TO RECONFIGURABLE DATA CONVERTERS

The two improvements given by resonation, i.e *SNDR* and BW increase, can be combined with proper digital programmability in order to adapt the performance of an H-ΣΔM based ADC to the requirements of the whole system in a multi-standard application.

Fig.5 (a) and (b) show the output spectra of the proposed modulators for different values of f_s and K_{FB}, considering $d = 1$ and multi-bit quantizers with $B_1 = B_2 = 4$. Fig.5(a) and Fig.5(b) illustrate the effect of local resonation, using DT and

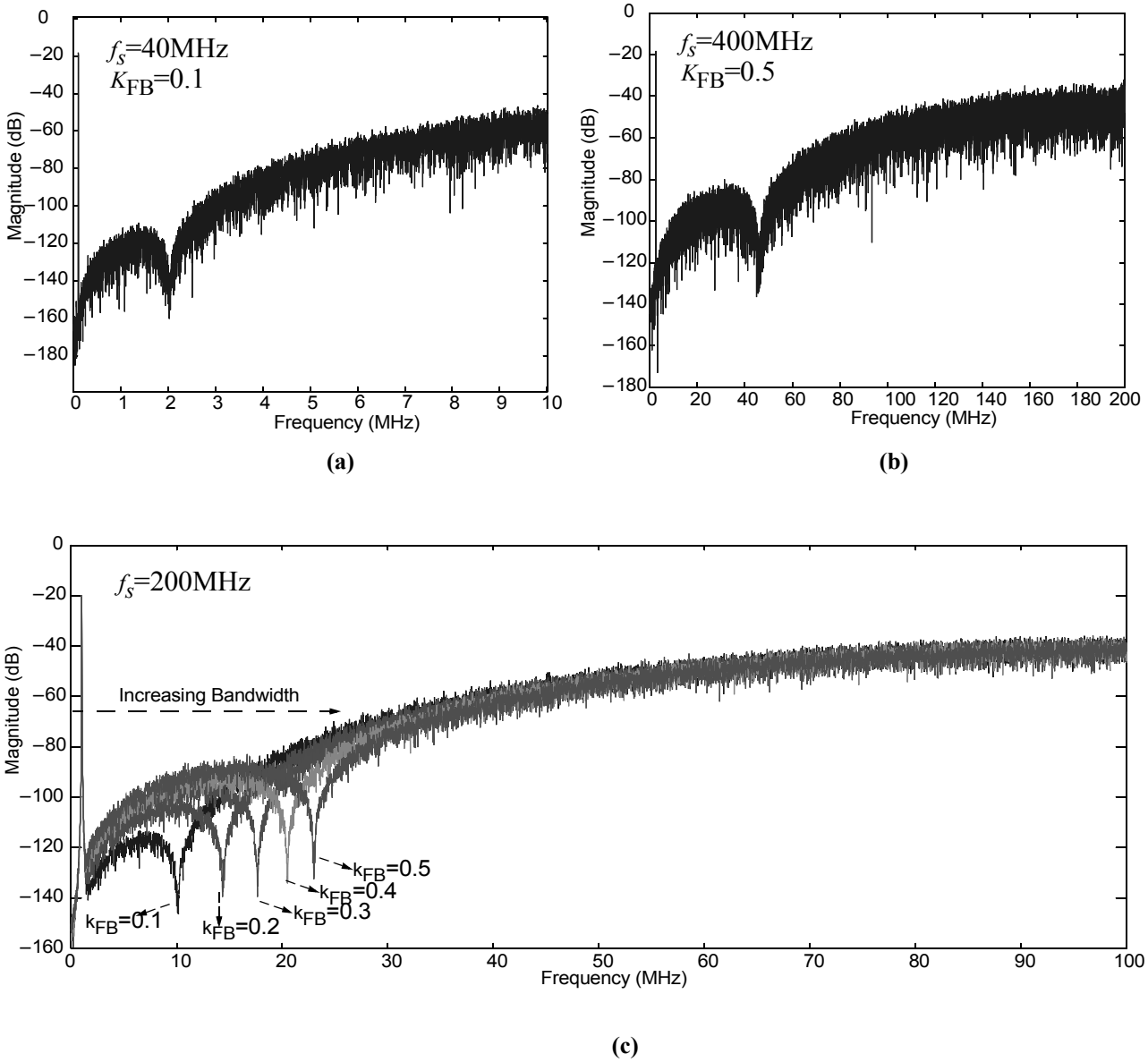
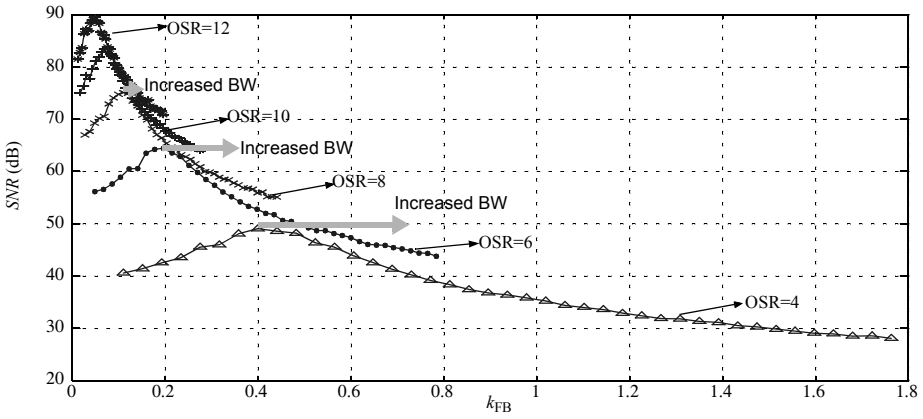


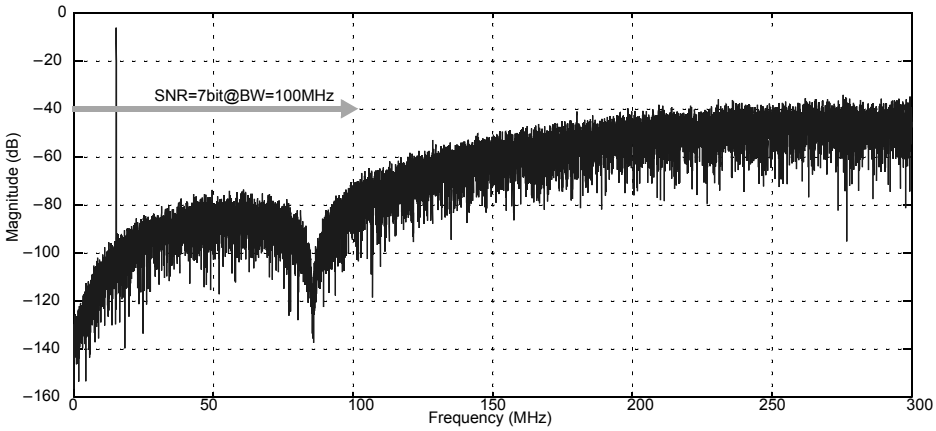
Figure 5. Output spectra of the proposed H-ΣΔMs. (a) DT LR with k_{FB}=0.1. (b) CT LR with k_{FB}=0.4. (c) GR with variable k_{FB}.

CT circuitry, respectively. The effect of varying the notch frequency with K_{FB} is illustrated in Fig.5(c), where several output spectra of the modulator with global resonation is shown. Note that, the signal bandwidth can be increased with K_{FB} at the price of reducing the effective resolution. This feature adds an additional ingredient to the basic design parameters of ΣΔMs, i.e OverSampling Ratio (OSR), modulator order, L, and internal quantization, $B_{1,2}$. All these parameters can be properly combined and digitally programmed to adapt the performance of H-ΣΔMs to different specifications.

Fig.6(a) shows the half-scale *Signal-to-Noise Ratio* (*SNR*) vs. k_{FB} for different values of OSR, corresponding to the GR H-ΣΔM, with $B_{1,2} = 4$, and $d = 1$. Note that, for each OSR case, there is an optimum value of k_{FB} that maximizes *SNR*. Above this value, the effect of resonation can be used to increase BW. This is highlighted in this figure, by showing the increment of BW corresponding to around 10-dB loss of resolution. Moreover, as OSR increases, the effect of resonation is less significant and the SNR graphs are sharper. Thus, in a multi-standard application, K_{FB}, OSR, L and $B_{1,2}$ need to be programmable in order to optimally adapt the performance of the H-ΣΔM to each operation mode. For instance, if the ADC needs to digitize a 100-kHz GSM signal with 14-bit effective resolution, this can be achieved just using the front-end stage (L=2) of Fig.4(c), with OSR=2, B_1=1,while the back-end stage can be kept switch off to save power. On the other hand, in broadband standards, the whole cascade (L=4) has to be used, with multi-bit ($B_{1,2}$=4) quantization. This is illustrated in Fig.6(b) by showing the output spectrum of Fig.4(c) with $K_{FB} = 0.75$, and $f_s = 600\text{MHz}$. The effective resolution is 7bit within a 100-MHz signal bandwidth. This sampling rate has been used in state-of-the-art CT-ΣΔMs [10], although it is very demanding for the DT back-end stage circuit. However, the circuit limitations of this stage has a lower impact on the performance of the whole modulator. Nevertheless, if f_s is reduced to 500MHz, the corresponding resolution reduces to 5-bit.



(a)



(b)

Figure 6. Effect of K_{FB} on the *SNR*. (a) *SNR* vs. K_{FB}. (b) Output Spectrum of the GR H-ΣΔM with f_s=600MHz and K_{FB}=0.75.

5. PRACTICAL IMPLEMENTATION AND EFFECT OF CIRCUIT ERRORS

The hybrid CT/DT nature of the proposed ΣΔMs requires using two different circuit techniques for their implementation. On the one hand, the CT front-end stage can be implemented either using RC-active or Gm-C integrators. The former present better linearity whereas the latter are more suited to operate at higher frequencies with less power consumption [10]. On the other hand, the DT back-end can be realized using either SC or Switched-Current (SI) circuits. Whereas the former are more robust and linear, the latter operate in current mode, thus simplifying the circuit implementation.

Fig.7 shows a Gm-C/SI conceptual implementation of the modulator in Fig.4(c), showing the values of transconductances. All transconductors can be tuned in order to keep the time constant C/g_m unchanged over C variations. The unitary transconductance, g_{mu} need to be tunable within 10 – 200μA/V in order to satisfy the requirements of the circuitry within the range of operation, 5-14bit@100kHz-100MHz. The modulator has been simulated using SIMSIDES, a time-domain behavioral simulator for ΣΔMs [21]. Main circuit errors have included in the models, namely: transconductance non-linear-

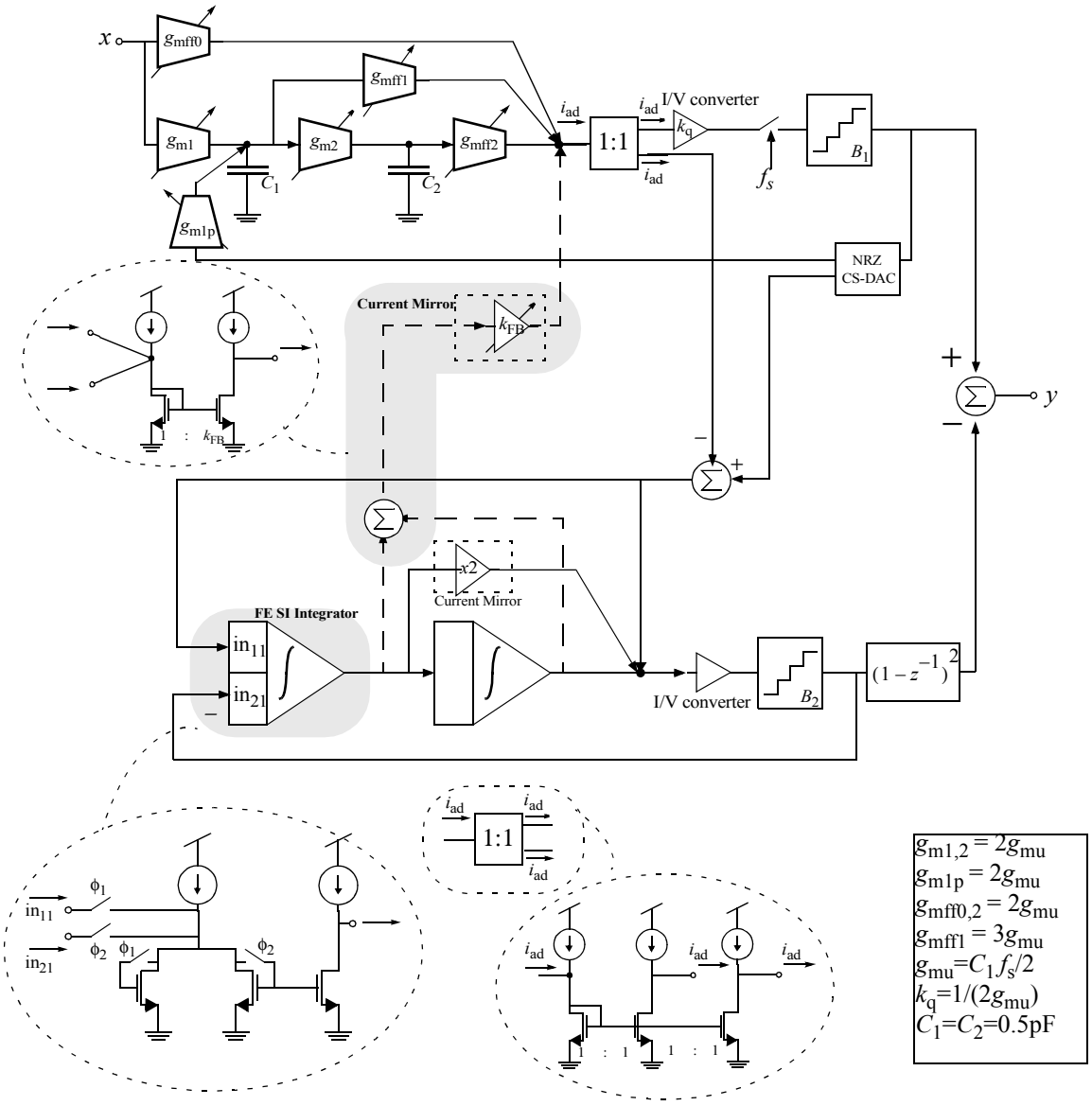
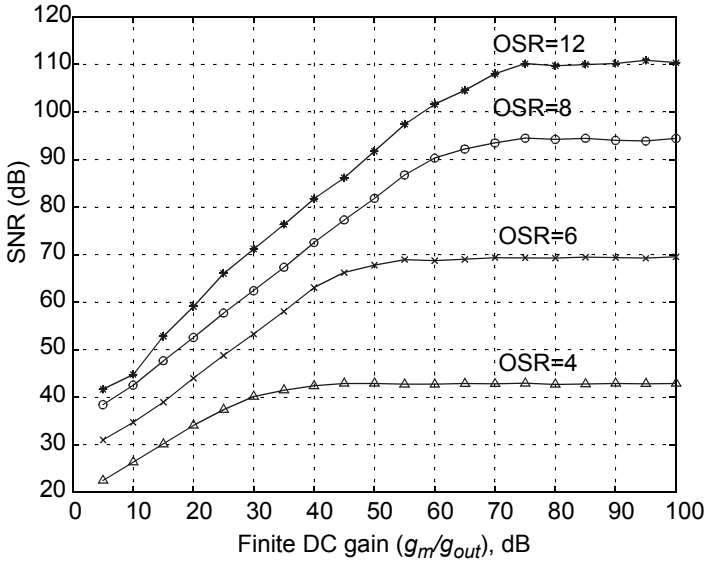


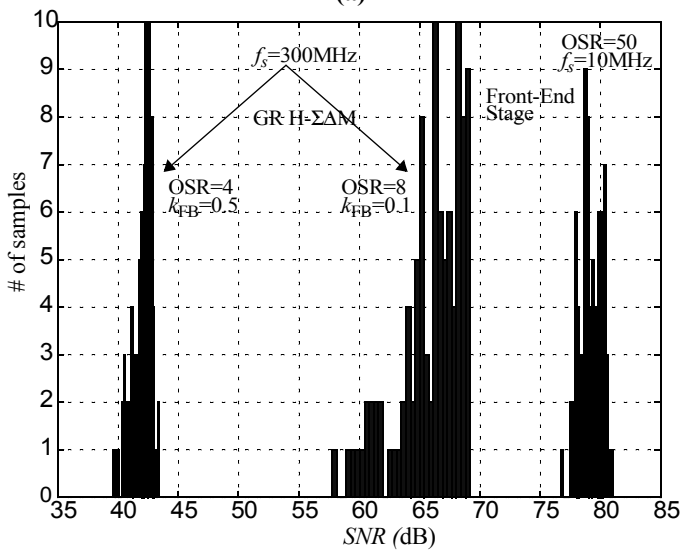
Figure 7. Gm-C/SI implementation of the GR H-ΣΔM in Fig.4(c).

ity, thermal noise, gain-bandwidth, parasitic input-output capacitances and finite DC gain. The effect of the latter is shown in Fig.8(a) for different values of the OSR, showing that realistic values of g_m/g_{out} are required for given specifications.

One of the most critical limiting factors in the proposed H-ΣΔMs are circuit tolerances and component mismatch. The first one can be controlled by proper tuning of time constants, but mismatch error still remains. In order to evaluate the impact of this mismatch, 100-sample MonteCarlo simulations of Fig.7 have been done, considering a standard deviation of 2% in the transconductances and SI integrator gains, and a 1% for the capacitors. Fig.8(b) shows the half-scale *SNR* obtained for different cases of OSR and K_{FB} . Note that the use of resonation introduces no appreciable degradation (3-4 dB around 40-dB medium *SNR*), for low oversampling ratios (OSR~4). However, as OSR is increased (and correspondingly the *SNR*), there is a higher degradation caused by resonation. Nevertheless, for medium-high resolutions (10-14 bit) and high oversampling ratios, the effect of resonation is not significant, as shown in Fig.6. In this case, the use of only the single-stage CT-ΣΔM – more robust against element tolerances – is more appropriate as illustrated in the histogram of Fig.8(b).



(a)



(b)

Figure 8. Effect of circuit errors. (a) Finite DC gain. (b) Mismatch.

CONCLUSIONS

Innovative hybrid CT/DT cascade ΣΔM architectures have been presented. They include either DT/CT local resonation or global resonation to optimally distribute the zeroes of NTF according to required specifications. This feature is combined with USTFs in all stages, implicit anti-aliasing filtering, reduced sampling requirements of the CT- front-end stage and reconfiguration of OSR, *L* and *B*. All these characteristics make the proposed modulators very suited for the implementation of fully digitally programmable ADCs intended for future software radios.

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