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Reducing the Impact of Reverse Currents in Tunnel FET Rectifiers for Energy Harvesting Applications

Juan Núñez and María J. Avedillo

***Abstract*—RF to DC passive rectifiers can benefit from the superior performance at low voltage of tunnel transistors. They have shown higher power conversion efficiency (*PCE*) at low input power than Si FinFETs counterparts. In this paper, we analyze the limitations of typical TFET rectifier topologies associated with the forward biasing of their intrinsic diode and show that this can occur at relatively weak input signals depending on the specific characteristic of the used tunnel device. We propose a simple modification in the implementation of the rectifiers to overcome this problem. The impact of our proposal is evaluated on the widely used gate cross-coupled topology. The proposed designs exhibit similar peak *PCE* and sensitivity but significantly improve PCE for larger input signal amplitude and larger input power.**

***Keywords*— Tunnel transistors, Steep subthreshold slope, Rectifiers, Reverse conduction, Energy harvesting.**

I. Introduction

The recent advent of Internet of Things (IoT) applications demands portable or remote devices powered by batteries or energy harvesters. CMOS technologies face power density and energy efficiency challenges and they are not able to scale supply voltages to achieve required ultra-low power operation for these applications. Emerging technologies, including emerging transistor devices, circuits, and architectures, provides the opportunity of further power scaling [1].

Tunnel field-effect transistors (TFETs) are one of the most attractive steep subthreshold slope (*SS*) devices currently being investigated as a means of overcoming such limitations of CMOS technology [2]-[4]. A smaller *SS* makes it possible to lower threshold voltage while keeping leakage current under control, facilitating low voltage operation. Many works have addressed the evaluation of these transistors for logic circuit applications, showing power benefits for iso-performance or higher performance at iso-power up to moderate operating frequencies, although opportunity also exists to provide benefits in higher performance domains in power or thermal limited applications [5]-[7]. More recently, other applications domains in addition to logic ones have been identified.

In particular, and relevant to the IoT application field, it has been shown that front-end circuits for energy harvesting can benefit from the superior performance of TFETs at low voltages [8],[9]. High sensitivity RF to DC passive rectifiers exhibiting much higher power conversion efficiency (*PCE*) al low input power than Si FinFETs counterparts (with exactly same topology) have been demonstrated [10]. TFET based rectifiers take advantage of the reduced turn-on voltage of these transistors with respect to Si FinFET to very much improve performance with weaker input signals. In addition, the higher I_{ON} current exhibited by TFETs at low supply voltages translates into a reduced on-state resistance which contributes to decrease resistive power losses improving *PCE*. Finally, according also to [10], unidirectional conduction of TFETs has a positive impact on *PCE* through reduced reverse losses. Reverse losses are associated to the symmetric conduction of conventional transistors which conduct under both positive and negative drain to source voltages. However, although *P* (*N*) TFETs do not conduct under low positive (negative) drain to source voltages, enough high reversed drain to source voltages produce the forward biasing of their intrinsic *p-i-n* diode which translates in large losses currents. That is, the advantage associated to unidirectional conduction is limited to enough low amplitude input signals (or enough low input power).

In this paper, we analyze in depth the operation limits of TFETs based rectifiers with respect to voltage levels of input signals and input power, and propose tuning the rectifier topology to the specific TFET characteristic to better control reverse currents and thus, extend the voltage/power operation range of TFETs based rectifiers.

The rest of the paper is structured as follows. Section II analyzes a simple 2-transistor (2-T) rectifier topology to illustrate the limitations of TFET rectifiers associated to the forward biasing of the *p-i-n* diode in the TFET devices and introduces the rationale of the proposed modification. Section III evaluates, by means of simulation results, our solution when applied to the more complex and widely used gate cross-coupled topology. Finally, some conclusions are given in Section IV.

II. Analysis of TFET based rectifier operation

Fig 1 depicts the well-known 2-T passive rectifier [11]. There are two regions of operation. In region *I*, P_1 transistor is on, while N_1 is off. Current is flowing through P_1 to supply current to the output load. Ideally no current flows through N_1. In region *II*, P_1 is off and N_1 is on. Current flows through N_1 to supply V_X. Ideally no current flows through P_1. In the stationary state, a DC output voltage is produced ($V_{DC,OUT}$).

Fig 2 compares $V_{DC,OUT}$ and output power (PWR_{OUT}) versus amplitude of input signal (V_{AC}) obtained for a Si FinFET and a TFET rectifier. The TFET is a 20nm GaN/InN single gate TFET [12]. Models have been obtained from the nanoHUB website. A predictive 20nm FinFET transistors for HP obtained from the PTM web page is used [13]. The TFET rectifier sizing is similar to that in [10]. Also, the values used for C_C (100*fF*), C_L (100*fF*) and R_L (1MΩ) have been taken from that reference. The FinFET transistors have

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been sized identical to the TFET ones. The frequency of the RF input signal is the standard 915MHz.

Advantages for low input amplitudes are evident in Fig 2 in agreement with previous works. It can be observed that, unlike the FinFET, increasing V_{AC} above 0.3V produces a decrement in both the output voltage and the output power. *PCE* (PWR_{OUT} / PWR_{IN}) sharply reduces over this voltage value because decreasing output power occurs for increasing input power (producing a larger amplitude RF signal). This behaviour can be explained on the basis of the *I-V* characteristic of TFET transistor. Fig 3a depicts the I_{DS}-V_{DS} curves for the used NTFET for different V_{GS} values (both positive and negative). Under enough negative V_{DS}, the forward biased *p-i-n* diode of the TFET conducts a large current. Fig 3b shows currents through P_1 for V_{AC}=0.4V and V_{AC}=0.6V for the TFET rectifier. Direct ($I_{P\text{-}TFET}$>0) and reverse ($I_{P\text{-}TFET}$<0) currents are larger at V_{AC} =0.6V than at V_{AC}=0.4V. However, note the larger increment in reverse current with respect to direct one, due to the forward biasing of the diode, leading to the degradation of the rectifier

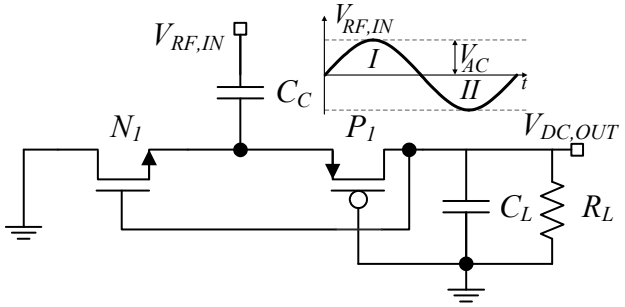

Fig 1. Schematic of the 2 transistor passive rectifier proposed in [11].

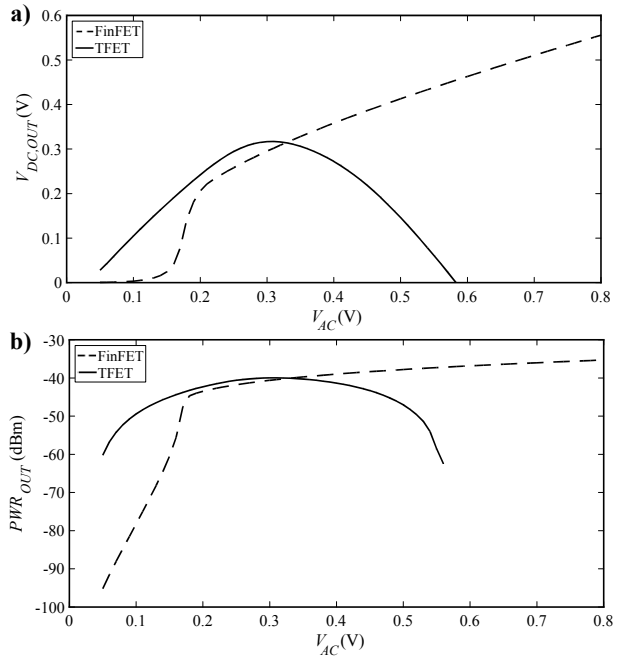

Fig 2. FinFET/TFET 2-T rectifier. (a) $V_{DC,OUT}$ vs. V_{AC}. (b) PWR_{OUT} vs. V_{AC}.

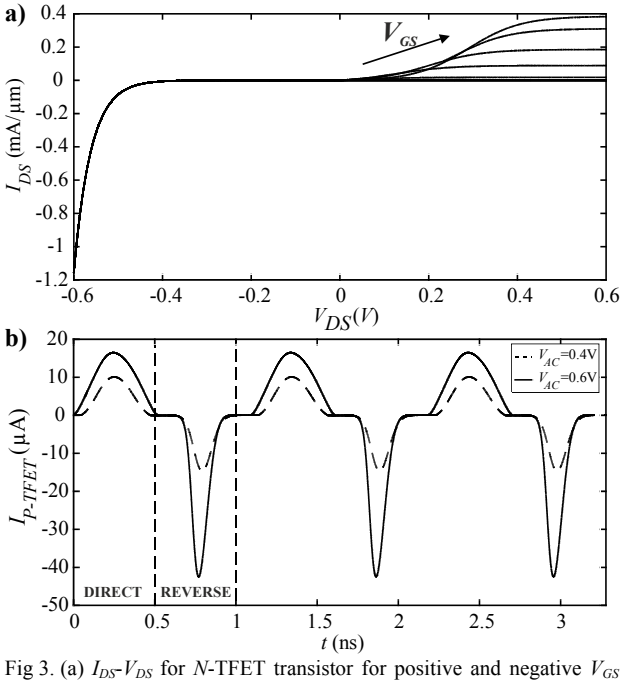

Fig 3. (a) I_{DS}-V_{DS} for *N*-TFET transistor for positive and negative V_{GS} values. (b) Current through P_1 in 2-T rectifier for two V_{AC} values.

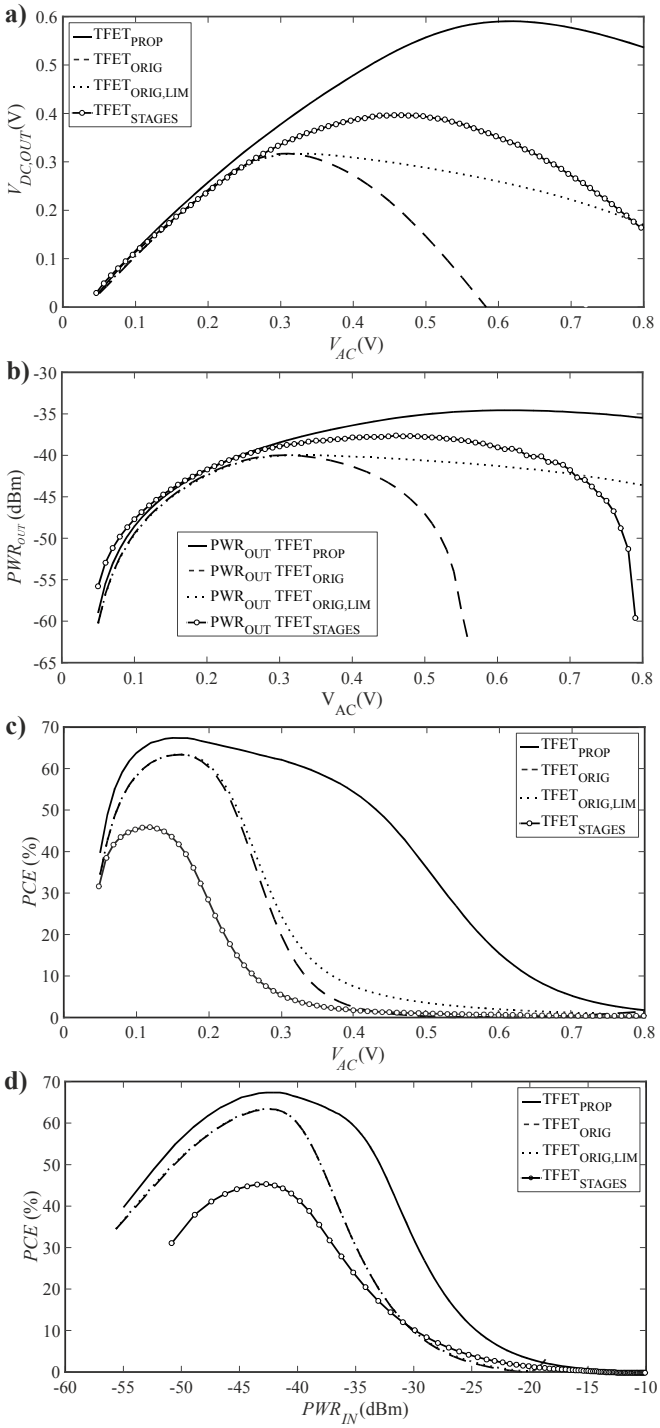

Fig 4. 2-T rectifier performance. (a) $V_{DC,OUT}$ vs. V_{AC}. (b) PWR_{OUT} vs. V_{AC}. (c) *PCE* vs. V_{AC}. (d) *PCE* vs. PWR_{IN}.

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operation. This behaviour is occurring at an input power around -33dBm. That is, in the sub-micro watt range of applications for which TFET rectifiers have been proposed.

In order to overcome this limitation, it is required that transistors are not operated with reversed drain to source bias above the diode´s on voltage. This can be achieved if each transistor in the original topology is implemented by the series connection of two transistors. Fig 4 shows output voltage (*a*) and power (*b*) versus V_{AC} and *PCE* against both V_{AC} and PWR_{IN} when this solution is adopted ($TFET_{PROP}$). It can be observed that the unwanted behaviour has been shifted to much larger V_{AC} and PWR_{IN} values in the TFET proposed design, improving the *PCE* performance at larger input voltages or input power. Fig 4 also depicts results for a 2-stage rectifier. Multiple-stages rectifiers are usually employed to obtain higher $V_{DC,OUT}$, thus they could be also considered potential candidates to solve the voltage drop phenomenon. A two-stage rectifier in which each stage is sized as the $TFET_{ORIG}$ achieves larger $V_{DC,OUT}$ than any of the alternatives shown in Fig 4a up to V_{AC}=0.3V ($V_{DC,OUT}$ =570mV at V_{AC}=0.3V). However, over this value of input amplitude, it exhibits same behaviour than $TFET_{ORIG}$, and $V_{DC,OUT}$ sharply falls down, since intrinsic diodes are also forward biased as it occurs in the $TFET_{ORIG}$. An alternative sizing of two stage rectifiers to mitigate the problem has been investigated. We have been able to somehow alleviate the problem ($TFET_{STAGES}$). The decrement in output voltage and output power is also evident in this solution, although it shifts to higher input voltages in comparison to $TFET_{ORIG}$.

The voltage drop could be also mitigated by limiting the reverse current. Observe the $TFET_{ORIG,LIM}$ curve obtained in Fig 4a. This solution is based on limiting V_X by decreasing the ratio C_C / C_T, with C_T the total transistor capacitance. However, when limiting reverse currents, also direct currents are limited and, thus, small *PCE* improvement is achieved as shown in Fig 4c and Fig 4d.

In [14] a TFET rectifier topology to better control reverse currents is proposed. It is based in forcing the gate to source voltage of the transistors to zero and it has shown to improve *PCE*. Note that the unwanted diode current is independent on V_{GS}, thus the topology in [14] can still suffer the limitation analysed in this paper. The maximum allowed V_{AC} (or input power) before it is triggered depends on the specific device. That is, the proposed topology in this paper and the technique in [14] to control V_{GS} address different targets. *PCE* data shown in Fig 4 could additionally benefit from the application of the V_{GS} control technique although it is not relevant for the evaluation of the impact of our proposal to avoid the forward biasing of the intrinsic diode.

III. Evaluation of Proposed Modification

TFET rectifiers based on the gate cross-coupled topology ($TFET_{ORIG}$) depicted in Fig 5a [15] have also shown higher efficiency than those using the two-transistor topology like it occurs in CMOS technologies [10]. The proposed modification ($TFET_{PROP}$, in Fig 5b) is evaluated for this type of rectifier. Designs for R_L=1MΩ and R_L=100KΩ have been carried out. In the first case, transistors are sized as in the 2-T design. Results are shown in Fig 6a ($V_{DC,\,OUT}$ versus V_{AC}) and Fig 6b (*PCE* versus PWR_{IN}). It can be observed that the limitation identified and analysed in previous section is also exhibited. Note that V_{AC} is now the amplitude of the difference signal $V_{RF,IN}^{+}$ - $V_{RF,IN}^{-}$. That is, it is

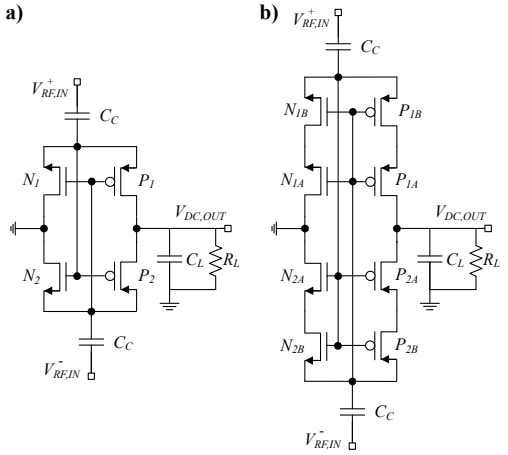

Fig 5. (a) Schematic of the gate cross-coupled rectifier reported in [15]. (b) Schematic of the proposed modification of the gate cross-coupled rectifier.

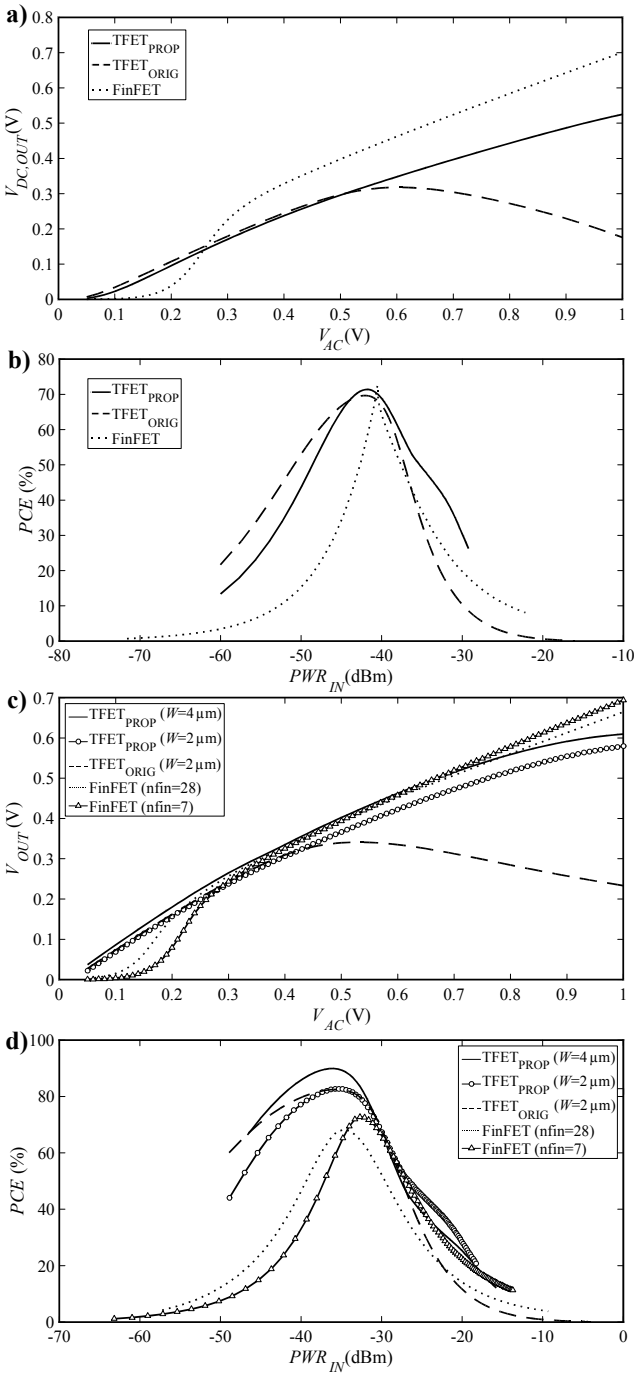

Fig 6. Gate cross coupled rectifier performance for R_L=1MΩ (a,b) and R_L=100KΩ (c,d).

different from the V_{AC} in Section II. This explains why the $V_{DC,OUT}$ drops observed for the $TFET_{ORIG}$ design are now shifted (towards larger V_{AC} values) with respect to the 2-T topology. Fig 6b clearly shows the advantages in *PCE* of the proposed design for large input signal amplitudes and input power.

Fig 6c and Fig 6d shows *PCE* results for R_L=100KΩ. Larger transistor sizes have now been used to optimize the peak *PCE* of the original design (W=2μm). Two different sizing of the proposed topologies have been evaluated. First, transistors have been sized to obtain a similar peak PCE to the original design (W=2μm). Second, the width of the transistors have been multiply by two since two transistors are connected in series (W=4μm). Both designs exhibit similar sensitivity but improve *PCE* for larger input signal amplitude and larger input power. The latter design in addition improves also *PCE* for low input power. For comparison purpose, FinFET rectifiers have been also included. Their performance with the number of fingers has been analysed. Results for two designs are shown. The one optimizing peak *PCE* (7 fingers) and another one sized similar to the original one (28 fingers). It can be clearly observed the advantages of the tunnel based rectifiers for low input power in agreement with previous works. In addition, the proposed rectifier also exhibits advantages with respect to the FinFET designs for larger input power.

IV. Conclusions

Using serial connected transistors in the implementation of the typical rectifier topologies avoids the degradation of their performance produced by the forward biasing of the *p-i-n* diodes. For the projected tunnel technology we use in this analysis, the above undesired behavior occurs at low input signal amplitudes, thus, it should be taken into account even for applications in the range of micro watts.

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