Insights into the Operation of Hyper-FET based Circuits

María J. Avedillo and Juan Núñez

***Abstract*— Devices combining transistors and phase transition materials are being investigated to obtain steep switching and a boost in the I_{ON}/I_{OFF} ratio and, thus, to solve power and energy limitations of CMOS technologies. This paper analyzes the operation of circuits built with these devices. In particular, we use a recently projected device called Hyper-FET to simulate different circuits, and to analyze the impact of the degraded DC output voltage levels of Hyper-FET logic gates on their circuit operation. Experiments have been carried out to evaluate power of these circuits and to compare with counterpart circuits using FinFETs. The estimated power advantages from device level analysis are also compared with the results of circuit level measurements. We show that these estimations can reduce, cancel, or even lead to power penalties in low switching and/or low frequency circuits. We also discuss relationships with some device level parameters showing that circuit level considerations should be taken into account for device design.**

***Keywords*—Steep subthreshold slope, Phase transition materials, Low power, Low voltage, Energy efficiency.**

I. Introduction

The recent advent of Internet of Things (IoT) applications demands portable or remote devices powered by batteries or energy harvesters. CMOS technologies face power density and energy efficiency challenges and they are not able to scale supply voltages to achieve required ultra-low power operation for these applications. Emerging technologies, including emerging transistor devices, circuits and architectures, provides the opportunity of further power scaling.

Steep subthreshold slope (*SS*) devices are currently being investigated as a means of overcoming such limitations of CMOS technologies. A smaller *SS* makes it possible to lower threshold voltage while keeping leakage current under control, facilitating low voltage operation. Several steep slope devices, based on very different physical mechanisms, have been reported as promising candidates to achieve these features. Tunnel FETs are reverse biased, gated p-i-n tunnel diode with asymmetrical source/drain doping. Current is controlled by the gate-voltage induced band-to-band tunneling at the source-channel junction, which enables the tunneling window in the energy bands [1]-[4]. Steep subthreshold slope can be also achieved by exploiting the negative capacitance exhibited by ferroelectric materials. They can be stacked into the gate insulator of a MOSFET transistor to obtain a negative capacitance FET (NCFET) [5]-[8]. A two-dimensional electrostrictive field effect transistor (2D-EFET), which operation is also based on an internal voltage amplification enabled by using a electrostrictive material as gate oxide, has been also proposed [9].

Alternatively to the development of novel transistors, recently, Hybrid-phase-transition FETs (Hyper-FETs) have been proposed by connecting a phase transition material (PTM) to the source terminal of a FET. The abrupt insulator-metal transitions of the PTM are used as a mechanism to obtain steep switching and a boost in the I_{ON}/I_{OFF} [10]. Hence, compared to conventional FET-based designs, power and energy advantages at iso-delay could be obtained. Significant static power/energy savings can be achieved if PTMs are combined with conventional FETs to reduce their leakage current without significant on currents reduction. Also, power/energy reductions can be achieved if leakage current of the Hyper-FET is matched to that of the conventional FET. In this case, the Hyper-FET exhibits higher ON current than the FET and iso-delay operation can be achieved with lower supply voltages.

Up to our knowledge, several Hyper-FETs have been experimentally obtained exhibiting *SS* around 8mV/dec [10], 5mV/dec [11] and 59mV/dec [12]. In [13], a phase-change Tunnel FET with *SS*=30mV/dec has been recently proposed. In addition to reducing power consumption in conventional logic computation, Hyper-FETs are considered as potential candidates to enable new computational paradigms such as neuromorphic architectures or non-Boolean processing [14].

Two recent publications have analyzed the operation of the Hyper-FET [15], [16]. In particular, it is shown in [16] that Hyper-FET logic gates exhibit degraded DC output voltages (different from V_{DD} and zero). This characteristic is not exhibited by the others steep slope devices mentioned and requires further analysis. In this paper, the impact of these non-ideal voltage levels when interconnecting gates is analyzed. We show that gates within a logic network could deviate from their desired behavior leading to power performance degradation. We study the impact of the addition of a PTM to FinFETs in terms of I_{OFF}. This contrasts with [15], [16], in which circuit performance is compared between FinFETs and Hyper-FETs at iso-I_{OFF}.

This paper is organized as follows: in Section II, the Hyper-FET and its operation principle are introduced. Critical relationships between device parameters of its PTM and its transistor to ensure correct operation of the Hyper-FET, both at device and gate level are described. Section III analyzes the operation of circuits designed using Hyper-FETs. Situations in which the logic gates deviate from the desired behavior are illustrated. In Section IV, the impact of such deviation in terms of power is evaluated. Section V describes a case study in which this evaluation is extended to a more complex circuit. Finally, key conclusions are provided in Section VI.

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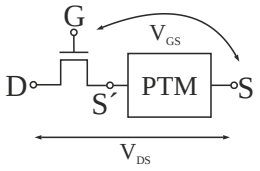

Fig 1. Schematic of the Hyper-FET.

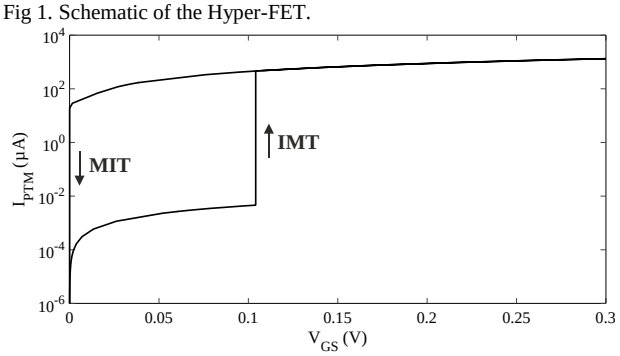

Fig 2. I-V curve of the PTM device.

II. BACKGROUND

As already mentioned in previous section, two recent publications have analysed the operation of the Hyper-FET both at device [15] (hereinafter Part I) and gate [16] (hereinafter Part II) levels. Part I describes requirements of the PTM to operate together with its host transistor in order to achieve optimized performance of the Hyper-FET. In Part II, circuit level analysis for Hyper-FETs is presented and PTM requirements for correct gate operation are established. The content of this section is based on those works.

A Hyper-FET integrates a phase-transition material (PTM) into the source terminal of a conventional transistor (Fig 1). PTMs undergo insulator-metal transitions under given electrical, thermal, or optical stimuli attributed to different physical mechanisms in different materials (electron–electron correlation, filamentary ion diffusion, and dimerization). That is, they experiment abrupt switchings from/to a high resistivity state (insulating phase) to/from a low resistivity state (metallic phase). Hyper-FETs use current-driven PTMs to achieve steep switching. Table I summarizes characteristic parameters of this type of PTMs. They are characterized by means of material, as well as geometrical parameters.

TABLE I PTM CHARACTERISTIC PARAMETERS.

Parameter	Parameter description	PTM-Sim
	Material	
ρ_{INS}	Resistivity of the insulating state	100 Ω·cm
ρ_{MET}	Resistivity of the metallic state	10^{-3} Ω·cm
$J_{C\text{-}IMT}$	Current density which triggers the insulator to metal transition (IMT)	$5.2\cdot10^2$A/cm^2
$J_{C\text{-}MIT}$	Current density which triggers the metal to insulator transition (MIT)	$8\cdot10^3$ A/cm^2
	Geometrical	
L	Length	20 nm
A	Area	$42\cdot21$ nm^2
	Electrical	
Parameter	**Parameter description**	
R_{INS}	Resistance of the PTM device in the insulating state	
R_{MET}	Resistance of the PTM device in the metallic state	
$V_{C\text{-}IMT}$	Voltage at which IMT occurs	
$V_{C\text{-}MIT}$	Voltage at which MIT occurs	
TT	Transition Time	
C_{PTM}	Intrinsic capacitance	

PTMs tend to stabilize in the insulating phase under no electrical stimuli. When a high enough current density ($J_{C\text{-}IMT}$) flows through it, Insulator to Metal Transition (IMT) occurs. Once in the metallic state, when the current density reduces below $J_{C\text{-}MIT}$, the Metal to Insulator Transition (MIT) takes place. PTM-Sim, used in Part I and Part II, is characterized in third column of Table I. Fig 2 depicts its I-V curve. It has been obtained with a Verilog-A model inspired in the macro-model proposed in Part I. It agrees well with the I-V curve shown in that paper. Electrical parameters used in the model are also shown in Table I. R_{INS}, R_{MET}, $V_{C\text{-}IMT}$ and $V_{C\text{-}MIT}$ have been calculated from the material and geometrical properties of PTM-Sim. In addition, MIT and IMT are abrupt but no instantaneous. Thus a transition time (TT) is also considered in that macro-model to take this into account. The value reported in Part I (50ps) has been used. Also, a parallel parasitic capacitance of 1fF has been also included, according to Part I.

The Hyper-FET transistor takes advantage of the orders of magnitude difference between R_{INS} and R_{MET} to boost the ratio of its ON current (I_{ON}) and its OFF current (I_{OFF}) achieving steep subthreshold slope. When the transistor is in the OFF state, the small current flowing through the Hyper-

TABLE II PTM CONSTRAINTS FOR CORRECT DEVICE AND GATE LEVEL OPERATION.

Constraint	Constraint description
Device (Part I)	
$\rho_{INS}/\rho_{MET}\,(PTM) > I_{ON}/I_{OFF}$ (transistor)	Necessary but not sufficient condition to achieve I_{ON}/I_{OFF} boost
$R_{INS}\,(PTM) \sim R_{OFF}$ (transistor)	If R_{INS} (ρ_{INS}) too high, it could not be driven by gate voltage Higher R_{INS} (ρ_{INS}) reduces I_{OFF}
$R_{MET}\,(PTM) << R_{ON}$ (transistor)	Avoids I_{ON} degradation with respect to intrinsic transistor
$I_{C\text{-}MIT,MIN} < A\cdot J_{C\text{-}MIT} < I_{C\text{-}MIT,MAX}$	Guarantees Hyper-FET can undergo MIT during normal operation $I_{C\text{-}MIT,MIN}$: Current flowing through the transistor in series with R_{MET} @ $V_{DS}=V_{DD}$ and $V_{GS}=0$ $I_{C\text{-}MIT,MAX}$: Current flowing through the transistor in series with R_{MET} @ $V_{DS}=V_{DD}$ and $V_{GS}= V_{DD}$
$I_{C\text{-}IMT,MIN} < A\cdot J_{C\text{-}IMT} < I_{C\text{-}IMT,MAX}$	Guarantees Hyper-FET can undergo IMT during normal operation $I_{C\text{-}IMT,MIN}$: Current flowing through the transistor in series with R_{INS} @ $V_{DS}=V_{DD}$ and $V_{GS}=0$ $I_{C\text{-}IMT,MAX}$: Current flowing through the transistor in series with R_{INS} @ $V_{DS}=V_{DD}$ and $V_{GS}= V_{DD}$
$V_{GS,IMT} > V_{GS,MIT}$	Hysteresis must be positive $V_{GS\text{-}IMT}$: Gate to source voltage required to trigger IMT in the Hyper-FET. $V_{GS\text{-}MIT}$: Gate to source voltage required to trigger MIT in the Hyper-FET
Inverter (Part II)	
$V_{GS,IMT} < V_{DD}/2$ @ $V_{DS}=V_{DD}/2$ $V_{GS,MIT} < V_{DD}/2$ @ $V_{DS}=V_{DD}/2$	Inverter with gain > 1
$R_{INS}\,(PTM) < R_{OFF}$ (transistor)	$V_{OH,MIN} > V_{DD}/2$ $V_{OL,MAX} < V_{DD}/2$
$V_{DS,MIT} < 1$mV	Rail to rail swing
$C_{PTM} << C_{Load}$	Avoids charge sharing
TT << intrinsic delay of transistor	Speed considerations

FET forces the PTM in the insulating state. Thus, the effective gate-to-source and drain-to-source voltages seen by the intrinsic transistor are reduced and I_{OFF} is also decreased. When the gate to drain voltage is increased, current through the Hyper-FET is also increased and the switch to the metallic state is triggered. Because of the small metallic resistance, the I_{ON} current of the Hyper-FET is almost not reduced with respect to the intrinsic transistors. Thus, I_{ON}/I_{OFF} is increased. Hyper-FET exhibits power and energy advantages on the basis of the I_{OFF} reduction. In applications for which static power dominates, the PTM is combined with conventional FETs to reduce leakage currents. However, Hyper-FETs can be also advantageous in other application domains. A Hyper-FET with same I_{OFF} than a given transistor could be obtained combining a PTM with a modified transistor exhibiting both larger OFF and ON currents than a conventional FET. Because of the higher I_{ON}, the Hyper-FET can be operated at reduced supply voltage without degrading speed, which translates in power and energy savings, with similar leakage currents than a conventional FET.

In order to achieve the operation principle described above for the Hyper-FET and the boost in the current ratio, proper tuning of the PTM and the intrinsic transistor is critical. At this respect, since many materials exhibit this type of phase transitions with a wide range of resistivity, and active research on techniques to control their properties is going on, it is expected that PTMs can be optimized to suitable fit the transistor (Part I). It has been stated that several constraints must be satisfied by the PTM. Some of these constraints guarantee operation at the device level (Part I) while others are required by logic gates to operate properly (Part II). Table II summarizes these constraints.

Concerning constraints derived from the inverter analysis, the two first one are derived from the analysis of its DC operation. The transfer characteristic of the Hyper-FET inverter very much differs from that of a conventional one. Both PTMs are in the metallic state in the transition region (gain > 1) and in the insulating state in the non-transition regions. Thus, output voltages in the non-transition regions are determined by the relationship between (R_{INS} + R_{ON}(transistor)) and (R_{INS} + R_{OFF}(transistor)). In the conventional inverter, they are determined instead by the relationship between R_{ON} and R_{OFF} of the transistors. Thus, output voltages below V_{DD} are obtained in the Hyper-FET inverter for small input voltages (in particular for V_{IN}=0V). Similarly, output voltages over 0V are obtained in the Hyper-FET inverter for large input voltages (in particular for V_{IN}= V_{DD}). This motivates that the resistance of the PTM in the insulting state is further constrained (shaded in Part II of Table II) from the limit derived during the device operation analysis (shaded in Part I of Table II). However, the analysis at the gate level does not take into account the impact of the degraded output voltages on the operation of Hyper-FET based circuits. This analysis is carried out in the next section.

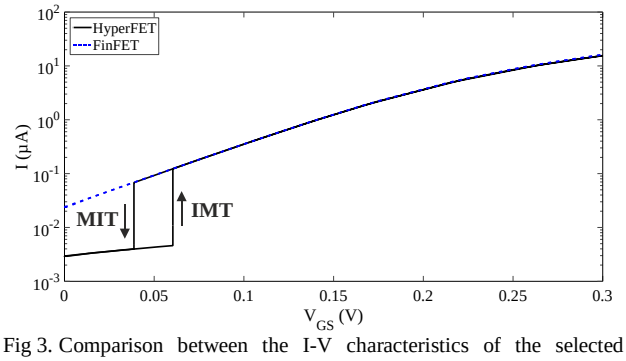

Fig 3. Comparison between the I-V characteristics of the selected FinFET and Hyper-FET.

III. Analysis of the Operation of Hyper-FETs Circuits

In order to analyse the operation of Hyper-FET based circuits, we use the recently projected device (PartI, PartII). We combine the PTM-Sim described in previous Section with predictive 14nm FinFET HP transistors [17]. The sizing of the FinFETs in Part I (2 fingers) has been also used. It has been verified that this Hyper-FET device satisfies the complete set of constraints introduced in previous section for V_{DD}=0.3V. Fig 3 shows the transfer characteristic obtained for this Hyper-FET with V_{DS}=0.3V. The positive hysteresis is clearly observed. The characteristic of the host FinFET transistor is also shown for comparison purpose. As expected, the I_{OFF} (2.9nA) of the Hyper-FET is lower than the I_{OFF} (24nA) of the FinFET (around one order of magnitude smaller), while the I_{ON} is only slightly degraded (16.2µA for the transistor and 15.5µA for the Hyper-FET). That is, the I_{ON} /I_{OFF} ratio of the HyperFET is multiplied by 8 with respect to the intrinsic FinFET. It might be also interesting to compare to other steep slope devices. For that, we have evaluated the I_{ON} /I_{OFF} ratio (at V_{DD} = 0.3V) of five different projected TFETs which models are available from nanoHUB. Four of them

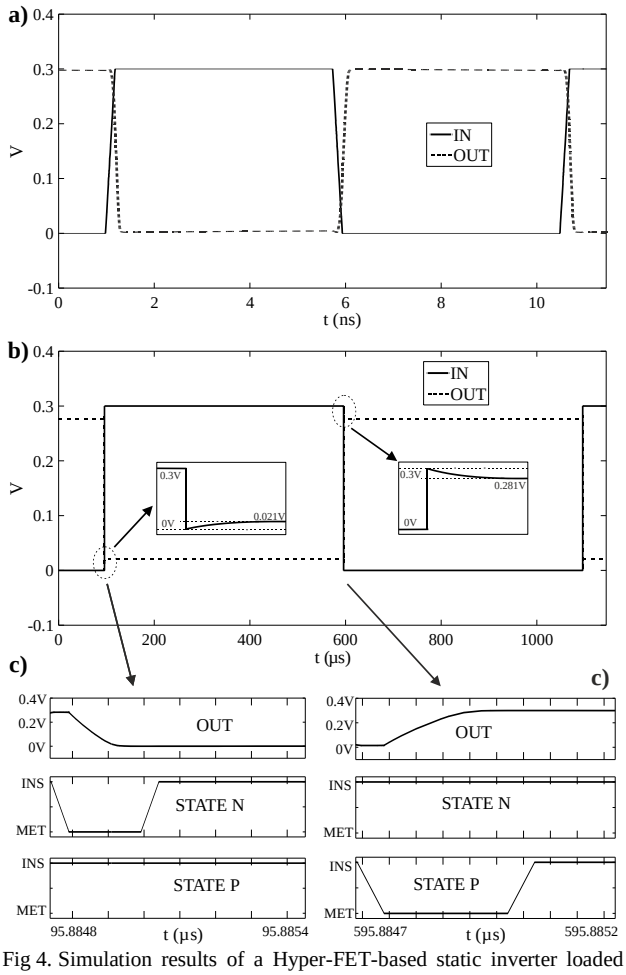

Fig 4. Simulation results of a Hyper-FET-based static inverter loaded with 5fF. Square input signals of (a) 100MHz and (b) 1KHz have been considered. (c) Insights of (b) for the falling and rising edges of the output, including states of the PTMs of the *N*-type and *P*-type Hyper-FETs.

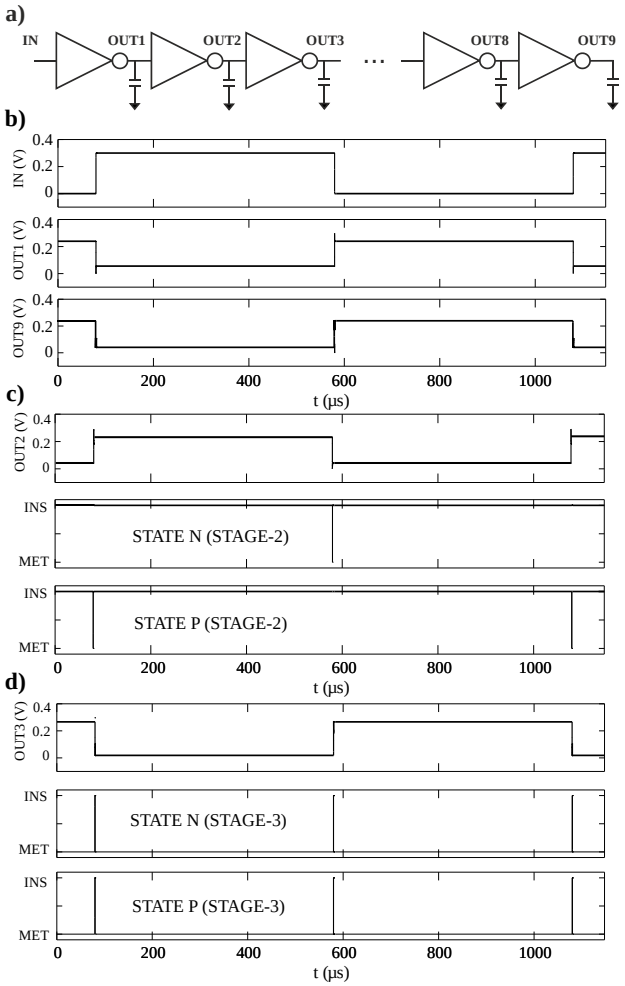

Fig 5. Simulation results for the chain of nine Hyper-FET-based static inverters depicted in (a). (b) Waveforms for the input and the output of stages 1 and 9. Output and states of the second (c) and third (d) stages.

exhibit ratios between 2 and 10 times larger than the PTM 20nm FinFET HP (20nm InAs Homojunction TFET and 20nm double gate GaSb-InAs Heterojunction TFET [18], 20nm InAs double-gate TFET and GaN/InN single gate TFET [19], [20]). However I_{ON} currents are smaller in three of them. AlGaSb/InAs double-gate TFET increases current ratio by 6000. This device is a TFET with an extremely low I_{OFF} (~1pA/µm), but very low I_{ON} (~6 times smaller than the Hyper-FET). Note that this comparison should be taken with care. Simply comparing current ratios or I_{ON} at a given supply voltage is completely insufficient to extract conclusions.

In addition the logic operation of different logic gates has been checked. Fig 4a shows waveforms for an inverter with C_{Load}=5fF for an input frequency of 100MHz. Correct operation is observed. The nonidealities exhibited by the DC transfer characteristic of Hyper-FET based gates, with non-zero output voltage level associated to logic 0, and voltage level associated to logic 1 distinct from V_{DD}, are not observed. As explained in Part II, these degraded logic levels are the result of a charging/discharging process occurring through the high resistance associated to the PTM device in the insulate state. Thus, it does not manifest for high enough switching rates of the gate output. However, if the output of the gate does not switch so often, as a result of circuits operated at low frequencies or with low switching activity, these degraded logic levels are reached.

Fig 4b shows the behaviour of the same inverter for a low frequency input (1KHz). The discharging of the output node

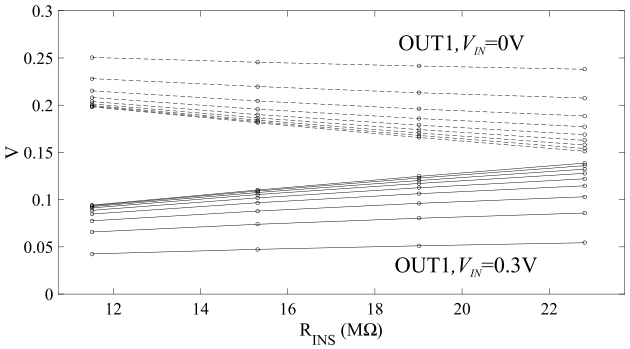

Fig 6. Static inverter DC output voltages for selected values of R_{INS}. Several values of V_{IN} have been simulated.

from V_{DD} = 300mV to 269mV and the charging from 0V to 22mV is observed. The states of both PTMs have been also monitored. Signal STATE P (STATE N) corresponds to the PTM in the *P*-type (*N*-type) Hyper-FET. Low levels of these signals are associated with the corresponding device in the metallic state and high levels with the device in the insulating state. The inverter exhibits the expected behaviour. During the output transitions, one of the PTMs switches to the metallic state. The PTM associated to the *P*-type (*N*-type) Hyper-FET switches in the low to high (high to low) transitions of the inverter output, so that, charging (discharging) current slightly degrades with respect to the inverter built form transistors and so speed is similar. When no transition is occurring, both PTMs are in the insulating state so leakage currents are largely reduced, leading to static power reductions. In this example, static power consumption of this Hyper-FET inverter is 0.72nW and 6.72nW for the FinFET inverter. However, at the circuit level, these degraded logic levels can impact the operation of other gates and should be analysed. For that, the chain of inverters in Fig 5a has been simulated.

In spite of the non-ideal behaviour described for the inverter, the circuit operates correctly. Fig 5b depicts the output of the first and the ninth stages of the inverter chain when the applied input frequency is 1KHz. This behaviour can be explained on the basis of the self-correcting capability of Hyper-FETs gates. When input signals degrade too much, PTMs switch to the metallic state and logic levels are regenerated at the output of the gate. In order to further analyse this, we have monitored the states of the PTMs. Results for the second and third stages are depicted in Fig 5c and Fig 5d, respectively. Second stage exhibits the desired behaviour in spite of the degraded input it receives (the output of the first stage in Fig 5b). That is, except during the transitions, the PTMs are in the insulating state. The behaviour exhibited by the third stage is completely different. PTMs are in metallic state most of the time. Because of this, logic levels are regenerated but almost no reduction of leakage current is expected. We have checked that this behaviour is exhibited by the third, the sixth and the ninth stages. Thus, static power advantages cancel in these stages, reducing power savings at the circuit level. Moreover, static power and power at low input switching rates could be larger for the Hyper-FET circuit than for its conventional counterpart due to the degraded logic levels on their inputs, producing larger leakage currents. Results described in next Section support these claims concerning power penalties.

DC output voltages of the inverter for low (close to 0V) and for high (close to V_{DD}) input voltages depend on the

resistance of the PTMs in the insulating state with respect to the OFF resistance of the transistor. Fig 6 shows the inverter DC output voltage (OUT1) for V_{IN}=0V (dashed line at top), and for V_{IN} =0.3V (solid line at bottom), versus the resistivity of the insulating state. OUT1 for V_{IN}=0V (V_{IN}=0.3V) reduces (increases) when the off resistance of the PTM device is increased. Figure also shows how, after being propagated through several inverters, levels would degrade assuming the PTMs of any stage in the insulator state. For example, second line from bottom/top corresponds to the output of the third inverter. We claim that since the gate output voltage levels are determined by R_{INS}, it is interesting to include this device parameter in the power performance evaluations carried out in next Section.

IV. Power Evaluation

Fig 7 shows average power versus input signal frequency for the fifth and the sixth stages of the Hyper-FET chain of inverters. The fifth (the sixth) stage behaves like the second (the third) in previous Section. They have been selected for power measures because they are well embedded into the inverter chain. A single stage is depicted for the FinFET counterpart circuit since there are no differences in this case. Static power for both a Hyper-FET and a conventional inverter are also shown. Static power for the Hyper-FET inverter has been measured considering both PTMs in the insulating state. That is, assuming it exhibits the correct/desired behaviour.

As expected, this ideal static power of the Hyper-FET inverter is almost one order of magnitude lower than static power of the FinFET inverter. However, at low input frequencies, power performances of the two selected Hyper-FET stages are different. Actually, three different frequency regions can be distinguished in terms of the behaviour of the Hyper-FET stages.

For the lowest frequencies (Region I), the sixth stage is significantly less efficient than even the FinFET inverter, as we anticipate from the analysis in previous Section. PTMs of stage 6 are in the metallic state for a large fraction of the time and its input voltages are degraded. Power benefits exhibited by the fifth stage are due to the advantages in terms of static power of well behaving Hyper-FETs inverters.

At the highest input frequencies (Region III) both Hyper-FET stages behave similar and exhibit lower power than FinFET. Although, as expected, and since the contribution of the static power reduces with input frequency, the fraction of saved power also falls. At very low input frequencies, the power of the fifth stage (the one working as desired) is less than 20% of the FinFET power. It is over 80% for the highest frequency in the figure.

Finally, there is an intermediate range of frequencies (Region II) in which results for stage 5 and stage 6 differ, unlike in Region III, although they are more similar than in Region I. Moreover, larger power values are observed for stage 5 for some frequencies. This region is explained taking into account that the behaviour of each stage in the chain depends also on the switching frequency, since it determines how much logic levels are degraded. At the frequency considered in Fig 5 in Section III, stage 5 behaves as it is desired (with PTMs most time in insulating) while stage 6 does not. Logic levels at the output of stage 5 are so much degraded that PTMs of stage 6 are most time in metallic. However, analysis of the simulation waveforms at

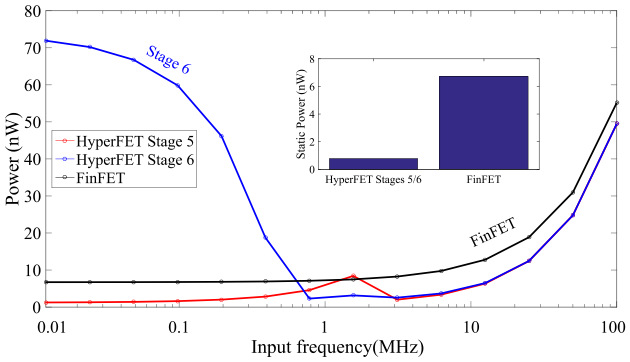

Fig 7. Power versus input frequency for a FinFET stage and stages 5 and 6 of the Hyper-FET chains of the inverters. Static powers for both designs have been also included.

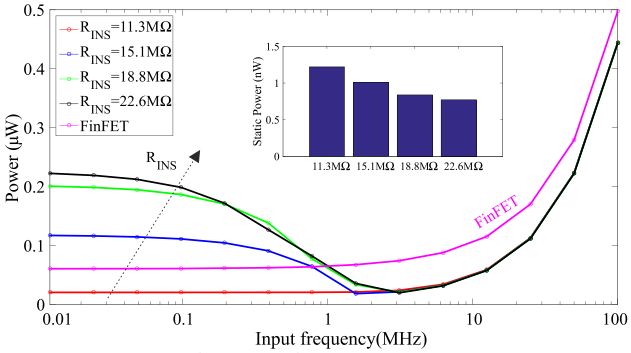

Fig 8. Power versus frequency for the FinFET and the Hyper-FET chains of inverters considering different values of R_{INS}. Ideal static power for the Hyper-FET inverters has been also included.

the intermediate frequencies shows differences. First, PTMs of both stages are most time in insulating, in agreement with power values lower or similar than for the FinFET inverter, although short periods in the metallic state are observed, in addition to those associated to the gate output transition. Second, both stages exhibit quite more similar performance in terms on the fraction of time PTMs are in metallic, and even, there are frequencies at which this fraction is slightly larger for stage 5 than for stage 6.

In order to take into account the different behaviour of a given stage with the switching frequency, Fig 8 shows power versus input signal frequency for the nine stage chains of inverters. Different values of R_{INS} have been evaluated. The value 22.6MΩ is the one used in previous experiment. It can be clearly observed in Fig 8 that, in spite of the power savings achieved by some stages of the Hyper-FET circuit, Hyper-FET chain consumes larger power than its conventional counterpart for low input switching frequencies. These power penalties at low frequencies reduce when R_{INS} is reduced, as we anticipated in previous Section. Power savings are achieved only with one of the analysed values, R_{INS}=11.3MΩ. Also, ideal static power of a single inverter (assuming both PTMs in the insulating state) for the different R_{INS} values are depicted. Static power increases when reducing R_{INS}, as expected, but at the circuit level, smaller R_{INS} are preferable.

The previous discussion has been carried out in terms of R_{INS}, a parameter of the PTM electrical model. It is interesting relating it to the material and geometrical parameters describing the PTM. R_{INS} can be reduced, without modifying the remaining model parameters, in different ways. First it could be reduced by using the same material parameters in Table I and a larger area. The value 11.3MΩ corresponds to a PTM with twice the area of PTM-

Sim in Table I. Alternatively, the reduction of R_{INS} can be the result of the simultaneous reduction of the insulating resistivity ρ_{INS} and the increment of $J_{C\text{-}IMT}$ by the same amount. The value 11.3MΩs corresponds to a PTM with half ρ_{INS} and double $J_{C\text{-}IMT}$ and same area than PTM-Sim.

Next Section analyses the operation of a functional circuit involving different logic gates and more realistic interconnection patterns.

V. 8 BIT RCA

The operation of an 8–bit Ripple Carry Adder (RCA) composed of Full Adders (FAs) is investigated. The FAs are built from inverters, NAND2 and NAND3 gates. In order to further illustrate the behavior of gates with low output switching activity and its impact on circuit operation, the input carry of the adder (C_{IN}) is fixed to 0. This is quite common in logic design. For example, the available RCA block in a library has a carry input, and it is customized, fixing it to logic 0, if a given design does not require it. Fig 9 depicts simulation results. Data A is switched from (00000000) to (11111111) at a given frequency f_{IN} and data B is constant (11111111). Waveforms for A (actually one bit from A), *S*0 and *S*8 (output carry of the last FA) are shown for f_{IN}=100MHz. In addition the output of the inverter, driven by constant input C_{IN}, signal $C_{IN,C}$, is also shown. Correct logic functionality is observed. *S*0 (*S*8) is 0(1) for *A*=(11111111) and *S*0 (*S*8) is 1(0) for *A*= (00000000). Larger delays in the high to low transition of *S*8 are observed, since, in this case, input changes propagate through the carry chain. However, note the behavior of $C_{IN,C}$. It slowly discharges until a limit voltage is reached. At this moment, the self-recovering mechanism regenerates the voltage level. Clearly there is power wasting associated with this behavior. Note this power penalty is different from the situation in Region I of Fig 7, in which power overheads came from gates working with its PTMs in the metallic state most of the time. Also note that the behavior of $C_{IN,C}$ is similar for f_{IN}=200MHz (last waveform in Fig 9). Additionally, gates directly or indirectly driven by $C_{IN,C}$ (in the signal path from $C_{IN,C}$) are receiving degraded input voltages and could eventually deviate from regular behavior (observe *S*0) and increase their power due to different reasons: larger leakage currents as a consequence of the degraded input voltages or because their PTMs switch to metallic, or repetitively charging of output nodes.

Some power evaluation experiments have been carried out. First, the average power consumed by the inverter driven by C_{IN}=0 ("Inv Hyper-FET RCA") has been measured. Table III summarizes results and compares with the ideal static power of a Hyper-FET inverter ("Inv. Hyper-FET Ideal") and with the static power of a FinFET inverter. It can be clearly observed that actual power savings are much smaller

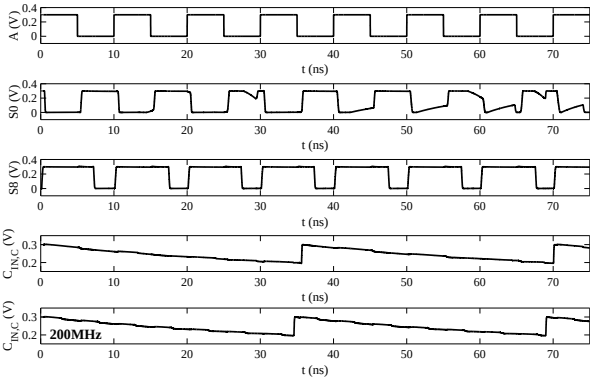

Fig 9. Simulation results for an 8-bit RCA

TABLE III STATIC POWER COMPARISON

Inv.Hyper-FET Ideal	Inv. Hyper-FET RCA	Inv. FinFET
0.72nW	5.60nW	6.72nW

TABLE IV HYPER-FET TO FINFET POWER RATIO OF THE RCA CONSIDERING DIFFERENT SETS OF INPUT PATTERNS

#1	#2	#3	#4	#5
0.763	1.001	0.604	0.781	1.447

than those estimated on the basis of the leakage current reduction associated with the higher resistance of the current path with the two PTMs in the insulating state. In fact, in the simulated condition, the Hyper-FET consumes almost as much as the FinFET one.

Second we have measured average power for the RCAs using five different sets of input patterns. Results are summarized in Table IV, in which Hyper-FET to FinFET power ratios are provided. It can be observed that very distinct power ratios are obtained. Power savings have been obtained in some cases, but also cancellation of power advantages (#2) and power penalties (#5) occur. Power ratios very much depend on input patterns, which determine the switching activity of the different nodes in the circuit. Thus, the evaluation of the advantages in term of power which can be obtained with the Hyper-FET technology cannot be carried out only from considerations of the leakage current reduction it achieves.

VI. CONCLUSIONS

The impact of the degraded DC output voltage levels of Hyper-FET logic gates on circuit operation has been analyzed. It has been shown that the logic operation of the circuits is not compromised due to the intrinsic self-recovering capability of Hyper-FETs gates. However, our experiments show that power advantages, associated to the reduction of the leakage currents with respect to the intrinsic transistor of the Hyper-FETs, estimated at the device/gate level, can reduce, cancel, or even switch to power penalties at the circuit level in low switching activity scenarios. Three different sources of power overheads have been identified: logic gates operating with their PTMs in the metallic states, larger leakage currents due to degraded input voltages and repetitive charging of circuit nodes. Our results suggest the need of further analyzing the operation at circuit level and taking it into account for suitable device design or adopting proper circuit level design techniques.

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