Comparative Analysis of Projected Tunnel and CMOS Transistors for Different Logic Application Areas

Juan Núñez and María J. Avedillo

***Abstract*— In this paper five projected tunnel transistor (TFET) technologies are evaluated and compared with MOSFET and FinFET transistors for high performance low power objectives. The scope of this benchmarking exercise is broader than that of previous studies in that it seeks solutions to different identified limitations. The power and energy of the technologies are evaluated and compared assuming given operating frequency targets. The results clearly show how the power/energy advantages of TFET devices are heavily dependent on required operating frequency, switching activity and logic depth, suggesting that architectural aspects should be taken into account in benchmarking experiments. Two of the TFET technologies analyzed prove to be very promising for different operating frequency ranges and, therefore, for different application areas.**

***Keywords*— Tunnel transistors, Steep subthreshold slope, Low power, Energy efficiency, Low supply voltage.**

I. INTRODUCTION

The physical limit of the minimum subthreshold slope (*SS*) of CMOS technologies (*SS*>60mV/dec) makes it impossible to achieve efficient trade-offs between low threshold voltages and acceptable leakage currents that could allow reducing supply voltage without degrading circuit speed. Thereby, this translates into power density problems for high performance applications requiring nominal supply voltages and energy inefficiency in low voltage applications, where increased long time delays raise leakage current energy so much that any advantages obtained by scaling dynamic power with supply voltage are cancelled out. In this context, intensive research is being conducted into devices with steeper subthreshold slopes (*SS*<60mV/dec) by which low voltage operation at acceptable speeds can be achieved including significant power and energy savings. Tunnel transistors are one of the most attractive steep subthreshold slope devices [1]-[4]. Recently, in [5], benchmarking of many beyond-CMOS devices reinforces that TFETs are the leading low-power devices.

Although the limited ON current of these devices is one of their main causes for concern, TFETs with improved ON currents around 1900μA per micrometer of channel width with a supply voltage of 0.4V have been projected [6]. Moreover, band-to-band tunnel field-effect transistors based on two-dimensional transition metal dichalcogenide semiconductors, with an average *SS* of 31.1mV/dec for four decades of drain current, at a supply-voltage of V_{DD}=0.1V at room temperature have been recently reported in [7].

Emerging devices need to be evaluated at circuit level for a number of reasons and different remarkable benchmarking experiments comparing different emerging devices have been carried out [5], [8]. Benchmarking is necessary to evaluate gains over CMOS and, thereby, identify the devices which are the most promising candidates for replacing or complementing CMOS under different metrics or in different application areas. Several works have shown that TFETs offer significant power and energy reductions [9]-[13]. Many of them have compared realizations of a given circuit implemented with TFETs with its CMOS counterpart at a nominal supply voltage, often producing application-dependent figures of merit. Others have evaluated the impact of reducing supply voltage in CMOS too, comparing a single TFET with a single CMOS. It would be very interesting, however, to make a broader comparison, taking into account not only different application scenarios (high performance, low stand-by power, …), but also CMOS devices targeting different objectives (HP, LP), operated at nominal and reduced supply voltages, and different TFET devices.

In [14] we reported a preliminary work in which power versus frequency curves were built and compared for several TFET and CMOS technologies at different supply voltages. In this paper we present a considerably more comprehensive, in-depth and complete evaluation and comparison, redressing some of the limitations of our previous work. More TFET devices and benchmark circuits have also been included since TFETs can be designed for different targets of OFF current (I_{OFF}) and ON current (I_{ON}) which translates in different performance in terms of speed, power and energy.

Many earlier comparative studies relied on analytical expressions to calculate delay and power from a reduced set of technological parameters like I_{ON}, I_{OFF}, input capacitance and supply voltage. However, several recent papers have illustrated the great impact of certain features specific to TFET transistors, such as super-linear onset, unidirectional conductance, enhanced Miller Capacitance and dominant gate to drain capacitance during performance [15]-[18]. To take these features into account, we carried out an evaluation-based simulation, carefully choosing the characterized circuits and completing the typical fan-out of 4 (*FO*4) inverter analysis with more complex circuits.

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The technologies were evaluated and compared assuming given operating frequency targets. We believe that this provides a clearer picture than the energy versus delay or power versus frequency (at a given supply voltage) curves shown in other papers [12]. Architectural aspects like logic depth were also included in the study, as suggested by the results reported in [19].

The paper is structured as follows. Section II describes the experiments we carried out. The results obtained for the *FO*4 inverter are shown and discussed in Section III. Section IV analyzes the results obtained for more complex gates in order to explore the impact of the fan-in. 8-bit adders are evaluated and compared in Section V, and finally some conclusions are presented in Section VI.

II. Experiment Description

A. Transistors

TFET devices can be designed for different targets of I_{OFF}, and I_{ON}. Several contributions [5], [12] report results for a set of TFETs exhibiting distinct performance in terms of speed, power and energy. This motivates the inclusion in our work of different types of TFETs. Those public models available in the NANOHUB website [20] satisfy these criteria.

Five different tunnel transistor models were used in this work. Two of them were derived by Pennsylvania State University (PSU) [21] and the other three by Notre Dame University [22] (ND), [23]. The TFETs from PSU were look-up table based Verilog-A models for III-V interband TFETs based on calibrated Synopsys TCAD device simulations. Models with gate lengths of 20nm are available for both a double gate InAs Homojunction TFET (PSU_{HOMO}) and a double gate GaSb-InAs Heterojunction TFET (PSU_{HETE}). The TFET models from ND were based on the Kane-Sze formula for tunneling. In this work, we used models for a planar double-gate InAs TFET (ND_{HOMO}), a double gate AlGaSb/InAs TFET ($ND_{HETE,1}$) and a single gate GaN/InN TFET ($ND_{HETE,2}$).

Four different CMOS transistors were also evaluated for comparison purposes, all of them predictive models obtained from the PTM web page [24]. The ones selected were those with channel lengths similar to the available TFETs, namely: 22nm MOSFET devices for both high performance ($MOSFET_{HP}$, nominal V_{DD}=0.8V) and low power ($MOSFET_{LP}$, nominal V_{DD}=0.95V) applications, and 20nm FinFET transistors for HP ($FinFET_{HP}$, nominal V_{DD}=0.9V) and low stand-by power ($FinFET_{LP}$, nominal V_{DD}=0.9V).

TABLE I. Transistor Characterization

	I_{OFF} Nom.V_{DD} [nA/μm]	I_{ON} Nom.V_{DD} [μA/μm]	I_{OFF} V_{DD}=0.5V [nA/μm]	I_{ON} V_{DD}=0.5V [μA/μm]	I_{OFF} V_{DD}=0.3V [nA/μm]	I_{ON} V_{DD}=0.3V [μA/μm]
PSU_{HOMO}			1.5	140	1.2	32
ND_{HOMO}			0.3	74	0.4	14
PSU_{HETE}			8	606	6	206
$ND_{HETE,1}$			0.001	70	0.001	24
$ND_{HETE,2}$			9	183	9	83
$MOSFET_{HP}$	121	1382	17	311	5	7
$MOSFET_{LP}$	0.03	599	0.004	1.5	0.002	0.005
$FinFET_{HP}$	99	1240	37	379	22	74
$FinFET_{LP}$	0.1	722	0.04	82	0.02	0.6

I_{60} [μA]	PSU_{HOMO}	ND_{HOMO}	PSU_{HETE}	$ND_{HETE,1}$	$ND_{HETE,2}$
	0.14	0.08	1.51	0.32	1.35

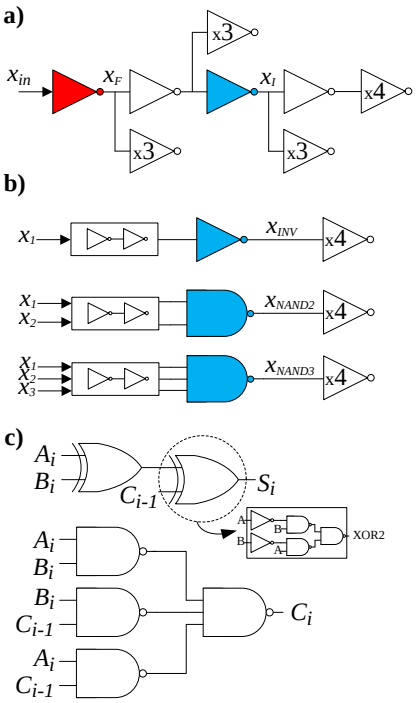

Fig. 1 (a) Circuit used to evaluate the performance of the *FO*4 inverter, (b) Logic gates with different fan ins. (c) Logic diagram of one of the full-adders (FA) of an 8-bit ripple-carry adder (RCA).

Table I summarizes I_{OFF}, I_{ON} and I_{60} [25] for the *n*-type transistors from each of these technologies. From Table I it can be inferred that $ND_{HETE,1}$ is suitable for those scenarios in which static power is dominant (low frequencies). On the other hand, PSU_{HETE} exhibits the largest I_{ON}, thus being the best option for high-speed applications. Experiments described below provide a more accurate evaluation in terms of selected target operation frequencies, using V_{DD} as a design parameter.

B. Circuits and measurements

Fig. 1a shows the circuit we used to evaluate the *FO*4 inverter performance. Note that an intermediate inverter (in blue) was evaluated. The importance of taking into account non-ideal inputs in order to evaluate actual performance is well known. The results are very different if the first stage (in red) is used. In [18] these differences were studied with regard to delay and power in TFET inverters. Their effect on supply voltages differs considerably for each technology, and this impacts not only the absolute values obtained for selected figures of merit, but also the comparison itself. Note that the simple analytical models used for evaluation did not take into account the effect of non-ideal inputs.

Fig. 1b shows the circuit used to evaluate and compare logic gates with different fan-ins. An inverter, a two-input NAND gate (NAND2) and a three-input NAND gate (NAND3) were evaluated (in blue). Note that, again, the gates being tested were loaded with four minimum inverters and their inputs were not ideal but generated with chains of inverters.

A circuit level benchmark was also included, to take into account some issues which had not appeared in previous experiments but which could have an impact on speed or power. These phenomena included glitches due to the propagation of signals through paths with different delays, leading to extra power, and sustained noise voltage pulses due to capacitive coupling and the asymmetric conduction exhibited by TFET devices, leading to delay degradation [16] [26]. An 8-bit ripple carry adder (RCA) was chosen for this circuit level analysis. An RCA is built by interconnecting full-adders (FA). Fig. 1c shows the logic diagram we used for the FA. Note that it comprises inverters and NAND gates.

Transistor sizing

In all the benchmarking circuits, transistors were sized using a minimum gate length. In each case, the *n*-type transistor width was also the minimum allowable (one finger for the FinFETs). MOSFET *p*-type transistors were widened (to twice the minimum value) to compensate for mobility differences. Minimum *p*-type TFET transistors were used because the models already assumed identical drive-on currents for both types of transistors.

Applying the typical scaling rule, the *n*-type transistors in the NAND2 and NAND3 gates were doubled and tripled in width respectively to maintain similar rise and fall characteristics in all the technologies except for the FinFET circuits, where a single finger was used for all the gates.

Measurements

The benchmarking circuits were characterized in terms of delay and power by simulation at different supply voltages (V_{DD} from 0.05V to 1V with a voltage step equal to 0.05V), in order to take into account the impact of the transistors' distinctive characteristics on performance, as mentioned above. For each circuit and technology, the minimum allowable V_{DD} was determined as the minimum supply voltage at which correct functionality could be observed with maximum logic swing degradation of 10%.

Worst case high-to-low and low-to-high propagation delays were measured (at $V_{DD}/2$) for the gates and the RCA. As a figure of merit, we used the average value for these delays.

Average power was evaluated at different operating frequencies, switching activities (α) and logic depths (*LD*) for each of the gates under characterization. Average power for the RCA was measured by applying 100 random input combinations at different frequencies.

The technologies were evaluated and compared assuming given target operating frequencies. That is to say, average power and average energy per operation were compared using the minimum V_{DD} required to operate at each target frequency (f_{TG}). This V_{DD} value could be different for each technology. 13 target frequencies were selected, from 2KHz to 6GHz. For the gate-level experiments, it was assumed that they were being conducted within a logic network with a given *LD*.

III. FO4 INVERTER RESULTS

Fig. 2 shows the power versus frequency curves for *LD*=50 and α=0.1 (with a switching activity of 10%), with logarithmic scales applied to both axes. For each target operating frequency, we evaluated the minimum V_{DD} at which $f_{MAX}>f_{TG}$, where $f_{MAX}=1/(LD\cdot\Delta_{FO4}(V_{DD}))$ is the maximum achievable frequency for certain values of *LD*, and the delay of a minimum V_{DD}-dependent *FO*4 inverter, Δ_{FO4}. The results were normalized with respect to $\text{MOSFET}_{\text{HP}}$, the negative values thus corresponding to technologies displaying better performance than $\text{MOSFET}_{\text{HP}}$. Note that some technologies were not able to achieve the larger frequency targets.

For low frequencies and switching actives (i.e. f_{TG}<10MHz), $\text{ND}_{\text{HETE,1}}$ clearly had the best performance, as expected from Table I. At these frequencies, static and dynamic dissipations were similar in all the technologies, but static power in $\text{ND}_{\text{HETE,1}}$ was around three orders of magnitude smaller than in the others, resulting in a significantly lower total power performance. Note from Table I that I_{OFF} differences between $\text{ND}_{\text{HETE,1}}$ and $\text{MOSFTE}_{\text{LP}}$ or $\text{FinFET}_{\text{LP}}$ devices were not so significant (around one order of magnitude in the worst case) when compared at the same V_{DD}. However, our results show more important improvements because, for low frequencies, $\text{ND}_{\text{HETE,1}}$ required lower V_{DD} values than LP CMOS technologies. This was the only TFET technology to achieve power savings at very low frequencies. The other four TFETs analyzed obtained worse power results than $\text{MOSFET}_{\text{LP}}$ and $\text{FinFET}_{\text{LP}}$ at the smallest frequency target.

When the operating frequency was increased ($f_{TG}\geq$100MHz), PSU_{HETE} was the most power-efficient technology, since it could operate with smaller V_{DD} values than the others (V_{DD}=0.2V @1GHz versus V_{DD}=0.45V for $\text{ND}_{\text{HETE,2}}$ and V_{DD}=0.55V for $\text{MOSFET}_{\text{HP}}$ at the same frequency). Although these results could have been predicted from Table I, now we can accurately define the frequency range in which PSU_{HETE} is competitive. PSU_{HETE} consumed more power than $\text{MOSFET}_{\text{HP}}$ at 2GHz and could not achieve the 3 GHz target. PSU_{HETE} was the only technology that could compete with $\text{MOSFET}_{\text{HP}}$ for target frequencies over 200MHz. The five TFET technologies were competitive with respect to both LP CMOS technologies ($\text{FinFET}_{\text{LP}}$ and $\text{MOSFET}_{\text{LP}}$) over that frequency.

The impact of the variation of *LD* is shown in Fig. 3a, where this parameter is halved with regard to Fig. 2. A reduction in *LD* implies that the minimum V_{DD} at which correct operation is possible (at a certain frequency) can be decreased (thereby also lowering power consumption). This results in larger maximum frequencies up to which power performance is better than for $\text{MOSFET}_{\text{HP}}$ (f_{EFF}). This effect is more significant for TFET than for the MOSFET and FinFET technologies. In PSU_{HETE}, for instance, the frequency is shifted up from 1.8GHz (marked with an arrow in Fig. 2) to 3.7GHz. On the other hand, in CMOS technologies f_{EFF} does not vary significantly with *LD* ($f_{EFF}\approx$2MHz for $\text{MOSFET}_{\text{LP}}$ and $\text{FinFET}_{\text{LP}}$) because for such low frequencies their minimum V_{DD} cannot be reduced when *LD* decreases, and power performance cannot therefore be improved.

The effect of changes in α is illustrated in Fig. 3b, where this value is reduced to 0.01 (*LD*=25, as in Fig. 3a). Static power contribution to total power is significant up to higher frequencies for lower values of α. In this scenario, the most notable power reductions in comparison to $\text{MOSFET}_{\text{HP}}$ were observed in $\text{MOSFET}_{\text{LP}}$ and $\text{FinFET}_{\text{LP}}$, which, with static powers approximately one order of magnitude lower, became

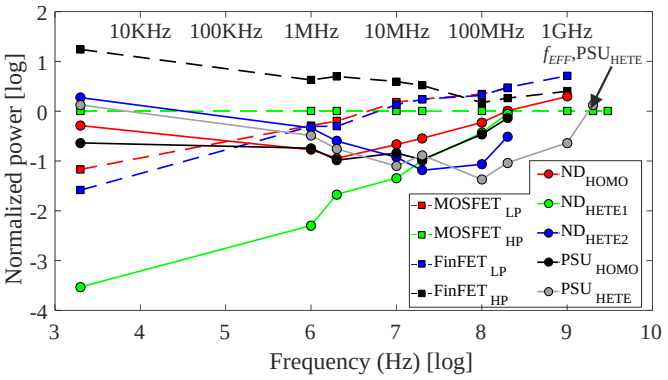

Fig. 2 Power versus frequency curves for LD=50 and α=0.1

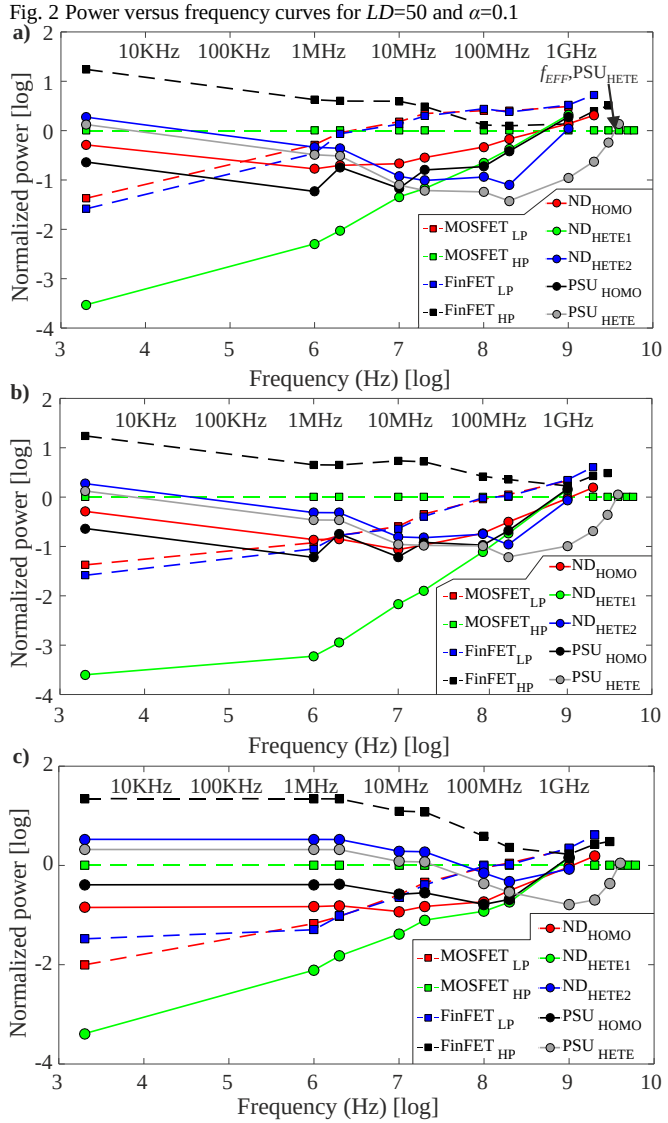

Fig. 3 Impact of LD and α variations in power versus frequency curves. (a) LD=25 and α=0.1. (b) LD=25 and α=0.01. (c) LD=25, α=0.1 and $V_{DD,MIN}$=0.25V.

more efficient up to around f_{EFF}≈100MHz (f_{EFF}≈2MHz@α=0.1). In the TFETs, the frequency up to which ND$_{HETE,1}$ was the best increased, rising from 10MHz (α=0.1) to 100MHz (α=0.01), as can be seen in Fig. 3b.

Fig. 3c shows the results for the experiment in Fig. 3a (LD=25, α=0.1), when the minimum explored V_{DD} ($V_{DD,MIN}$) was raised from 0.05V to 0.25V to take into account the possible practical limitations of lowering supply voltage so much, especially in terms of variability issues [27]. The significant differences between Fig. 3a and Fig. 3c are not qualitative but quantitative. For example, the power savings in MOSFET$_{LP}$ improved with respect to MOSFET$_{HP}$ at the lowest frequency target. The relative order of ND$_{HOMO}$ and PSU$_{HOMO}$, and also of MOSFET$_{LP}$ and FinFET$_{LP}$, was interchanged at that frequency. In general, these quantitative changes were seen at the lower frequencies for which operation with a V_{DD} of under 0.25V was possible. The exception was PSU$_{HETE}$. For this technology, differences were observed up to higher frequencies. Power savings fell for the intermediate target frequencies (from tenths of kilohertz to around 1GHz) that can be achieved with supply voltages of under 0.25V with these transistors.

We next evaluated power consumption versus frequency for three values of α (0.01, 0.1, 0.5) and two of LD (25, 50). For each frequency, LD and α, we chose the most power efficient technology and normalized it with respect to the best CMOS (MOSFET/FinFET) technology. The results are summarized in Table II. In each cell, the first row reports the technology which achieved the lowest power among the nine we analyzed ("Best tech."). The second row shows the CMOS technology with the best power result ("Best CMOS tech."). The third row reports the power consumed by "Best tech." normalized with respect to "Best CMOS tech.". Note that, as in Fig. 2, none of the technologies worked for LD=50 and fTG>3GHz.

It is clear from the table that the power advantages of TFET devices depend heavily on required operating frequency, switching activity and logic depth. (f_{TG}, LD, α) combinations were identified for which no TFET was competitive (the cells with MOSFET$_{HP}$ as the "Best tech.").

The range of normalized power (or power ratio) values obtained was very wide. ND$_{HETE,1}$ had the lowest power consumption ratio (0.0010) with respect to MOSFET$_{LP}$ (at f_{TG}=1MHz and LD=50, α=0.01, marked in blue). This means that ND$_{HETE,1}$ power was 0.1% of the best CMOS power, representing a power saving of 99.9%, that is, ND$_{HETE,1}$ power 1000 times smaller than the best CMOS power. In general, very low ratios were also observed for this technology at low frequencies (reductions of over one order of magnitude in all cases and of over two orders of magnitude in many cases). This is explained by the technology's ultra-low off state current (static power).

The best case in which PSU$_{HETE}$ was better than MOSFET$_{HP}$ gave a power ratio of 2.8% (f_{TG}=20MHz and LD=25, α=0.5, marked in green). The worst case in which PSU$_{HETE}$ was better than MOSFET$_{HP}$ gave a power ratio of 98% (f_{TG}=2GHz and LD=50, α=0.01, marked in red). That is to say, the values varied widely depending on frequency, LD and α. From f_{TG}=2GHz upwards, MOSFET$_{HP}$ began to be the most efficient node. In no case were the homojunction transistors the most competitive.

It was also observed, as described above (Fig. 3a), that the frequency values at which the same normalized power was achieved in comparison with CMOS nodes were larger for LD=25 than for LD=50. As a case example, for ND$_{HETE,1}$ normalized power values (with respect to FinFET$_{LP}$) around

TABLE II. NORMALIZED POWER VERSUS f_{TG} FOR SELECTED (LD,α) PAIRS

f_{TG} (MHz)	(LD,α)					
	(25,0.01)	(25,0.1)	(25,0.5)	(50,0.01)	(50,0.1)	(50,0.5)
0.002	**$ND_{HETE,1}$ $FinFET_{LP}$ 0.0010**	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0113	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0188	**$ND_{HETE,1}$ $FinFET_{LP}$ 0.0010**	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0113	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0188
2	$ND_{HETE,1}$ $MOSFET_{LP}$ 0.0068	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0109	$ND_{HETE,1}$ $MOSFET_{HP}$ 0.0311	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0259	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0431	$ND_{HETE,1}$ $MOSFET_{HP}$ 0.0727
10	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0294	$ND_{HETE,1}$ $MOSFET_{HP}$ 0.0455	PSU_{HETE} $MOSFET_{HP}$ 0.0396	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0294	$ND_{HETE,1}$ $MOSFET_{HP}$ 0.0455	PSU_{HETE} $MOSFET_{HP}$ 0.0396
20	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0316	PSU_{HETE} $MOSFET_{HP}$ 0.0612	**PSU_{HETE} $MOSFET_{HP}$ 0.0280**	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0543	$ND_{HETE,2}$ $MOSFET_{HP}$ 0.0650	$ND_{HETE,2}$ $MOSFET_{HP}$ 0.0410
100	$ND_{HETE,1}$ $MOSFET_{LP}$ 0.0860	PSU_{HETE} $MOSFET_{HP}$ 0.0573	PSU_{HETE} $FinFET_{HP}$ 0.0488	PSU_{HETE} $FinFET_{LP}$ 0.1059	PSU_{HETE} $MOSFET_{HP}$ 0.0428	PSU_{HETE} $MOSFET_{HP}$ 0.0336
200-(1000)	PSU_{HETE} $MOSFET_{HP}$ 0.0613-(0.1017)	PSU_{HETE} $MOSFET_{HP}$ 0.0377-(0.1094)	PSU_{HETE} $MOSFET_{HP}$ 0.0323-(0.1104)	PSU_{HETE} $MOSFET_{HP}$ 0.1201-(0.1802)	PSU_{HETE} $MOSFET_{HP}$ 0.0920-(0.2312)	PSU_{HETE} $MOSFET_{HP}$ 0.0855-(0.2390)
2000	PSU_{HETE} $MOSFET_{HP}$ 0.2024	PSU_{HETE} $MOSFET_{HP}$ 0.2358	PSU_{HETE} $MOSFET_{HP}$ 0.2398	**PSU_{HETE} $MOSFET_{HP}$ 0.9755**	$MOSFET_{HP}$ $MOSFET_{HP}$ 1	$MOSFET_{HP}$ $MOSFET_{HP}$ 1
3000	PSU_{HETE} $MOSFET_{HP}$ 0.4369	PSU_{HETE} $MOSFET_{HP}$ 0.5694	PSU_{HETE} $MOSFET_{HP}$ 0.5863	$MOSFET_{HP}$ $MOSFET_{HP}$ 1	$MOSFET_{HP}$ $MOSFET_{HP}$ 1	$MOSFET_{HP}$ $MOSFET_{HP}$ 1
4000-6000	$MOSFET_{HP}$ $MOSFET_{HP}$ 1	$MOSFET_{HP}$ $MOSFET_{HP}$ 1	$MOSFET_{HP}$ $MOSFET_{HP}$ 1	--- --- ---	--- --- ---	--- --- ---

3% are obtained at 20MHz and 10MHz for LD=25 and LD=50, respectively (with α=0.01).

On the other hand, for the same f_{TG}, normalized power was equal or better for the lowest LD. Improvements were greater for higher frequencies. At f_{TG}=1GHz and α=0.1, for example, the normalized power of PSU_{HETE} compared to $MOSFET_{HP}$ was over twice as small for LD=25 (0.1094) than for LD=50 (0.2312). And for f_{TG}=2GHz, α=0.01, it was more than four times smaller. For both technologies, power fell when LD was decreased from 50 to 25 since the V_{DD} required to operate at a given frequency decreases when the logic paths for signal propagation are shortened (smaller LD). The results therefore show that the amount by which power is reduced is larger for PSU_{HETE} than for $MOSFET_{HP}$. This is due to the different delay versus V_{DD} behaviors shown by TFETs and CMOS.

In TFETs there is a larger, flat region in which delay slightly increases with V_{DD} reduction. The reduction in V_{DD} achieved by changing from LD=50 to LD=25 is larger for PSU_{HETE} than for $MOSFET_{HP}$. This illustrates the limitations of benchmarking by simply comparing the performance of $FO4$ inverters or using a fixed LD value, and suggests that evaluation experiments should ideally take into account architectural aspects (like LD). In other words, different architectural options may be more appropriate for different technologies. With regard to the LD parameter, for example, LD=25 can be interpreted as a two-stage pipelined implementation of an original circuit with LD=50 (assuming ideal pipeline registers). In this scenario, our results show that pipelining to reduce power consumption is more efficient for the TFET technology than for CMOS. We compared power for both LD values in each technology. For PSU_{HETE}, power with LD=25 was 13% of power with LD=50, and for $MOSFET_{HP}$ it was 65%. The significantly larger saving shown by PSU_{HETE} suggests that pipelining can be an efficient technique for obtaining power and energy savings, (more remarkable for TFETs than for CMOS) even taking into account the power overheads associated with its registers.

Finally, it should be noted that $FinFET_{HP}$ did not emerge as "Best CMOS Tech" in any of the cases analyzed. This, however, should not be interpreted as an indication that this technology is not competitive with respect to $MOSFET_{HP}$, but as the result of the sizing selected for the experiment, which produced larger capacitance for the FinFET technologies. This will be clarified in the next section, where more complex gates and functional circuits are analyzed. In spite of the sizing strategy, in Table II $FinFET_{LP}$ still appears as the best CMOS

technology for the lowest frequency targets (see Fig. 2 and Fig. 3), since in these cases power is not dominated by the charging and discharging of transistor capacitance.

Average energy per operation (E) versus frequency curves in the $FO4$ inverter are shown in Fig. 4 for LD=50 and α=0.1. Energy was calculated as $E=P/f$, using the minimum V_{DD} required to operate at such a frequency. No explicit general comments on these figures are made because the conclusions drawn regarding power performance also apply to energy. Our interest here is in analyzing the minimum energy point. It can be observed that TFET inverters have smaller minimum energy values than CMOS inverters. In particular, $ND_{HETE,1}$, the best one, has values around 1.6 orders of magnitude lower than its best CMOS counterpart ($MOSFET_{HP}$ in this case). Unlike energy versus V_{DD}, which is usually used, this representation also makes it possible to evaluate the energy-speed tradeoff achieved by each technology. The minimum energy points of all the TEFTs except PSU_{HETE} were obtained at frequencies lower than in HP CMOS, although slightly higher than in LP CMOS. In fact, the only TFET technology to show an advantage in terms of E/f (a figure of merit for estimating energy-speed tradeoff) was PSU_{HETE}. The minimum energy for each technological node does not necessarily correspond to the lowest V_{DD}. The critical V_{DD} value for minimum energy ($V_{DD,OPT}$) is much lower in TFET than in MOSFET/FinFET because the on/off current ratio in tunnel technologies is larger (the SS is steeper), as corroborated in previous works [19], [13], [27].

The impact of LD and α on energy performance is illustrated in Fig. 5. In Fig. 5a, LD was reduced to 25, without significantly modifying the energy curves but with slight differences in the frequency at which minimum energy was achieved. On the other hand, a downward shift in energy was seen when the switching activity factor was decreased by 10, as shown in Fig. 5b for α=0.01. Note that LD was only multiplied by 2 (the doubling frequency for a given V_{DD}), which explains the more notable impact of the variation in α with respect to the experiment in which LD was varied. We also found that energy is also impacted by $V_{DD,MIN}$. The advantages of $ND_{HETE,1}$ with respect to CMOS in terms of minimum energy, for example, dropped to around one order of magnitude for $V_{DD,MIN}$ =0.15.

IV. Fan-in Experiment Results

This Section analyzes the performances of more complex gates. More specifically, the inverter is compared to the NAND2 and NAND3 gates as a case study. The test bench for this experiment is shown in Fig. 1b.

The experiment shown in Table II in Section III was repeated for all three gates. That is to say, for each frequency, LD and α, we chose the technology with the best power consumption and normalized its average measured power with respect to the best MOSFET/FinFET technology result. The best technology ("Best tech.") and CMOS technologies ("Best CMOS tech.") at each target frequency are shown in Table III for one of the LD and α combinations (LD=25, α=0.1). The regions in which $MOSFET_{LP}$ or $FinFET_{LP}$ are the "Best CMOS tech." (low frequencies) are distinguished from those in which $MOSFET_{HP}$/$FinFET_{HP}$ are the most efficient by a bold line.

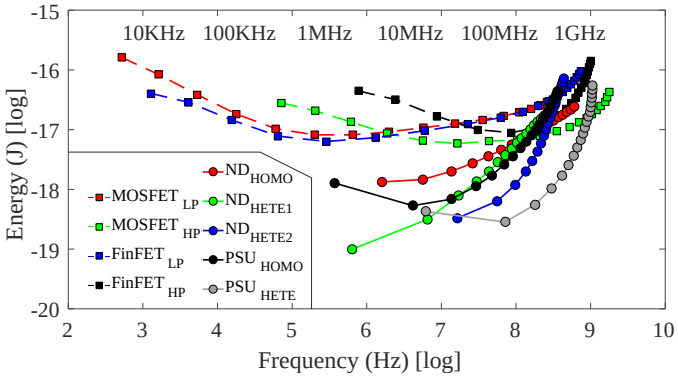

Fig. 4 Energy versus frequency curves for LD=50 and α=0.1.

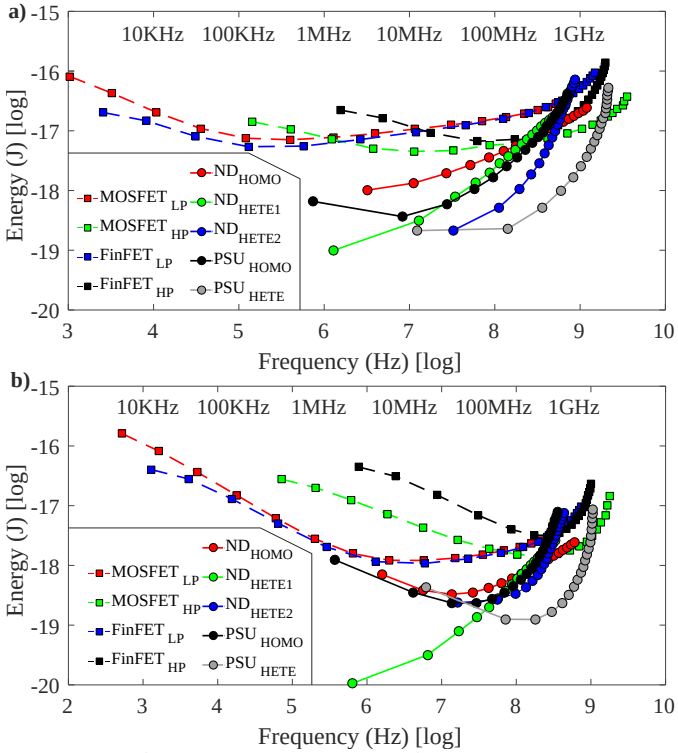

Fig. 5 Impact of LD and α on energy versus frequency curves. (a) LD=25, α=0.1. (b) LD=50, α=0.01.

Note that, unlike in the previous Section, $FinFET_{HP}$ now appears as the "Best CMOS tech." for several target frequencies of NAND2 and NAND3. The benefits of the $FinFET_{HP}$ technology could not be shown in the inverter experiment described in Section III, but now, with more complex gates, they could. The border frequencies obtained between regions increased with fan-in. Note the clear correspondence between the regions described above and the frequency ranges at which $ND_{HETE,1}$ and PSU_{HETE} (highlighted in Table III) are the best "Best tech.".

Care should be taken when comparing the normalized power results obtained for the different gates (the third row in each cell) because in many cases the comparison would be between data corresponding to different technologies and, moreover, normalized with respect to different CMOS technologies. However, it is still interesting to look at the results obtained for NAND2 and NAND3 in those cases in which "Best CMOS tech." and "Best tech." match each other. Two different

TABLE III. NORMALIZED POWER OF THE BEST TFET FOR EACH TARGET FREQUENCY WITH RESPECT TO THE BEST CMOS (LD=25, α=0.1)

Gate	**INV**	**NAND2**	**NAND3**
f_{TG}(MHz)	Best tech. Best CMOS tech.	Best tech. Best CMOS tech.	Best tech. Best CMOS tech.
0.002	$ND_{HETE,1}$ $MOSFET_{LP}$ 0.0192	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0167	$ND_{HETE,1}$ $MOSFET_{LP}$ 0.0137
10	$ND_{HETE,1}$ $FinFET_{LP}$ 0.1121	$ND_{HETE,1}$ $FinFET_{LP}$ 0.1178	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0440
20	PSU_{HOMO} $MOSFET_{HP}$ 0.0679	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0810	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0515
100	PSU_{HETE} $MOSFET_{HP}$ 0.1053	PSU_{HETE} $FinFET_{LP}$ 0.0702	$ND_{HETE,1}$ $FinFET_{LP}$ 0.0973
1000	PSU_{HETE} $MOSFET_{HP}$ 0.0924	PSU_{HETE} $FinFET_{HP}$ 0.0707	PSU_{HETE} $FinFET_{LP}$ 0.2886
2000-(6000)	PSU_{HETE} $MOSFET_{HP}$ 0.1313-(0.2630)	PSU_{HETE} $FinFET_{HP}$ 0.1169-(0.5487)	PSU_{HETE} $FinFET_{HP}$ 0.3169-(0.9113)

behaviors can be observed. For low frequencies, between 1MHz and 20MHz ($FinFET_{LP}$ as "Best CMOS tech." and ND_{HETE1} as "Best tech."), normalized power is smaller in NAND3 than in NAND2. At these frequencies, the contribution of static power due to leakage currents dominates in $ND_{HETE,1}$ and, so, advantages in terms of the stack factor could be better in this technology than in $FinFET_{LP}$. This was also reported in [28]. For high frequencies between 1GHz and 4GHz ($FinFET_{HP}$ as "Best CMOS tech." and PSU_{HETE} as "Best tech."), the opposite behavior is observed. That is, the normalized power of TFET is higher in NAND3 than in NAND2. In this case, dynamic power dominates and the results obtained can be put down to the sizing strategy, with pull-down transistors that are wider in the TFET NAND3 with respect to NAND2 but identical in the FinFET gates. When PSU_{HETE} power is normalized with respect to $MOSFET_{HP}$, the results for both gates are much more similar.

Finally, note that there are differences between the results reported for the inverter in Section III and those reported in this experiment. Advantages of PSU_{HETE} can now be observed up to frequencies at which it was not previously competitive. These dissimilarities are caused by the different circuits used to drive the gate under characterization. Input is now produced by a fan-out 1 inverter, whereas in the experiment described in Section III a fan-out 4 inverter was used. This confirms that benchmarking experiments are also heavily dependent on selected input waveforms, as discussed above. It also justifies the circuit level evaluation experiment described in Section V and the aforementioned study of how the different features of TFET devices impact circuit operation.

TABLE IV. MEASURED POWER CONSUMPTION FOR THE 8-BIT RCA

	Power (nW)					
	Target frequency (MHz)					
Technology	0.1	1	10	100	500	1000
$MOSFET_{LP}$	0.1	1.41	19.4	307	2010	5120
$MOSFET_{HP}$	0.7	0.85	**9.6**	113	650	1580
$FinFET_{LP}$	**0.048**	**0.67**	11.7	154	1168	2890
$FinFET_{HP}$	9.96	10.1	11	**68.9**	**365**	**1020**
$ND_{HETE,1}$	**0.002**	**0.02**	**0.69**	15.6	524	2310
$ND_{HETE,2}$	0.64	0.66	0.85	**2.76**	109	658
PSU_{HETE}	1.30	1.34	1.63	4.36	**15.9**	**84**
Norm. power	0.04	0.03	0.07	0.04	0.04	0.08

V. CARRY PROPAGATION ADDER RESULTS

Table IV summarizes the power results for the 8-bit RCA adders implemented with the four CMOS transistors and the three heterojunction TFET technologies. The homojunction TFETs are omitted, since they were not shown to be competitive in any of the comparisons carried out at gate level in the previous sections. The best CMOS and best TFET results for each frequency are shown in bold type.

Note that the results obtained agree with those obtained at gate level. For each of the moderate frequency targets explored, the most competitive power solution corresponded to a TFET technology, with large power and energy savings being achieved in all cases. The ratio between the smallest power achieved with TFET technologies and the smallest power obtained with CMOS transistors was evaluated and is shown in the last row in Table IV. Power reductions ranged from 92% (1GHz) to 97% (1MHz), although they did not decrease monotonically with frequency. Again, this can be explained by the different delay versus V_{DD} behavior shown by the TFET and CMOS transistors and by experimental discretization.

Normalized power values for NAND2 (NAND3) in Table III (up to 1GHz) were between 0.02 and 0.12 (0.01 and 0.29), and slightly smaller for the RCA (between 0.03 and 0.08). However, it should be noted that, in this experiment, LD and α were different. That is to say, the power savings obtained for the benchmark at circuit level were larger than those obtained in the gate level experiment with LD=25 and α =0.1.

It is also interesting to compare the last two columns of Table IV. For all the CMOS transistors, power at 0.5GHz is less than three times smaller than power at 1GHz. Assuming dynamic power dominates at these frequencies, and that power halves when the circuit is operated two times more slowly, the additional power savings stem from supply voltage reductions associated with smaller frequency targets. For TFET transistors, the reduction factor is over 4 (4.40 for $ND_{HETE,1}$, 6 for $ND_{HETE,2}$ and 5.3 for PSU_{HETE}). Power savings associated with supply voltage reduction are therefore larger for TFETs, and when frequency targets are relaxed, supply voltage reductions supported by TFETs, are larger than in CMOS. This fully concurs with the results described at gate level, and may be specifically related to our analysis of the impact of logic depth when comparing power and energy advantages. Experiments carried out at circuit level also show that the impact of techniques to improve throughput used for power optimization is larger in TFET technologies. From this perspective, these results show that the power benefits that can be obtained by using parallelism in the implementation of the

adder with a throughput target of 1GHz (each individual copy operating at 0.5GHz) are larger in TFET than in CMOS. They also seem to indicate that evaluation experiments should take into account architectural aspects.

VI. CONCLUSIONS

The experiments carried out in this study show that estimating TFET power benefits or energy savings simply from the reductions obtained in V_{DD} with respect to nominal supply voltages in CMOS technologies can be misleading. The advantages of TFET devices depend heavily on required operating frequency, switching activity, logic depth and the minimum supply voltage that is practical for actual circuit applications. As in conventional CMOS technologies, a single device is not competitive in all application domains.

Of the five TFET technologies analyzed, two were identified as competitive devices in two different application fields. $ND_{HETE,1}$ is suitable for applications in which static power dominates (very low frequency-switching activity products), but has severe speed limitations. It offers significant advantages in power and energy with respect to CMOS, even with regard to LP devices in this domain. PSU_{HETE} was seen to be greatly advantageous in terms of power and energy in a given frequency range, the exact position of which depends on logic depth and switching activity. In addition, we have found that only the two most promising transistors in terms of speed (PEN_{HETE} and $ND_{HETE,2}$) exhibit I_{60} in the 1-10μA/μm range, identified in [25] as the required range to be competitive with CMOS. For these devices, power-related advantages are associated with lower required supply voltages than those applicable in CMOS, to fulfill with the constraint on path delay imposed by working frequency. This suggests the existence of limitations in benchmarking experiments in which identical CMOS and TFET circuits are evaluated and compared. The adoption of architectural solutions involving path delay constraints capable of fully exploiting TFETs distinctive speed versus supply voltage behavior can make TFET logic circuits competitive up to higher frequencies, increasing their power (energy) efficiency.

Circuit-level evaluation using an 8-bit RCA showed that TFET implementations using $ND_{HETE,1}$ for low frequencies and PSU_{HETE} for larger frequencies have power (energy) consumption values between 3% and 8% of the best values obtained with CMOS. Although CMOS RCAs achieve higher operating frequencies, our results suggest that architectural techniques like pipelining or parallelization could be applied to TFET designs to enable them to operate at those higher frequencies without losing their power and energy advantages.

REFERENCES

[1] A. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proceedings of the IEEE*, vol. 98, no. 12, Dec. 2010.

[2] A. Seabaugh, "The Tunneling Transistor ", *IEEE Spectrum*, vol.2, no.4, pp.55-62, Oct. 2013.

[3] H. Lu and A. Seabaugh, "Tunnel Field-Effect Transistors: State-of-the-Art", *J. of the Electron Device Society*, vol.2, no.4, pp.44-49, Jul. 2014.

[4] U. E. Avci, D.H. Morris and I.A. Young, "Tunnel Field-Effect Transistors: Prospect and Challenges*", IEEE Journal of the Electron Device Society*, vol. 3, no. 3, pp. 88-95, Jan. 2015.

[5] Nikonov, Dmitri E., and Ian A. Young. "Benchmarking of beyond-CMOS exploratory devices for logic integrated circuits." *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 1 pp. 3-11, Dec. 2015.

[6] S. Koswatta.; S. Koester; W. Haensch, "On the Possibility of Obtaining MOSFET-Like Performance and Sub-60-mV/dec Swing in 1-D Broken-Gap Tunnel Transistors," *IEEE Trans. on Elec. Dev*,vol.57,no.12, pp.3222-3230, 2010.

[7] Deblina Sarkar et al., "A subthermionic tunnel field-effect transistor with an atomically thin channel", *Nature*, vol. 526, pp. 91-95, Oct. 2015.

[8] K. Bernstein, R.K. Cavin, A. Seabaugh and J. Welser, "Device and Architecture Outlook for Beyond-CMOS Switches," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2169-2184 Dec. 2010.

[9] A.M. Ionescu, H. Riel: "Tunnel field-effect transistors as energy-efficient electronic switches", *Nature*, no. 479, pp. 329–337, 2011.

[10] H. Chenming; P. Patel; A. Bowonder; J. Kanghoon et al., "Prospect of tunneling green transistor for 0.1V CMOS," *Electron Devices Meeting, IEEE International*, pp.16.1.1/4, 2010.

[11] H. Liu, S. Datta, V. Narayanan, "Steep switching tunnel FET: a promise to extend energy efficient roadmap for post-CMOS digital and analog/RF applications", *Symp. on Low Power and Design*, 2013.

[12] K. Swaminathan, M. Seok Kim, N. Chandramoorthy, B. Sedighi, R. Perricone, J. Sampson and V. Narayanan, "Modeling Steep Slope Devices: From Circuits to Architectures", *Proceedings Design, Automation and Test in Europe Conference*, 2014.

[13] S. Datta, R. Bijesh, H. Liu, D. Mohata and V. Narayanan, "Tunnel Transistors for Low Power Logic", *IEEE Compound Semiconductor Integrated Circuit Symposium*, pp. 1-4, Oct. 2013.

[14] M.J. Avedillo and J. Núñez, "Assessing application areas for tunnel transistor technologies", Proceedings *of the XXX Design of Circuits and Integrated Systems Conference* (DCIS), pp. 1-6, 2015.

[15] S. Mookerjea, R. Krishman and S. Datta, "On Enhanced Miller Capacitance Effect in Interband Tunnel Transistors", *IEEE Electron Devices Letters*, vol. 30, no. 10, pp. 1102-1104, Oct. 2009.

[16] D.H. Morris, U.E Avci, R. Rios and I.A Young, "Design of low voltage Tunneling-FET logic circuits considering asymmetric conduction characteristics", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 4, no.4, pp. 380-388, Dec. 2014.

[17] A. Pal, A.B. Sachid, H. Gossner and V.R. Rao, "Insights into the design and optimization of tunnel-FET devices and circuits", *IEEE Trans. On Electron Devices*, vol. 58, no. 4, pp. 1045-1053, April 2011.

[18] N. Dagtekin and A.M. Ionescu: "Impact of Super-Linear Onset, Off-Region Due to Uni-Directional Conductance and Dominant C_{GD} on Performance of TFET-Based Circuits", *Journal of the Electron Devices Society*, vol. 3, no. 3, pp. 233-239, May 2015.

[19] M. Alioto and D. Esseni, "Tunnel FETs for Ultra-Low Voltage Digital VLSI Circuits: Part II–Evaluation at Circuit Level and Design Perspectives", *IEEE Trans. On VLSI Systems*, vol. 22, no. 12, pp. 2499-2512, Dec. 2014.

[20] nanoHUB. https:// nanohub.org.

[21] H. Liu; V. Saripalli; V. Narayanan; S. Datta (2014), "III-V Tunnel FET Model 1.0.0," https://nanohub.org/resources/21012.

[22] H. Lu T. Ytterdal, A. Seabaugh, "Universal TFET model". nanoHUB. doi:10.4231/D3901ZG9H.

[23] H. Lu, D. Esseni, and A. Seabaugh, "Universal analytic model for tunnel FET circuit simulation," *Solid-State Electronics*, 2015, vol. 108, pp. 110-117, June 2015.

[24] W. Zhao and Y. Cao, "New generation of predictive technology model for sub-45nm design exploration", *Proc. 7th Int. Symp. Quality Electronic Design*, 2006.

[25] Vandenberghe, William G. et al., "Figure of merit for and identification of sub-60 mV/decade devices", *Applied Physics Letters*, vol. 102, id. 013510. 2013.

[26] M. J. Avedillo and J. Nuñez, "Improving speed of tunnel FETs logic circuits," *IET Electronics Lett.*, vol.51, no.21, pp.1702-1704, Oct. 2015.

[27] S. Strangio, P. Palestri, et al., "Assessment of InAs/AlGaSb Tunnel-FET Virtual Technology Platform for Low-Power Digital Circuits*", IEEE Trans. On Electron Devices*, vol. 63, no.7, pp. 2749-2756, July, 2016.

[28] D. Esseni, M. Guglielmini, B. Kapidani, T. Rollo, M. Alioto, "Tunnel FETs for Ultra-Low Voltage Digital VLSI Circuits: Part I – Device-Circuit Interaction and Evaluation at Device Level," *IEEE Trans. on VLSI Systems*, vol. 22, no. 12, pp. 2488-2498, Dec. 2014.