Experimental Validation of a Two-Phase Clock Scheme for Fine-Grained Pipelined Circuits Based on Monostable to Bistable Logic Elements

Juan Núñez, María J. Avedillo and José M. Quintana

Abstract— **Research on fine-grained pipelines can be a way to obtain high performance applications. Monostable to Bistable (MOBILE) gates are very suitable for implementing gate-level pipelines which can be achieved without resorting to memory elements. The MOBILE operating principle is implemented operating two series connected Negative Differential Resistance (NDR) devices with a clock bias. This paper describes and experimentally validates a two-phase clock scheme for such MOBILE based ultra-grained pipelines. Its advantages over other reported interconnection schemes for MOBILE gates, and also over pure CMOS two-phase counterparts, are stated and analyzed. Chains of MOBILE gates have been fabricated and the experimental results of their correct operation with a two-phase clock scheme are provided. As far as we know, this is the first working MOBILE circuit to have been reported with this interconnection architecture.**

Index Terms— **Monostable-to-Bistable Logic Element, Negative Differential Resistance, Pipeline, Clock schemes.**

I. INTRODUCTION

The design of functional units implementing very fine-grained pipelining for high performance applications is currently a very active area of research. These solutions do not apply conventional pipeline techniques, which insert flip-flops to short down signal propagation paths in combinational logic, but instead rely on logic circuit styles which naturally are able to block the propagation of data. That is, evaluation of their inputs can be disabled. The potential of dynamic logic, with its precharge and evaluation phases, in implementing this kind of pipelining was recognized long ago [1], [2]. The operation of Domino logic in a pipelined fashion using an overlapping multi-phase clock scheme and without latches between consecutive clock phases was analyzed in depth in [2]. It is known that variations of this multi-phase solution (three to six phases) have been developed by different companies and applied to commercial applications [3], [4].

In these superpipeline logic styles, operating frequency (or throughput) depends both on the number of clock-phases and the number of gate levels per clock-phase. The clock period needs to accommodate all the phases and the duration of each phase is determined by the number of gate levels per clock-phase. Thus, from the point of view of ultra high speed applications, a two-phase scheme with a single gate per clock-phase is very attractive.

Logic styles based on the Monostable to Bistable (MOBILE) operating principle are very suitable for implementing gate-level pipelines which can be achieved without resorting to memory elements [5]. Originally, MOBILE gates were operated in a pipelined fashion using a four-phase clock scheme, but a two-phase overlapping clocking is also possible. MOBILE gates are implemented operating two series connected Negative Differential Resistance (NDR) devices with a switching bias. Different devices like Resonant Tunneling Diodes, transistors [6] or molecular devices [7] exhibit NDR in their *I-V* characteristic. Many circuits have been reported which use NDR for different applications (memories, logic, oscillators, A/D converters) and with different goals (high speed, low power or low device count,...) [8], [9] and the MOBILE principle has been identified as a key element in crossbar architectures [10]. In particular, MOBILE RTD-CMOS pipelined architectures have been compared to conventional CMOS fine-grained pipelines [11] and shown to be significatively more power efficient than conventional CMOS. Also, different transistor circuits have been explored that emulate the NDR characteristic [12], [13], [14], [15], [16]. This paper explores in depth and experimentally validates the two-phase clock scheme for MOBILE based fine-grained pipelines. These pipelines do not have the functional limitation of the Domino solutions, in which only non-inverting blocks can be chained. Also, the well known race-through failure of two-phase fine grained Domino pipelines without latches is eliminated.

This paper is organized as follows: in Section II, the MOBILE logic style is described. In Section III, we analyze the two-phase gate-level MOBILE pipelines. In Section IV we describe the circuits which have been designed and fabricated to experimentally validate the proposed pipeline and show experimental results. Finally, some key conclusions are given in Section V.

II. MOBILE LOGIC STYLE

A. MOBILE operating principle

The MOBILE [17] in Fig. 1b is an edge-triggered current controlled gate which consists of two devices exhibiting NDR in their *I-V* characteristic (Fig. 1a), connected in series and driven by a switching bias voltage, V_{CK}. When V_{CK} is low, both NDRs are in the on-state and the circuit is monostable. In-
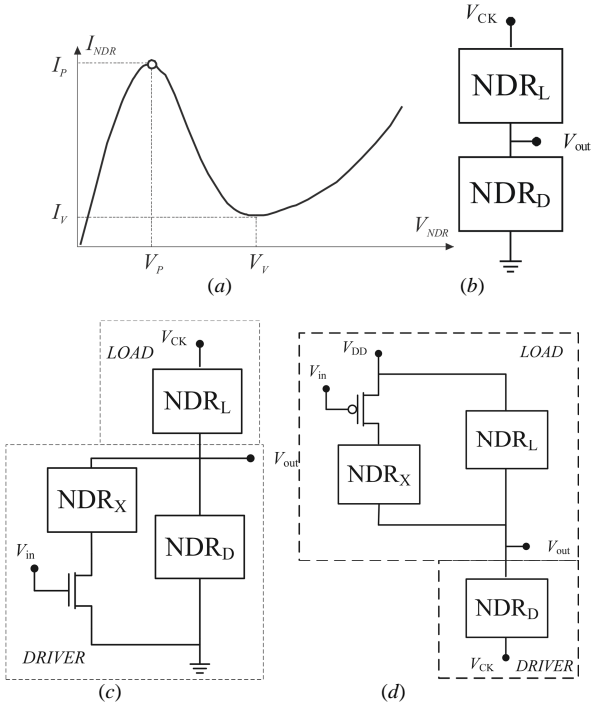
Fig 1. MOBILE circuits. (*a*) NDR *I-V* characteristic. (*b*) Basic MOBILE. (*c*) Rising edge-triggered MOBILE inverter. (*d*) Falling edge-triggered MOBILE inverter.

creasing V_{CK} to an appropriate maximum value ensures that only the device with the lowest peak current switches from the on-state to the off-state. Output is high if the driver NDR switches and low if the load switches. Logic functionality can be achieved if the peak current of one of the NDR devices is controlled by an input. In the configuration of the rising edge-triggered inverter MOBILE shown in Fig. 1c, the peak current of the driver NDR can be modulated using the external input signal V_{in}. The transistor acts as a switch, so that for a low input, current flows only through NDR_D, but for a high input, the effective peak current of the driver is the sum of the peak currents of NDR_D and NDR_X. The inverter topology can be generalized to implement arbitrary functions by just replacing the single transistor in Fig. 1c (or 1d) by a transistor network realizing the target functionality. NDR peak currents are selected such that the value of the output depends on whether the network transistor evaluates to "1" or to "0". Figure 1d depicts a falling edge triggered inverter. Note that branch implementing functionality is now in parallel to the load NDR and uses a p-type transistor.

It is well known that a sufficiently slow rising (or falling) transition of V_{CK} is required for MOBILE operation [18]. That is to say, there is a critical rise time for the switching bias below which the gate does not operate correctly. Under that critical rise time, there is at least one input combination for which the gate does not produce the expected logic output. This is due to AC currents associated with internal parasitics and output capacitive loads (fan-out), which are more important for faster clock changes and which somewhat "alter"

the ideal MOBILE operating principle based on peak currents comparison. This critical value depends on both circuit (NDR peak currents, fan-out …) and technological parameters. Design must therefore take into account these AC currents in order to guarantee the desired relationship between load and driver currents for each input combination when V_{CK} approaches $2V_p$, V_p being the peak voltage of the NDRs (see Fig. 1a).

Rising (falling) edge-triggered MOBILE logic gates evaluate inputs with the rising (falling) edge of the bias voltage and hold the logic level of the output while the bias voltage is high (low), even though the inputs change (self-latching operation [19]). The output returns to zero (to one) with the falling (rising) edge of the clock until the next evaluation. The self-latching operation allows the implementation of gate-level pipelined architectures without extra memory elements [5].

B. MOBILE interconnections

Four phase clock scheme

Originally, cascaded rising edge-triggered MOBILE gates were operated in a pipelined fashion using a four-phase overlapping clocking scheme shown in Fig. 2a [5], [20]. Note that there are four steps in the operation of each MOBILE gate: evaluation (clock rises), hold (clock high), reset (clock falls) and wait (clock low). $V_{CK, i}$ is delayed with respect to $V_{CK, i-1}$ by $T/4$, T being the clock period. In this way the ith stage evaluates (rising edge of $V_{CK, i}$) while the $(i-1)^{th}$ stage is in the hold phase ($V_{CK, i-1}$ high). Four clock signals are enough, since the first phase can be used for the fifth level and so on. In Subsec-
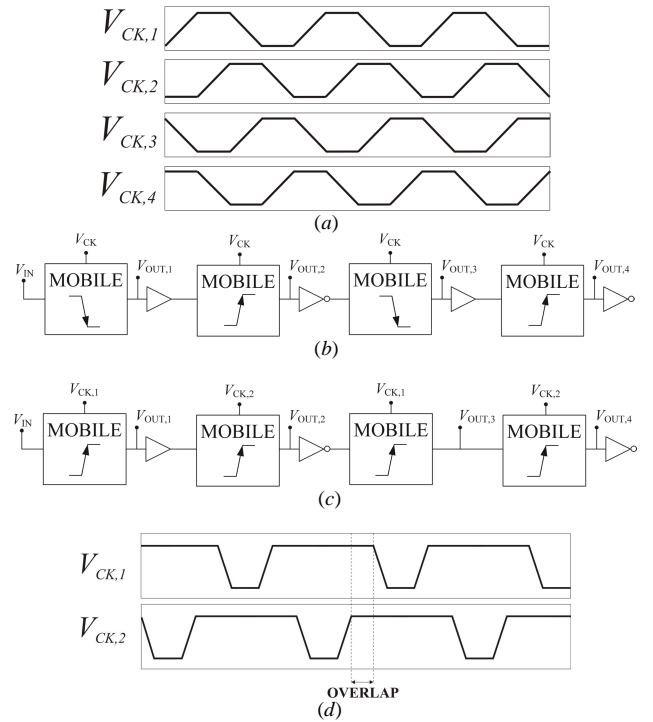

Fig. 2. (a) Four-phase clock scheme. (b) Block diagram of a single-phase clock scheme. (c)-(d) Block diagram and clock waveforms of the two-phase counterpart.

tion A, it was stated that there is a critical rise time below which the gate does not operate correctly. This explains the clock shape with equal rise, high, fall and low times. Thus, for this scheme, the clock cycle is $4T_{EVAL,MAX}$ (operating frequency is $0.25 /T_{EVAL,MAX}$) with $T_{EVAL,MAX}$ being the largest evaluation time required by any gate in the network.

Other simpler clock schemes have been explored in order to reduce the difficulties of distributing four clock signals with tight constraints on their relative delays and to increase throughput, which is limited by the evaluation time of four gates.

Single phase clock scheme
A network of MOBILE-based gates can be operated with a single clocked bias signal if rising edge-triggered gates and falling edge-triggered gates are alternated and latches are added at each stage to eliminate the return-to-reset behavior [21]. However, it has been demonstrated that to ensure correct operation it is not necessary to eliminate return-to-reset behavior [22]. It is enough to keep the output of each MOBILE stage stable until it has been evaluated by the next one. Thus, each latch is replaced by a static inverter. Figure 2b depicts chained MOBILEs implemented with the single-phase architecture. The first and the third gates are rising edge-triggered, whereas the second and the fourth are falling edge-triggered. Note that the role of the inter-gate elements is to guarantee that one MOBILE has already taken the decision about its output before the reset to zero of the previous one reaches its input. The functionality of the inter-gate element is not, therefore, limited to be inverting (note that both inverters and buffers have been used in Fig. 2b), and this makes logic design more flexible. The clock cycle is $2T_{EVAL,MAX}$ (operating frequency is $0.5/T_{EVAL,MAX}$) with $T_{EVAL,MAX}$ being the largest evaluation time required by any stage (MOBILE + static logic) in the network. However, the single-phase solution has two drawbacks. First, negative edge-triggered MOBILEs are used, which requires p-type transistors. This means larger transistors and thus larger parasitic capacitances, which degrade gate speed. Secondly, the only clock skew tolerance mechanism is the delay of the inter-gate element. Both of these problems are overcome by the two-phase scheme described in next Section.

III. ANALYSIS OF TWO-PHASE MOBILE NETWORKS

One alternative solution is to design networks with only positive edge triggered MOBILE gates operated with an overlapping two phase clock scheme as shown in Fig. 2c [23]. Note that inter-gate elements (inverting or non-inverting) can also be added if required by logical (to increase design flexibility), or electrical (for example, efficient handling of large loads) considerations.

The throughput (or frequency) behavior of the single phase scheme is preserved in the sense that it is also determined by the evaluation time of two stages. Also, the proposed two-phase scheme has clear advantages over the one-phase solution since the worse evaluation time is larger for the latter because it uses falling edge gates with PMOS functional networks. Moreover, the overlapping of the two clocks makes it possible to directly connect two MOBILE gates, since the return to reset of one stage takes place after the evaluation of the next stage, and to increase clock skew tolerance - a critical weak point in the single-phase interconnection.

In terms of area, the proposed topology eliminates p-type transistors, which not only leads to area savings but to have smaller input capacitances and, therefore, smaller NDR in previous stages. A reduction in area up to 28% over a single-phase scheme have been obtained in the core of a 4 bit CLA designed in an RTD-CMOS hybrid technology, which leads to a more compact solution even including the area occupied by the two-phase clock generation circuitry.

A comparison with Domino-based counterparts also produces some interesting results. As we mentioned earlier in Section I, Domino based solutions are functionally limited in that they do not allow the implementation of inverting stages. This limitation is due to the fact that dynamic gates evaluate when their clock is high, and might therefore respond to the precharge of their preceding stages. This will occur if the precharge results in a low to high transition of the preceding stage output, since this high value can discharge the dynamic output node. However, there is no response to high to low transitions in the output of the preceding stages. That is why an odd number of inverting static gates are allowed after each dynamic gate, resulting in non inverting stages. More specifically, the basic domino stage comprises a dynamic gate followed by a static inverter. It has been proposed that modifying the topology of the dynamic gate will avoid this limitation, but at the expense of using at least three clock phases [24]. This limitation does not apply to MOBILE pipelines, thanks to the self-latching property of these gates: during clock high (hold), gate inputs can change without affecting the gate output. In this way, a MOBILE stage does not respond to the reset to zero of its driving stages. Since self-latching holds both for high to low and for low to high input transitions, this is true regardless of the number of inversions (none, odd number or pair number) between two consecutive MOBILE gates, and so both inverting and non inverting stages are allowed. This leads to greater flexibility in logic design.

Two-phase domino pipelines also require labor-intensive design due to race-through failure. The fact that there is both an upper and a lower limit on the allowed overlap of the two phases represents a timing challenge which complicates design, and, in many cases, causes latches to be introduced [25], [26]. The lower limit is determined by the fact that it should be long enough for a stage to evaluate before the precharge of the preceding stages driving it reaches its inputs, even under worst case clock skew conditions. In fact, multi-phase overlapped clock schemes are said to be clock skew tolerant because of this overlapping. However, when only two phases are used, evaluation may slip over consecutive stages if the overlap is too long (race-through failure). In Fig. 3, assuming domino stages, stage 2 evaluates when $V_{CK,2}$ is high, and stage 3 could respond to stage 2 output if $V_{CK,1}$ is a high enough time after $V_{CK,2}$ goes high. Stage 3 thus evaluates twice in one clock cycle. This is not normal pipelining behavior. Again, the self-latching property of MOBILE logic blocks eliminates the upper limit. Evaluation is associated to the clock edge, so even if $V_{CK,1}$ is high long after $V_{CK,2}$ goes to high, there is no evaluation because stage 3 does not see a clock edge.
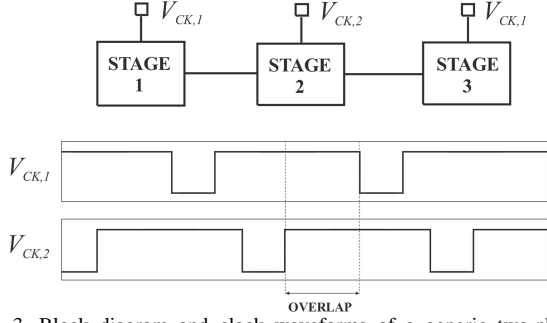
Fig 3. Block diagram and clock waveforms of a generic two-phase interconnection scheme.

IV. EXPERIMENTAL RESULTS

The operation of the two-phase MOBILE gate interconnection scheme has been experimentally validated. As far as we know, this is the first time a working two-phase MOBILE network has been reported.

Two-phase clocked chains of MOBILE inverters have been designed and fabricated. These structures were implemented with MOS-NDR devices (circuits made up of transistors that emulate the NDR I-V characteristic) and the MOBILE gate topology from [14] in a 1.2V/90nm CMOS technology. Figures 4a and 4b depict the schematics of the MOS-NDR device used and a MOBILE inverter implemented with them. The design of MOBILE blocks operating at high frequencies is not straightforward. As was previously mentioned, it is necessary to take into account AC currents associated to parasitic, which may be large at high frequencies. Design validation thus requires accurate modeling of layout parasitics and this is why experimental validation is so important.

Figure 4c depicts the block diagram of one of the fabricated circuits. Each MOBILE stage is an inverter like the one shown in Fig. 4b. As shown in Fig. 4c, a two-phase clock generator has been also included. It provides two non-overlapped clock signals ($V_{CK,1}$ and $V_{CK,2}$) with the same frequency as the master clock (V_{CK}). Note that power clocks are avoided since the clock signal of each MOBILE circuit is applied to the input of a static inverter. The output of this inverter is used as the clock of the MOBILE inverter. In this way, the two overlapped clocks required are generated and the constraints on clock rising time are relaxed. Area overhead for the clocks generator represents 24% of the total of the chain. Note that this percentage would be smaller if this circuit is integrated into more complex networks.

The packaged circuit was tested and shown to operate correctly. Critical input for this kind of circuit is a sequence alternating 0's and 1's in the sense that it limits operating frequency. Figure 4d shows the experimental results when such sequence is applied to the ten-stage pipeline. Waveforms are shown of the master clock, the input (V_{IN}) and the output (V_{OUT}). These were captured using the Agilent DSO6104A oscilloscope. Note that in addition to the package, there are input buffers (for V_{IN} and V_{CK}) and output buffers and pads not shown in Fig. 4. V_{CK} and V_{IN} are 1.2V pulse trains at 400MHz and 200MHz, respectively. As expected, V_{OUT} is a periodical sig-
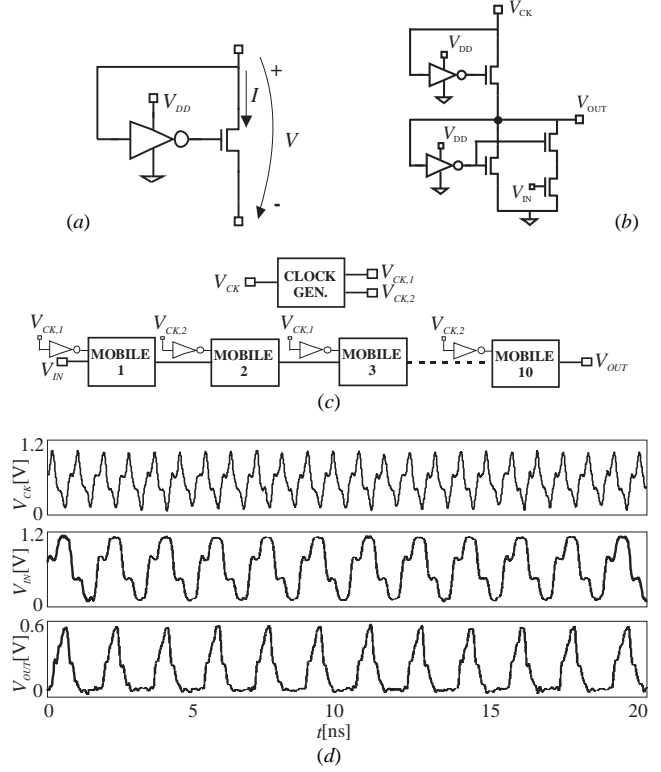

Fig 4. (a) MOS-NDR device. (b) MOBILE inverter implemented with MOS-NDR devices. (c) Block diagram of the fabricated two-phase chain of inverters. (d) Measured waveforms.

nal of the same frequency as the input. The 0101…01 sequence is obtained at the output of the pipeline with a latency of five clock cycles, since data is evaluated twice each V_{CK} cycle. Note the different shapes of V_{IN} and V_{OUT}, due to the return to zero behavior of MOBILE. Results are shown at 400MHz so that the signals are not attenuated by the experimental set-up, but correct operation was observed for this and counterpart circuits incorporating static inverting and non inverting elements between MOBILE gates of over 1GHz, which was the target design frequency considering the available measurement setup. However, simulations of the extracted stand-alone pipelined chain in Fig. 4c exhibits correct behavior up to 2.2 GHz.

We fabricated a variation of the previous chain in which the master clock was distributed as shown in the block diagram of Fig. 5a. The purpose of this experiment is to further validate the operation of the direct connection of MOBILE stages, which is the more critical one in terms of minimum overlap of the clocks of consecutive stages. In this simple configuration this overlap is just the delay introduced by one inverter and thus suits well our target.

Experimental results for this topology are given in Fig. 5b, where V_{CK} and V_{OUT} are the clock and the output and V_{IN} is the input. For this experiment, V_{CK} and V_{IN} are clock pulses at 1.4GHz and 175MHz (one-eight of the frequency of V_{CK}), respectively. Since V_{IN} has a duty cycle of 25%, the output waveform consists of two cycles at high level and six at low level, which is consistent with the expected response to the
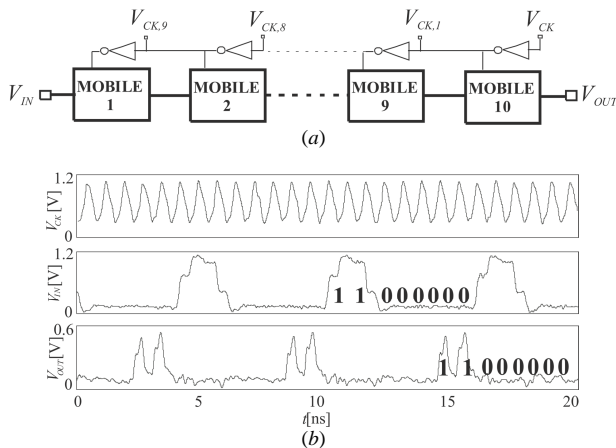
Fig 5. (a) Block diagram of the reverse clock distribution chain of inverters. (b) Experimental waveforms.

input. As previously mentioned, at this frequency attenuation due to the experimental set-up was observed.

V. CONCLUSIONS

The operation of two-phase gate-level pipelines based on the MOBILE operating principle has been experimentally validated. As far as we know, this is the first time a working two-phase MOBILE network has been reported. This interconnection scheme has advantages over other previously reported clock schemes for MOBILE logic networks. It is simpler than the conventional four-phase solution and leads to higher operating frequencies, since only two stages, instead of four, sequentially evaluate in one clock cycle. Unlike one phase schemes, p-type transistors are avoided and clock skew tolerance increases. This is possible due to the self-latching property of MOBILE gates, which make it possible to take advantage of the overlapping of the two clock phases to tolerate clock skew, and also avoids the limitations of conventional CMOS counterparts.

Finally, one additional feature of MOBILE logic blocks is that, unlike other clocked logic styles, they can be operated with sinusoidal clocks. It would therefore be worth exploring their use with energy recovering techniques.

REFERENCES

[1] Friedman, V.; Liu, S., "Dynamic logic CMOS circuits," Solid-State Circuits, IEEE Journal of, vol.19, no.2, pp.263,266, April 1984.

[2] D. Harris and M.A. Horowitz, "Skew-tolerant domino circuits", *IEEE Journal of Solid-State Circuits*, 32(11), pp.1702-1711, Nov. 1997.

[3] R. Hossain, "High Performance ASIC Design", Cambridge, 2008.

[4] S. Horne, D. Glowka, S. McMahon, P. Nixon, M. Seningen and G. Vijayan, "Fast14 Technology: design technology for the automation of multi-gigahertz digital logic", *International Conference on Integrated Circuit Design and Technology*, pp. 165- 173, 2004.

[5] P. Mazumder, S. Kulkarni, M. Bhattacharya, J.P. Sun, and G.I. Haddad, "Digital circuit applications of resonant tunneling devices", *Proc. IEEE*, 86, pp. 664-686, Apr. 1998.

[6] X. Yu, L.-H. Mao, W.-L. Guo, S.-L. Zhang, S. Xie and Y. Chen, "Monostable–Bistable Transition Logic Element Formed by Tunneling Real-Space Transfer Transistors With Negative Differential Resistance", *IEEE Electron Device Letters*, 31(11), pp.1224-1226, Nov. 2010.

[7] G.S. Rose and M.R. Stan, "Memory arrays based on molecular RTD devices", *Third IEEE Conference on Nanotechnology*, 1, pp. 453- 456, Aug. 2003.

[8] S. Choi , Y. Jeong, J. Lee, and K. Yang, "A Novel High-Speed Multiplexing IC Based on Resonant Tunneling Diodes", *IEEE Trans. On Nanotechnology*, 8(4), pp. 482-486, Jul. 2009.

[9] K. Karda, J. Brockman, S. Sutar, A. Seabaugh, and J. Nahas, "Bistable-Body Tunnel SRAM", *IEEE Trans. Nanotechnology*, 9, pp. 1, 2010.

[10] G. S. Rose, H. Manem, J. Rajendran, R. Karri and R. Pino, "Leveraging Memristive Systems in the Construction of Digital Logic Circuits", *Proc. of the IEEE*, DOI:10.1109/JPROC.2011.21674.

[11] J. Núñez, M.J. Avedillo and J.M. Quintana "RTD-CMOS pipelined networks for reduced power consumption", *IEEE Trans. On Nanotechnology*, 10(6), pp. 1217-1220, Nov. 2011.

[12] A. González, , et al., "CMOS implementation of a multiple-valued logic signed-digit full adder based on negative differential resistance devices", *IEEE Journal of Solid State Circuits*, 36, pp. 924-932, 2001.

[13] D. Bol, J.-D. Legat, J.M. Quintana and M.J. Avedillo, "Monostable-Bistable Transition Logic Elements: Threshold Logic vs. Boolean Logic Comparison", *IEEE International Conference on Electronics, Circuits and Systems*, pp. 1049-1052, Dec. 2006.

[14] J. Núñez, M.J. Avedillo and J.M. Quintana, "Efficient Realisation of MOS-NDR Threshold Logic Gates", *IET Electronics Letters*, 45(23), pp. 1158-1160, 2009.

[15] L. Ding and P. Mazumder, "On Circuit Techniques to Improve Noise Immunity of CMOS Dynamic Logic", *IEEE Trans. On VLSI Systems,* 12(9), pp. 910-925, Sept. 2004.

[16] K.-J. Gan, C.-S. Tsai, and D.-S. Liang, "Design and characterization of the negative differential resistance circuits using the CMOS and BiCMOS process", *Analog Integrated Circuit Signal Processing*, 62, pp. 63 – 68, 2010.

[17] T. AKeyoshi, T., et al., "Weighted sum threshold logic operation of MOBILE's (Monostable Bistable Logic Element) using resonant-tunnelling transistors", *IEEE Electron Device Lett.*, 14, pp. 475-477, Oct. 1993.

[18] H. Matsuzaki, H. Fukuyama and T. Enoki: "Analysis of Transient Response and Operating Speed of MOBILE", *IEEE Trans. on Electron Devices*, 51(4), pp. 616-622, April 2004.

[19] M.J. Avedillo, J.M. Quintana and H. Pettenghi, "Self-Latching Operation of MOBILE Circuits using Series-Connection of RTDs and Transistors", *IEEE Trans. on Circuits and Systems-II,* 53(5), pp. 334-338, May 2006.

[20] S. Mohan, et al., "Ultrafast pipelined arithmetic using quantum electronic devices", *Computers and Digital Techniques, IEE Proceedings*, 141(2), pp.104-110, Mar 1994.

[21] H. Pettenghi, M.J. Avedillo and J.M. Quintana, "Single phase clock scheme for MOBILE logic gates", *IEE Electronics Letters*, 42, pp. 1382-1383, 2006.

[22] J. Núñez, M.J. Avedillo and J.M. Quintana, "Simplified single-phase clock scheme for MOBILE networks", *Electronics Letters*, 47(11), pp. 648-650, May 2011.

[23] J. Núñez, M.J. Avedillo and J.M. Quintana, "Domino Inspired MOBILE Networks", *Electronics Letters*, 48(5), Feb, 2012.

[24] R. J.-H. Sung and D. G. Elliott, "Clock-Logic Domino Circuits for High-Speed and Energy-Efficient Microprocessor Pipelines", *IEEE Transactions on Circuits and Systems II*, 54(5), pp. 460-464, May 2007.

[25] J. Sivagnaname, H.C. Ngo, K.J. Nowka, R.K. Montoye and R.B. Brown, "Wide limited switch dynamic logic circuit implementations", *IEEE International Conference on VLSI Design*, 2006.

[26] C.K. Jerry, W.-H. Ma, S. Kim and M. Papaefthymiou, "2.07 GHz floating-point unit with resonant-clock precharge logic", *IEEE Asian Solid State Circuits Conference (A-SSCC)*, pp.1-4, Nov. 2010.