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Diseño Sistemático de Circuitos y Sistemas Analógicos y de Señal Mixta Reconfigurable

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ABSTRACT

During the last decades, there has been an increasing demand of electronic devices, mostly in the field of mobile communications. Every year, hand-held communication devices must include more and more functionalities and support an increasing number of different communication standards in order to satisfy the necessities of nowadays society. In order to be able to answer the market demands, those devices should not increase the area occupation while the power consumption is at reasonable levels and, more importantly, the time-to-market factor must be reduced as much as possible.

In this scenario, reconfigurable analog and mixed-signal circuits are ideal for such requirements, since they are able to reuse the same blocks to work in different operation modes, which increases the hardware-sharing and reduces the total area occupation of the devices. Besides, they can adapt their power consumption dynamically depending on the application demands, increasing the battery life of such devices. However, reconfigurable circuits are even more complex to design than regular ones. Moreover, the available CAD-tools for analog design are far from the level of automatization that is found in the digital domain. Therefore, the use of systematic design methodologies is mandatory to avoid increasing the design time critically.

During the last years, bottom-up methodologies have appeared as promising alternatives of more traditional top-down approaches. These methodologies rely on the use of the Pareto-optimal fronts (PoFs) of the basic building blocks of a complex system, which are a representation of the best achievable trade-offs between the circuit performances. The PoF of the complete system is obtained by composing hierarchically the PoFs of the basic building blocks, from the bottom up to the top-level. This methodology is so advantageous because every design of the PoF at the top-level points to a fully sized design of each one of the lower-level blocks, which help reducing the design time of the system. Besides, the PoFs of basic building blocks can be reused, avoiding the tedious and time-consuming generation of PoFs of low-level blocks every time a different system is considered.

However, there is no reference in the literature illustrating bottom-up methodologies applied to reconfigurable circuits. Adding support for the use of reconfigurable building blocks in these methodologies would mean a huge advance in the field of systematic design methodologies of analog and mixed-signal circuits. Furthermore, the hierarchical composition of PoFs, either for regular or for reconfigurable circuits, presents implementation issues that have not been addressed and that affect directly to the reusability of PoFs.

This thesis aims to contribute to this field by proposing a new design methodology that adds full support to the use of reconfigurable circuits and that solves two important issues related to the hierarchical composition of PoFs and that has not been addressed before. For this, a method to generate PoFs of reconfigurable circuits, which we have called Multi-mode PoFs (mm-PoFs), has been developed. The method is based on the use of a new multi-objective evolutionary algorithm, which is able to optimize the multiple operation modes of the reconfigurable circuits simultaneously. One of the implementation issues of the hierarchical composition of PoFs and mm-Pofs has been solved by introducing a new technique that is able to re-evaluate circuits under different loading conditions without electrical simulation, which improves the reusability of PoFs in the design of different systems. The second issue has been addressed by proposing a new method to efficiently explore efficiently the PoFs of low-level blocks.

The presented design methodology is succesfully applied in the design of two different systems. The first application example is the design of a 0.35-um reconfigurable, continuous-time low-pass active filter that must fulfil specification for GSM and DECT standards. The active filter is implemented using a two-stage topology with reconfigurable folded-cascode, Miller-compensated operational amplifiers. For the generation of the mm-PoF of the filter, mm-PoFs of the reconfigurable amplifiers are hierarchicaly composed. In the second application example, the presented methodology is applied in the design of a 130-nm reconfigurable Sigma-Delta modulator that must fulfil specifications for three different standards: GSM, Bluetooth and UMTS. The integrators of the modulator are implemented using reconfigurable folded-cascode operational amplifiers that are able to operate in four different modes by switching the bias current. For the generation of the mm-PoF of the modulator, mm-PoFs of these reconfigurable amplifiers are hierarchically composed.

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ACRONYMS

AMS Analog and mixed-signal

BT Bluetooth

CD Crowding Distance

CR Cognitive Radio

CS Two-set Coverage Metric

CT Continuous-Time

CV Constraint Violation

DA Digital-to-Analog

DAC Digital-to-Analog Converter

DECT Digital Enhanced Cordless Telecommunications

DNA Deoxyribonucleic Acid

DR Dynamic Range

DVB Digital Video Broadcasting

EA Evolutionary Algorithm

ENOB Effective Number of Bits

GB Gain-Bandwidth

GPS Global Positioning System

GSM Global System for Mobile Communications

IC Integrated Circuit

IoT Internet Of Things

IP Intelectual Property

LP Low-Pass

LSB Least Significant Bits

MOBU Multi-Objective Bottom-Up

MOEA Multi-Objective Evolutionary Algorithm

mm-PoF Multi-mode Pareto-optimal Front

MiM Metal-Insulator-Metal

MOOP Multi-Objective Optimization Problem

M^{3}OOP Multi-mode Multi-Objective Optimization Property

NTF Noise Transfer Function

OPAMP Operational Amplifier

OSR Oversampling Ratio

PGA Programmable-Gain Amplifier

PLL Phase-locked Loop

PM Phase-Margin

PoF Pareto-optimal Front

P$_{CN}$ In-band Error Power due to Circuit Noise

P$_{Q}$ In-band Quantization Error Power

P$_{st}$ Power due to the Integrator Defective Settling

RF Radio Frequency

SC Switched-Capacitor

SINC signal shaping and interpolation

SMS Sort Message Services

SNDR Signal-to-noise plus Distortion Ratio

SoC System-On-Chip

UMTS Universal Mobile Telecommunications System

WCDMA Wideband Code Division Multiple Access

WiMAX Worldwide Interoperability for Microwave Access

WLAN Wireless Local Area Network

WMAN Wireless Metropolitan Area Networking

1 INTRODUCTION

1.1 CMOS TECHNOLOGY OVERVIEW

Since the invention of the first point-contact transistor by John Bardeen, William Shockley and Walter Brattain at Bell's Labs in 1947, for which they were awarded the Nobel Prize in Physics in 1956, the electronics industry have experimented an unstoppable advance in the number of transistors and the complexity of electronic systems.

In 1965, just six years after the first planar Integrated Circuit (IC) was manufactured, Gordon E. Moore predicted that the number of transistors that could be included in a chip without increasing the fabrication cost per transistor would be increased at a factor of 2 per year [1]. Ten years later he modified his predictions stating that the increment rate would be of 2 every 2 years [2]. Whether if these were good predictions or the fact that electronic industry has used them as a goal to achieve, the fact is that the predicted trend has been fulfilled so far, and the semiconductor industry has evolved from the invention of the transistor to manufacture complete System-on-Chips (SoC), including digital, analog, mixed-signal and RF functions on a single chip substrate. As an illustration of this evolution, Fig.1.1 shows the number of transistors of Intel processors, from the first that appeared in 1970 until the last generation that hit the market in 2016.

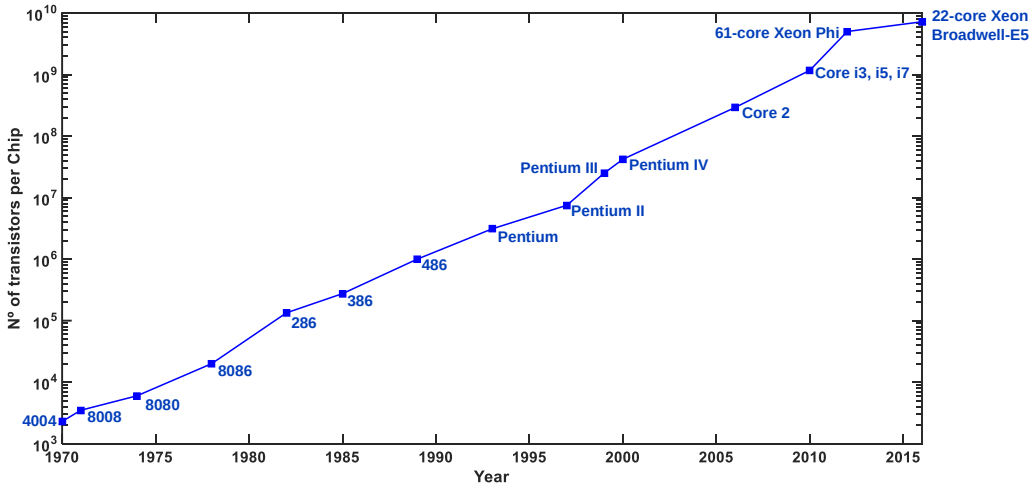


Figure 1.1: Increment of the number of transistors in the Intel processors.

Today, advances in microelectronics have gone beyond Moore's predictions and many aspects of our society are in the middle of a revolution. Every year new achievements are made in the field of wireless communication systems, which has led to a succession of generations of mobile communication devices. The early first generation, known as 1G, was based on analog modulation schemes. It was followed by the second generation, 2G, which was based on digital modulation schemes and added short message services (SMS). Later, with the development of the third generation, 3G, the functionalities of mobile phones were expanded, turning them into multimedia electronic devices: featuring digital video cameras, multimedia players, short-range connectivity to other electronic devices and broad band connectivity to the Internet with data rates of up to 2Mb/s using the UMTS/WCDMA standard. Today, the fourth generation, 4*G*, includes services such as global positioning system (GPS), digital video broadcasting (DVB) and support for most extended wireless networks (WMAN, WiMAX, WLAN) as well as wide-band connectivity for media content [3]. This allows using today's hand-held devices for different applications such as communication, entertainment and media in a world where everybody is connected through the Internet in a new paradigm that has arisen, known as the Internet Of Things (IoT) [4]. Beyond communication and entertainment, these advances are allowing the development of new applications in important fields like medical healthcare [5,6] and automotive security [7].

In this unstoppable trend, the new electronic devices are required not only to improve their performances for a given communication standard, but also to be able to switch automatically between different networks, operating correctly for different communication standards with different bandwidth requirements [8–14]. These requirements have redefined the concept of wireless hand-held mobile terminals from a purely hardware device to what is known as Software-defined radio, which bases its operation in a combination of hardware and software [15–19]. Other proposals go beyond this concept, to what is known as Cognitive Radio (CR) [17,20]. This new technology allows both wireless networks and mobile devices to use dynamically the RF spectrum. As a result, a better use of the spectrum, with a lower interference level and lower power consumption, is achieved. However, the transceivers of these devices must be flexible enough, both in software and hardware terms, as to adapt and reconfigure themselves according to their spectral environment [21,22].

Including more and more features within the same device, such as support for multiple communication standards and reconfiguration capabilities, implies that the complexity and the power requirements of the electronic circuits that make all this possible are constantly increasing. In this scenario, it is clear that it is of the greatest importance to be able to develop flexible and reconfigurable transceivers, able to adapt their power consumption dynamically [23].

Furthermore, if designers want to follow this rapid evolution of technological advances and meet the demands of the society, the use of efficient design methodologies and automation design tools will play a key role in order to provide the new required transceivers in adequate design time. The term design methodology loosely makes reference to the use of a systematic flow of design, where some steps can be automated with the use of specific tools. Of course, achieving this is something that requires a lot of investment, both in development time and money. However, it can be beneficial in the long-term, improving the productivity of designers and allowing to face the challenge of the ever increasing complexity of today's analog and mixed-signal systems [24–26]. There is still a lot of work to do in order to reach the level of systematization in the arena of digital integrated circuits, where most of the design processes are automated with the use of numerous commercial tools. This has been made possible in part by the very nature of digital operations, which can be easily transformed into logic operations. Analog design, in the other end, still relies heavily on the knowledge of expert designers and most of the design processes have to be made manually, with multiple tweaks to not only accomplish first-order performances but to overcome second-order non-desirable effects. As a result, in complex mixed-signal systems, most of the design time is spent in the analog part, even though it constitutes only a small fraction of the total system. Solutions for the automation of different processes of the analog design have been proposed in the last decades. Design techniques with automatic layout placement and routing have been presented [27–30]. Other design methodologies are being proposed that let the designer interact with the design tool at some or any phase of the process [31]. Even there are proposal towards the development of systematic design methodologies of analog IP-blocks [32]. The idea is that basic analog circuits could be taken directly from a pre-designed IP-library, increasing the re-usability of these circuits and reducing the number of transistors the designer has to worry about.

The work presented in this Thesis is a contribution in the field of **systematic design of reconfigurable analog circuits**. In a few words, a reconfigurable circuit is able to provide different performances by changing dynamically some of its constitutive elements. Each configuration of the circuit is known as an operation mode. These concepts will be explained in more detail later on. The methodology presented here is the first approach that fully support the systematic optimization of reconfigurable circuits. It is able to cope with the multi-mode operation of such circuits, optimizing simultaneously the multiple sets of performances of each mode. Besides, this methodology is not only aimed for simple blocks, such as amplifiers or comparators, but it also provides efficient mechanisms for the design of more complex circuits, like reconfigurable active filters or modulators. A brief description of optimization methods for analog circuits, both traditional and emerging solutions, that have been proposed over the last decade, is detailed in the

following lines. This will serve as a starting point to understand the challenges of developing a design methodology for reconfigurable circuits.

1.2 SYSTEMATIC DESIGN TECHNIQUES FOR ANALOG AND MIXED-SIGNAL CIRCUITS

In any analog design problem, designers usually begin by evaluating the specifications the circuit must fulfill. According to these, some candidate topologies can be considered and, after one of them has been selected, the circuit is designed as a whole. This is known as flat design, and it works fine as long as the circuits are simple enough, with tens of transistors. However, for more complex systems, such as an analog-to-digital converter (e.g., a $\Sigma\Delta$ modulator), this is not affordable. In these cases, what is done is to decompose hierarchically the system into its constitutive building blocks, as shown in Fig.1.2.

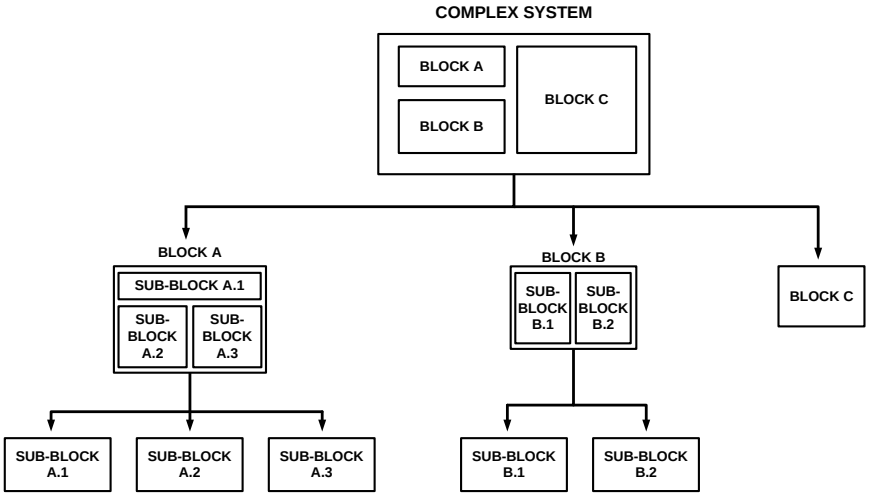


Figure 1.2: Hierarchical decomposition of a complex system into its constitutive building blocks.

The hierarchical design methodologies can be classified according to the flow of design. First, the **Top-down design flow**, which starts at the top-level of the hierarchy and, consecutively, designs each lower-level building block for specifications that are estimated at the immediate higher-level of the hierarchy [33–36]. This design flow is used by most traditional approaches. However, it shows several problems that may negatively impact the work flow (either increasing the design time or making it difficult to arrive to the best solution). First, specifications of low-level building blocks are estimated at early stages of the design process. It may happen that later when designing these blocks, those specifications are

impossible to meet. This requires to repeat the design process using more relaxed specifications for that building block. Second, it may occur that, even after all building blocks have been successfully designed, when the system is verified at the top-level, it does not meet the required specifications because of some low-level details that were not taken into account at earlier stages of the design process. This requires, once again, to repeat the design cycle. Finally, there is the possibility that, although the system is finally verified successfully, it will probably be a sub-optimal design in terms of area and power consumption due to over-design of some of the building blocks, that is, increasing the power consumption or the area of some building blocks in order to meet the specifications.

Alternatively, a bottom-up design flow constructs the system starting with the most basic building blocks, which are at the bottom-level of the hierarchy. These blocks are designed to obtain their feasibility information, that is, the whole **feasible performance space** of the blocks. This concept can be defined as:

- **Feasible performance space:** the set of all possible performances a circuit is able to achieve, for a given topology (a particular arrangement of a number of devices and its interconnections), by varying the values of its design variables.

An illustration is depicted for a simple bi-dimensional case in Fig.1.3, where all possible values of gain and bandwidth an operational amplifier can provide are shown. Each set of values can be obtained for a given configuration of the design variables of the amplifier, that is, the size of the transistors, bias voltages and currents and the values of passive devices such as resistors and capacitors.

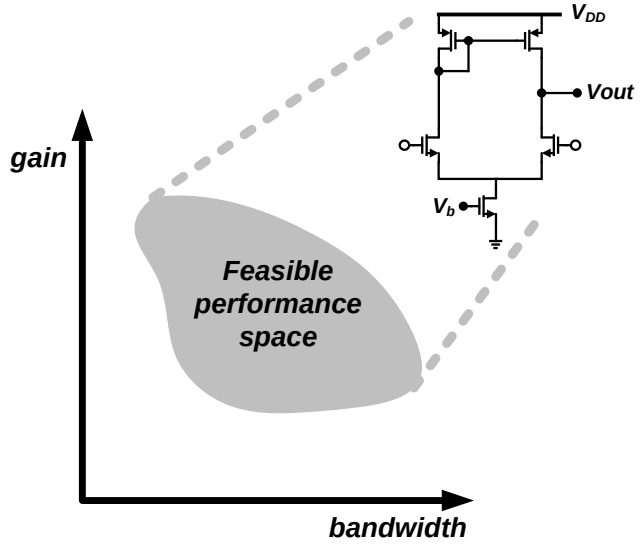


Figure 1.3: Feasible performance space of an operational amplifier.

Afterwards, this feasibility information can be composed hierarchically to obtain that of the blocks that are in higher levels of the hierarchy. The problem of this method is that the generation of the feasibility information of each block of the hierarchy is an expensive and inefficient process. Therefore, a method to simplify the problem is necessary.

In particular, the MOBU methodology (Multi-objective Bottom-up) proposes using the Pareto-optimal Fronts (PoF) of the circuits instead of the whole feasible performance space [37]. The concept of Pareto-optimal Front (PoF) of an electronic circuit is defined as:

- **Pareto-optimal Front:** the set of all possible designs of an electronic circuit that altogether represent the best achievable trade-offs between the set of performances that are considered. All designs that form a PoF are non-dominated between them, that is, any individual is not better than any other in all the performances simultaneously. This is also known as Pareto optimality, or Pareto dominance criterion.

The concept of Pareto optimality was proposed by V. Pareto in [38] and it states that in a group of individuals that are Pareto-optimal, it is impossible to improve any individual without worsening other. An example of a PoF is shown in Fig.1.4, where the trade-off between the area and power consumption of a hypothetical circuit is represented. As it can be seen, the PoF is a continuous region of the performance space, formed by a huge, even infinite, number of solutions. Obtaining that set as such would be as unaffordable as obtaining the whole feasible performance space. What can be done instead is to look for a set of samples that properly represent that region.

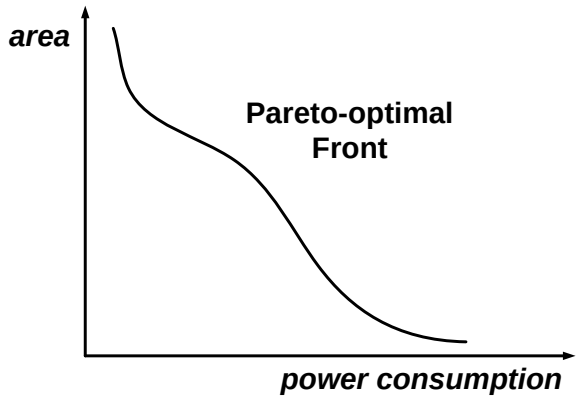


Figure 1.4: Trade-off between the area and the power consumption of an hypothetical circuit.

This can be done in several different ways, the most efficient of them involving the use of some type of optimization algorithm. Optimization algorithms can be divided in two basic classes: deterministic and probabilistic algorithms [39]. Deterministic algorithms show a faster convergence to the nearest local minimum and thus require establishing the starting point adequately. Probabilistic algorithms, on the other hand, introduce heuristic mechanisms and are less susceptible to the starting point. In general, it can be said that the probability of finding the global optimum is higher using probabilistic algorithms. An important family of probabilistic algorithms are Monte-Carlo algorithms [40], among which there are approaches based on physical processes, like for example Simulated Annealing algorithms [41]. On the other hand, there are Evolutionary Computation approaches, which take inspiration from the processes involved in natural evolution and work with a set of individuals that compete to find the best solutions. The work developed in this Thesis is based on the use of Evolutionary Algorithms for the optimization of electronic circuits.

Whether a deterministic or probabilistic algorithm is used, an approximation to the PoF can be obtained by either applying a single-objective or a multi-objective optimization algorithm. In order to understand the difference between these two approaches, let us consider an example where a hypothetical circuit must be optimized to minimize the power consumption and the area. Using single-objective optimization requires transforming the multi-objective problem into a single-objective one by using a weight function that involves both the power consumption and the area, as shown in the following equation:

$$f(\vec{x}) = w_1 \cdot power(\vec{x}) + w_2 \cdot area(\vec{x}) \tag{1.1}$$

where $\vec{x}$ is the set of design variables of the circuit such as transistor sizes or the values of resistors and capacitors. For given values of weights w_1 and w_2, a point of the PoF will be obtained. Each combination of weights will provide a different point. Varying these weights, we can obtain a sufficiently spread sampling of the PoF region, as depicted in Fig.1.5.

The drawback of this approach is that it is an expensive process because a different optimization is required to obtain each sample of the PoF. For this reason, a more efficient method is based on the use of a multi-objective optimizer that allows to obtain multiple points of the PoF in a single run. Among multi-objective optimizers are Multi-Objective Evolutionary Algorithms (MOEAs), which appeared in the late nineties [42]. As said before, evolutionary algorithms take inspiration from natural evolution. Based on the use of a finite population of individuals, MOEAs evolve that population through an iterative process for a number of generations. As in natural selection, MOEAs use crossover and mutation operators that act on the set of design variables of the individuals, like mutation

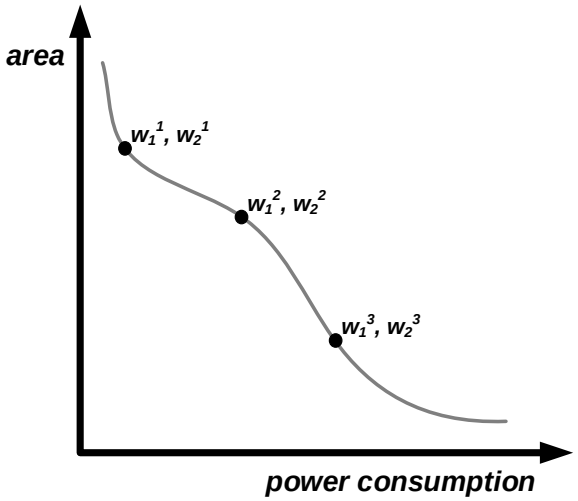


Figure 1.5: Sampling points of the PoF.

occurs in nature in the DNA of cells. In the case of an electronic circuit, the set of design variables, or chromosome, is formed by the set of variables that define the performances of the circuit, such as transistors sizes or the values of resistors or capacitors. By doing so, new and, sometimes, better individuals are found that replace the old ones and survive to be part of the next generation of the evolutionary process. In this way, the individuals of the population will be better after each generation, as depicted in Fig.1.6.

Besides the inherent issues regarding the complex generation of PoFs, there are, still, open issues in Bottom-up design methodologies regarding the hierarchical composition of PoFs. One of them is related to the dependency of some performances of analog circuits to their surrounding circuitry. The second is related to how the PoFs of lower-level blocks can be integrated and explored during the generation of the PoFs of higher-level blocks. Despite of their impact on the efficiency of bottom-up methodologies based on the use of PoFs, an efficient solution or detailed study regarding these problems has not been published yet in the literature.

Now that the main aspects of emerging design methodologies for analog circuits have been described, we can move forward to the development of a design methodology for reconfigurable circuits, which is the main contribution of this work. For this, first the main characteristics of reconfigurable circuits are detailed in the next section.

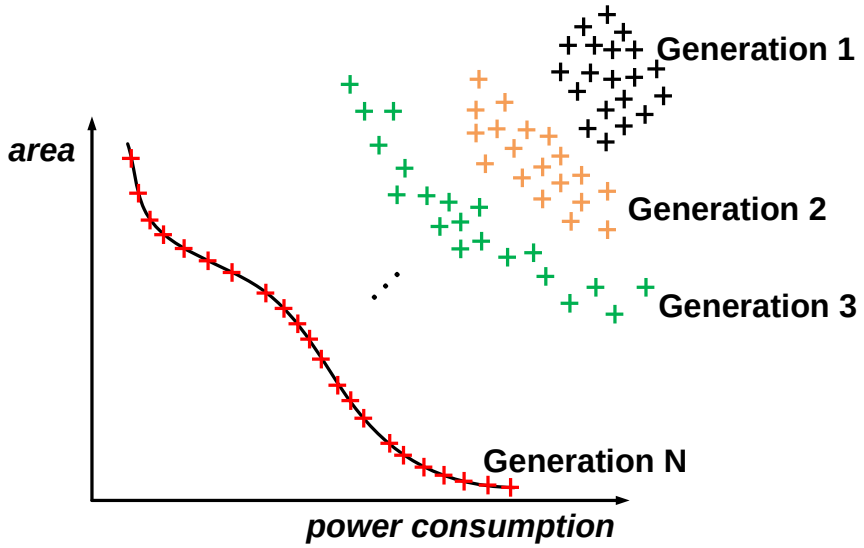


Figure 1.6: Evolution of a population of designs.

1.3 RECONFIGURABLE ANALOG CIRCUITS

As said above, reconfigurable circuits play an important role in current generations of communication systems. Their ability to provide different sets of performances by varying dynamically one or several of its design variables results quite advantageous in multi-standard communication scenarios [43, 44]. For example, these circuits allow reducing the area by promoting the amount of shared area since the same circuit can be used for different operational modes of the system. Besides, they exhibit power adaptation capabilities that allow reducing the power consumption by switching to economic modes for the least demanding applications. The main characteristics of reconfigurable circuits, as well as the definition of several concepts that will be used in this work, are detailed in the following lines:

- **Reconfigurable Circuit:** An electronic circuit that is able to change its performances by changing, dynamically, one or several of its design variables.
- **Operation Mode:** Each one of the different sets of performances a reconfigurable circuit is able to provide.

Reconfiguration Strategy and **Reconfiguration Directive** are two concepts related to how the reconfiguration is carried out and how it changes between operation modes. These concepts will be used quite frequently in this Thesis and their definition is provided in the following lines:

- **Reconfiguration Strategy:** it refers to the changes in a reconfigurable circuit so that it provides different sets of performances. For example, an operational amplifier can change the value of the bias current to provide different bandwidths.
- **Reconfiguration Directive:** it refers to how the reconfiguration strategy is performed. For example, the bias current of the operational amplifier may double or triple its value to increase the bandwidth.

An illustrative example is depicted in Fig.1.7. It is an active low-pass filter that provides different attenuation frequencies by changing the values of its passive network. Thus, in this case the reconfiguration strategy is to change the values of the passive network. By doing so, not only the frequency response of the filter is changed, but also the power consumption. The reconfiguration directive is how the passive network is changed between operation modes.

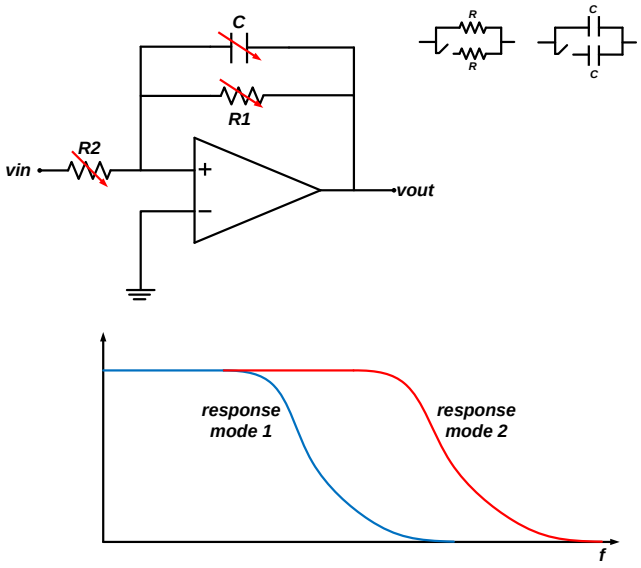


Figure 1.7: Reconfigurable low-pass filter that can change the attenuation band by changing the values of its passive devices.

Beyond the simple variation of the passive network, the operational amplifier provides another degree of freedom since its specifications may also be different for each operation mode of the filter. Therefore, another reconfiguration strategy would be to change the performances of the operational amplifier for each mode of the filter so that the power consumption of the less demanding mode is reduced. The reconfiguration directive in this case could be to use different amplifiers for each mode or to use a reconfigurable amplifier so that the savings in the

power consumption does not imply a significant increase of the area. Of course, reconfiguration strategies and directives of different circuit components can be combined. In this example, we could change the passive network of the filter and simultaneously change the performances of the amplifier either by using different amplifiers or by using a reconfigurable amplifier.

It is important to note here that reconfigurable systems are important not only in integrated circuits but also in many other applications. For instance, the design of reconfigurable antennas [45–47], the design of reconfigurable manufacturing systems [48, 49] or applications in the field of real-time video processing where multi-mode operation is also advantageous [50]. Once the main aspects of reconfigurable circuits have been stated, the next step is to discuss how a design methodology should give support to the design of such circuits.

1.4 A DESIGN METHODOLOGY FOR RECONFIGURABLE ANALOG CIRCUITS

Although the advantages of reconfigurable analog circuits in many scenarios are clear, emerging design methodologies have not yet supported their use. To make this possible, it is necessary to develop and provide tools and methods to systematically optimize these circuits, considering their multi-mode nature. If we go back to the multi-objective optimizations methods, instead of a set of conflicting design objectives, reconfigurable circuits are characterized by multiple sets of design objectives, each one corresponding to one of their operation modes. This means that, whatever the used method to optimize these circuits, it must be able to optimize, simultaneously and independently, the multiple sets of design objectives. This, at the best of our knowledge, is something that has not been reported before. In this Thesis, a new evolutionary optimization strategy has been developed to solve the new type of multi-objective optimization problem that reconfigurable systems pose. We have called these problems Multi-Mode Multi-Objective Optimization Problems (M^3OOPs). Using the new evolutionary algorithm, the PoFs of reconfigurable analog circuits can be obtained, called multi-mode PoFs (mm-PoFs) [51]:

- **Multi-Mode Pareto-optimal Front:** Pareto-optimal front of a reconfigurable circuit, formed by the Pareto-fronts of each of its operation modes.

Fig.1.8 depicts an illustrative example of a mm-PoF of a reconfigurable circuit. As it can be seen, each solution of the mm-PoF is formed by the set of its operation modes. We have called solutions of mm-PoFs twin solutions, or twin designs, as we are focusing here on designs of electronic circuits:

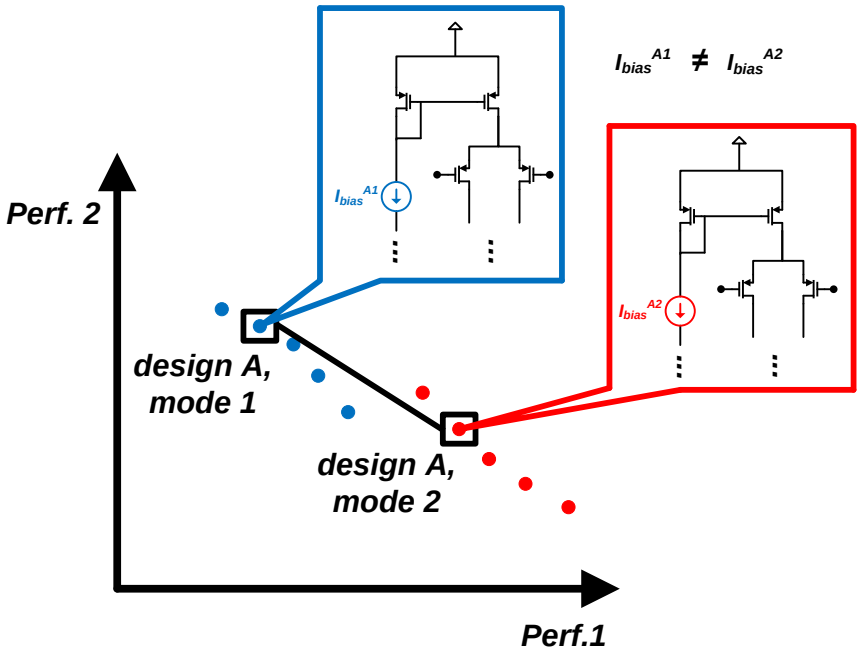


Figure 1.8: Example of a Multi-mode Pareto-optimal Front.

- **Twin designs:** the set of circuit designs that implement each operation mode of a reconfigurable circuit and that only differ in the values of the reconfiguration variables.[1]

As it will be explained in Chapter 3 of this Thesis, to be able to generate a mm-PoF it is necessary to define a new type of Pareto-dominance criterion. Besides, another important aspect of bottom-up design methodologies based on the use of PoFs is that these must be hierarchically composed. This is something that, to the best of our knowledge, has received little attention in the literature. It presents some serious implementation issues that basically refers, on the one hand, to the dependency of analog circuits with their surrounding circuitry, and on the other, with how PoFs of low-level building blocks can be included in the design space of higher and more complex blocks of the hierarchy. Furthermore, the hierarchical composition of PoFs must allow the use of mm-PoFs of reconfigurable blocks. These problems have been addressed in this Thesis and efficient solutions have been established for them. Chapter 4 is dedicated to these issues.

1 Equivalently, triplet designs correspond to 3 modes, quadruplet designs to 4, and so on. Nevertheless, for the sake of simplicity, we will use the term *twin* to refer to any number of operation modes

1.5 OUTLINE OF THIS DISSERTATION

A complete description of the methodology presented in this Thesis is given in Chapter 2. From a structural point of view, all aspects of the methodology are detailed: the developed optimizer, necessary to generate the PoFs and mm-PoFs of circuits; the hierarchical decomposition of complex systems and the later composition of PoFs and mm-PoFs, giving also details about the solutions that have been established for the implementation issues of this hierarchical composition.

Chapter 3 is dedicated to give a detailed description of the new evolutionary algorithm that has been developed to generate multi-mode PoFs of reconfigurable circuits, which is one of the fundamental pillars of this work. It gives a complete description of the basics of any evolutionary algorithm, focusing later on the details of NSGA-II, which has been used as inspiration for the EA developed in this work. After the description of the new EA developed here, the generation of the mm-PoF of an operational amplifier is used as demonstration vehicle. Finally, an example is considered to show the advantages of the use of reconfigurable circuits in multi-standard scenarios.

Chapter 4 focuses on the hierarchical composition of PoFs and mm-PoFs and goes through two key implementation issues of this aspect of the methodology. In this Thesis, and for the first time, new and efficient solutions are proposed for both problems and their validity is demonstrated with experimental results.

Finally, the presented design methodology is validated through the design of two important blocks, present in the design of any communication system. The first is a reconfigurable continuous-time low-pass active filter, whose mm-PoF is generated by hierarchical composition of mm-PoFs of reconfigurable operational amplifiers. Second, the generation of the mm-PoF of a reconfigurable $\Sigma\Delta$ modulator is considered. In this last experiment, different reconfiguration directives are explored so that the best option can be distinguished. The results of these design processes are detailed in chapters 5 and 6, respectively. All steps of the methodology are covered in these examples, from the generation of PoFs and mm-PoFs of basic building blocks to the hierarchical composition of fronts, and the final generation of the mm-PoFs at the system level.

2

MULTI-MODE MULTI-OBJECTIVE BOTTOM-UP DESIGN METHODOLOGY

The design process of this methodology can be divided in three different parts. First, a hierarchical decomposition of the system into its constitutive building blocks, from the system or top-level down to the bottom level. Second, the generation of the PoFs and the mm-PoFs of basic building blocks at the bottom level of the hierarchy. And finally, the hierarchical composition of the generated PoFs and mm-PoFs, from the bottom level up to the top-level. In this Chapter, first an overview of the complete methodology is presented and afterwards each one of these three parts is explained in detail.

2.1 METHODOLOGY OVERVIEW

Every system design begins with a set of specifications the system must fulfill. These specifications are then transformed into specifications for every building block of the system. A traditional top-down approach of this mapping of specifications is depicted in Fig.2.1. As it can be seen, at each hierarchical level, the blocks specifications are established according to those of the immediate higher-level blocks. After each block at every level has been sized, a bottom-up verification of the performances of all blocks is done, up to system level. If the system fulfills the required specifications, the design process continues to the layout-level design. If the system does not fulfill the required specifications, the low-level block specifications must be re-evaluated and the design process must be repeated. On the other hand, even when the system does fulfill the required specifications, the design may be totally suboptimal. The reason is that, due to an inefficient transmission of specifications, low-level blocks might be over-designed, increasing unnecessarily the power consumption or the area of the system. The problem is accentuated in the case of reconfigurable systems, where low-level blocks must be able to switch dynamically between several sets of performances.

The methodology presented in this Thesis proposes to alleviate these problems by using new hierarchical optimization mechanisms. Besides, a new optimization technique is presented that allows performing multi-mode optimization of low-level reconfigurable blocks. The conceptual representation of this methodology is depicted in Fig.2.2. As it can be seen, on the one hand, the system is decomposed into lower-level blocks. This process is repeated for each sub-block of the lower levels until the bottom-level is reached. On the other hand, the relevant feasibility

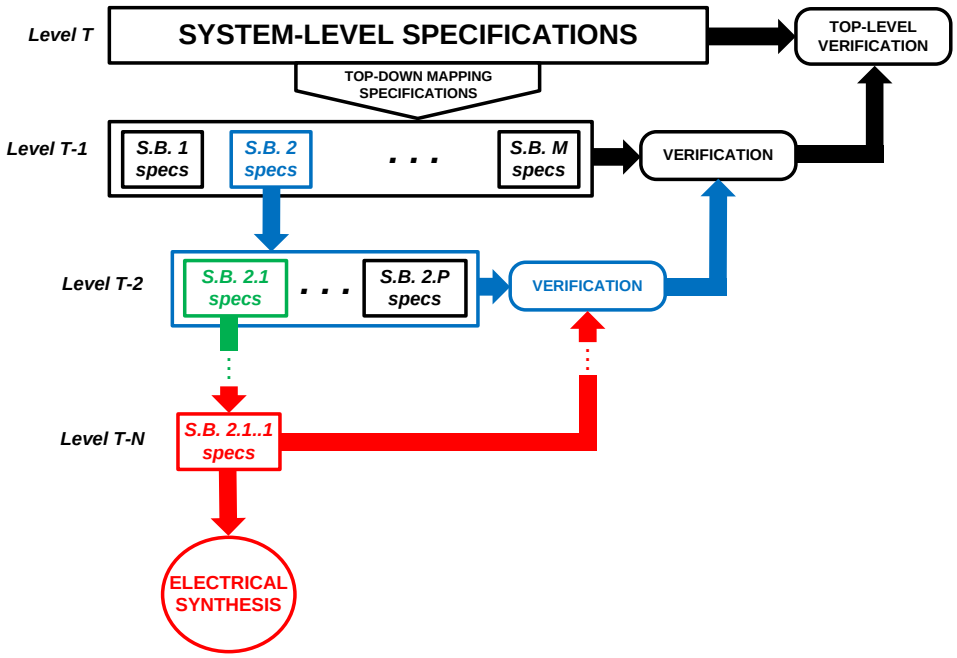


Figure 2.1: Traditional top-down design process.

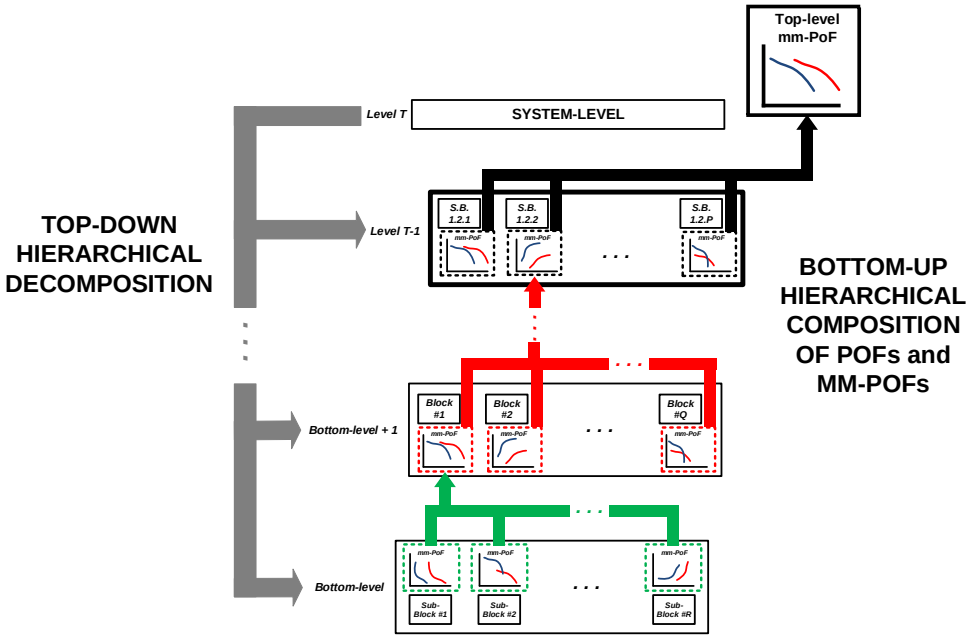


Figure 2.2: Multi-mode multi-objective bottom-up methodology (mm-MOBU).

information of the bottom-level blocks is hierarchically composed up through the hierarchy, from the bottom-level up to the top-level. The feasibility information of the blocks is given in the form of Pareto-optimal Fronts (PoF), or multi-mode PoFs in the case of reconfigurable blocks. As it has already been explained in the first Chapter, the PoF of a circuit is the set of all its possible designs that, altogether, represent the best achievable trade-offs between the conflicting circuit performances. It also provides information about reconfiguration capabilities in the case of mm-PoFs of reconfigurable circuits. The bottom-up hierarchical composition of PoFs and mm-PoFs can go up to the system-level. By doing so, once the system-level PoF is obtained, we are sure that all the designs that form that PoF fulfill the system-level specifications. As stated above, this methodology avoids the main limitations of traditional top-down approaches. First, by using the PoFs and mm-PoFs, we avoid estimating infeasible block specifications. Second, by composing the PoFs of the blocks up to the system-level we ensure that the designs obtained at the end of the process that form the system-level PoF or mm-PoF fulfill the system specifications and, also important, they are optimal designs. Every aspect involved in this design process will be detailed in this Chapter.

2.2 HIERARCHICAL DECOMPOSITION OF THE SYSTEM

At this first stage of the design methodology, the system is hierarchically decomposed into its constitutive building-blocks. An example is shown in Fig.2.3, where a hypothetical system is decomposed in the more commonly considered levels according to reported methodologies [33] [24]. These levels are:

- **Subsystem level**, where, for example, an analog and mixed-signal system (AMS) can be separated into a digital and an analog independent subsystems.
- **Module level**, formed by standalone blocks with robust interfaces that can be clearly distinguished from their environment. Examples of blocks that can be placed at this level are modulators, PLLs or filters.
- **Cell level**, where the blocks perform basic operations. Examples of blocks at the cell level are amplifiers, comparators or switches.
- **Device level**, formed by the most basic elements such as resistors, capacitors or transistors.

According to this hierarchy, the top-level is at the system level. However, as in any AMS system the analog and digital parts are usually independent, the sub-system level can be considered as the top-level in most design problems, and that will be the case in the designs that will be considered in this Thesis. In the same way, the

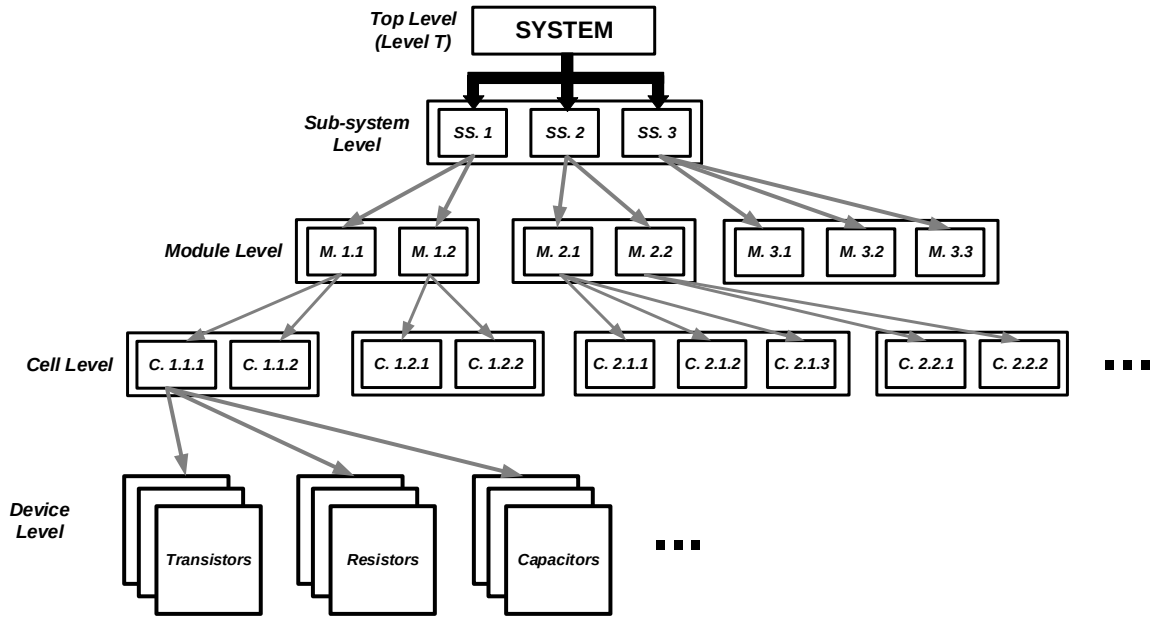


Figure 2.3: Top-down hierarchical decomposition, from system level to cell level.

cell level can be considered as the bottom level in most cases, since the blocks at the device level, such as transistor or capacitors, are usually taken from libraries and their design is not part of the circuit designer problems.

2.3 GENERATION OF POFS AND MM-POFS

The PoFs and mm-PoFs of the building blocks of the system are the cornerstone of this methodology. As it has already been explained, the PoF of a block is a representation of the best achievable trade-offs between the conflictive performances of that block. The example shown in Fig.2.4 depicts the PoF between the area and the power consumption of a differential amplifier. As it is shown, the PoF is formed by a set of different designs of the amplifier, each one with different values of the design variables, which are, among others, the size of the input transistors.

In the case of mm-PoFs, each design is represented by a set of different operation modes and each mode provides a different set of performances. A conceptual example is shown in Fig.2.5, where the mm-PoF of area and power consumption of another amplifier is depicted. As it can be seen, each design is formed by each one of its operation modes. As it is also shown in the figure, the different operation modes of a design are obtained by changing the value of its bias current. As it

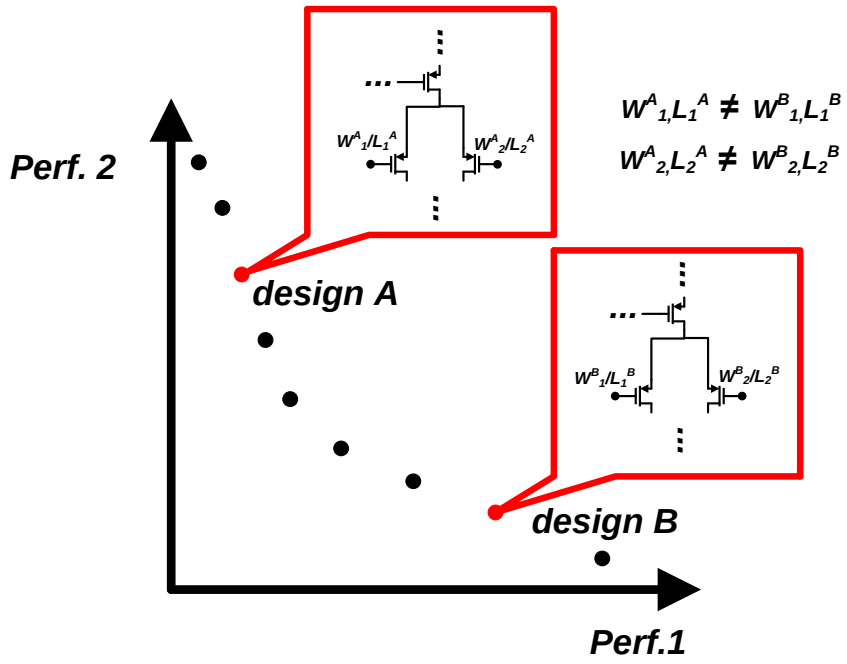


Figure 2.4: Example of a Pareto-optimal front.

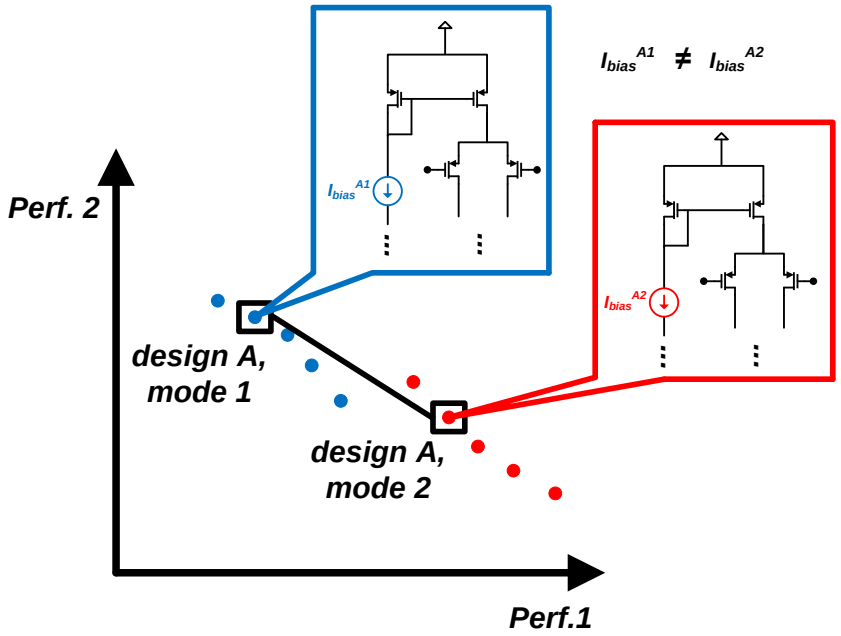


Figure 2.5: Example of a multi-mode Pareto-optimal front.

is explained in Chapter 1, this is known as the reconfiguration strategy, which establishes what changes in the circuit to provide different performances. In the example shown in the figure, the reconfiguration directive is to double the value of the bias current for the second operation mode of the amplifier.

The problem of generating mm-PoFs of reconfigurable circuits is something that has never been considered and, thus, the maths of such optimization problem have not been formulated before. This work introduces the first evolutionary algorithm capable to solve such problems. The algorithm has been developed to perform the optimization of the different operation modes of reconfigurable circuits simultaneously. A detailed description of this new evolutionary algorithm is given in Chapter 3. Here, we will only focus on how the MOEA is used and it is enough to remember that, as explained in Chapter 1, MOEAs work with a population of individuals that evolves during a number of generations. At each generation, the individuals compete between them to generate new individuals, and only the best are preserved for the next generation of the process. Thus, in this process, the MOEA must be coupled to an evaluator, which is responsible for obtaining the values of the design objectives and constraints of each individual and that are used to decide if an individual is better than another. Depending on the abstraction level, the evaluator will be an electrical simulator like HSPICE® or Cadence Spectre®, or higher-level simulators, e.g., based on Matlab SIMULINK®. The concept of the coupling between the evaluator and the optimizer is depicted in Fig.2.6. The MOEA, which is the optimizer, sends the design variables of each individual to the evaluator, which afterwards returns the performances and constraints to the optimizer. This exchange of information must be repeated for each new individual that is generated at each generation of the evolutionary process.

2.4 HIERARCHICAL COMPOSITION OF POFS AND MM-POFS

The second key aspect of the methodology presented in this Thesis is the hierarchical composition of PoFs and mm-PoFs. This is not a straightforward process and presents important problems and challenges that must be handled carefully so that the obtained results can be considered acceptable. First, when generating the PoF at a certain level, we must ensure that only PoFs of the blocks at the lower level and not their whole feasible performance space are necessary. This idea is depicted in Fig.2.7.

However, for this to be truth, a set of conditions must be met. Otherwise, it could happen that designs of the low-level spaces that are not part of the PoF lead to Pareto-optimal designs of the higher-level blocks and, therefore, using only the PoF would not be the best concept to represent the whole feasibility space. This unwanted situation is shown in Fig.2.8.

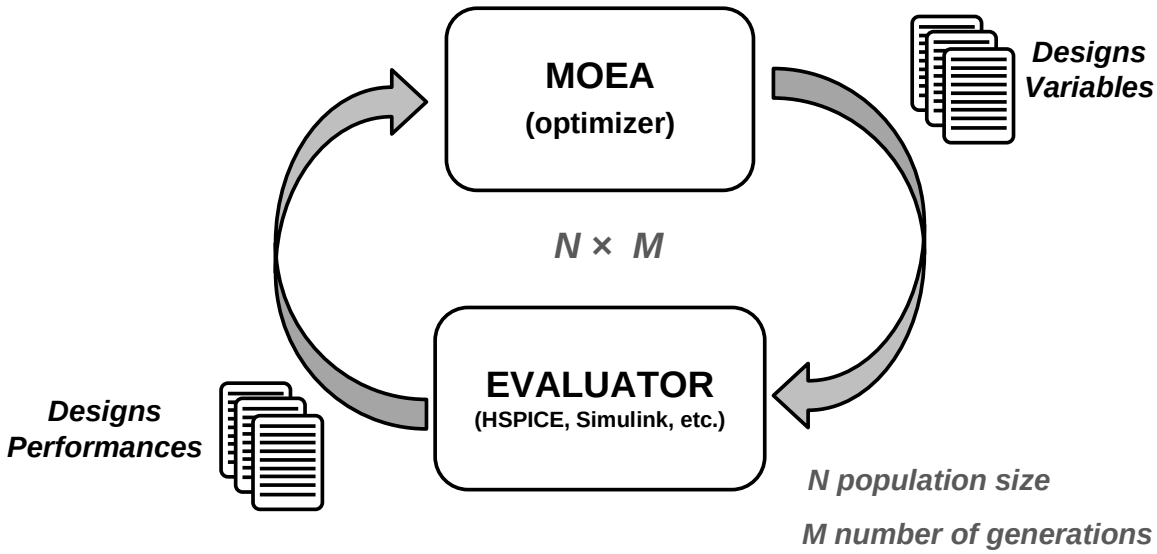


Figure 2.6: Multi-objective Evolutionary Algorithm (MOEA) coupled to an evaluator. The MOEA passes the design variables of each individual to the evaluator, which returns the values of the design objectives and constraints back to the optimizer. This is repeated for each new individual that is generated at each generation.

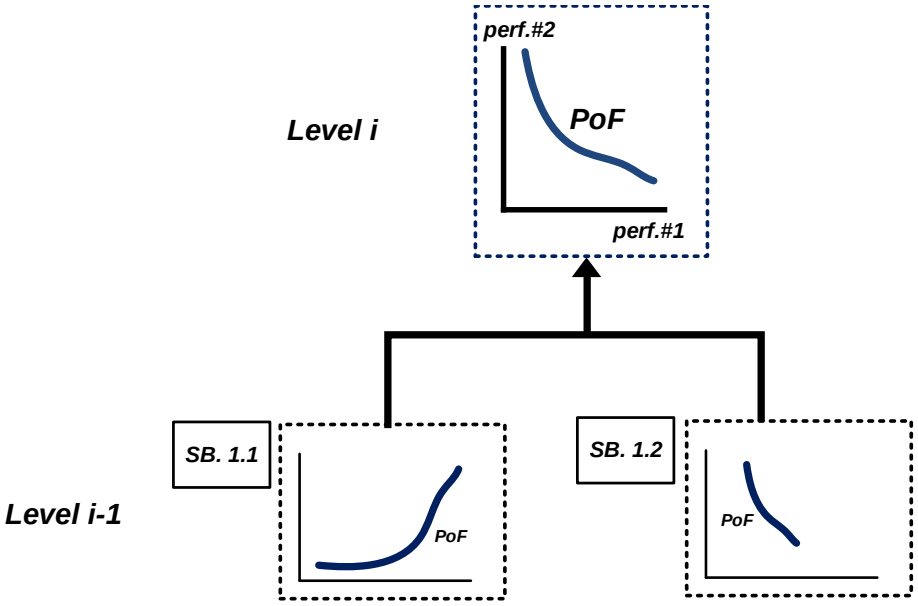


Figure 2.7: The generation of a PoF of a block at a certain level requires only the PoFs of the blocks at the lower level.

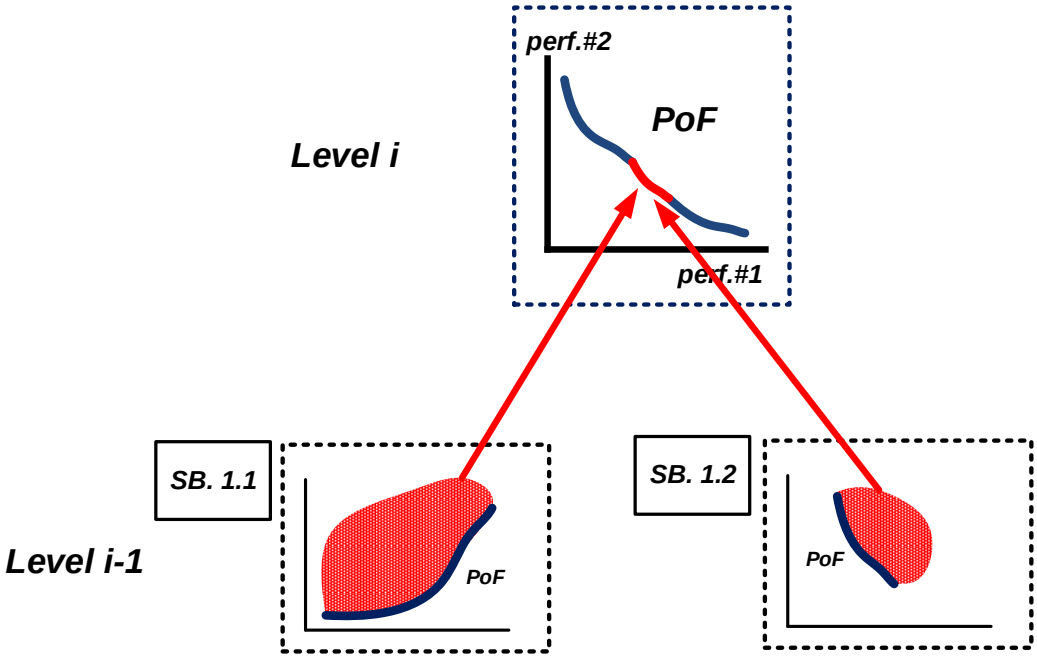


Figure 2.8: Designs that are not part of the PoF of the blocks at the lower level contribute to the PoF of the block at the higher level.

This problem was first addressed in [52], which stated that the Pareto front at one level of the hierarchy can be obtained from the Pareto fronts of a lower level as long as the relationships between the performances at the higher level with respect to performances at the lower level satisfy strong monotonicity. Later, Eeckelaert et al. extended these relationships in [37].

This Thesis addresses two other important problems in bottom-up methodologies. The first one is the dependence of some performances of analog circuits on their surrounding circuitry. The consequence of this dependence is that performances of low-level blocks may change during the generation of the PoFs of higher-level blocks that impose different conditions than those for which the low-level PoFs were generated. As a consequence of this change, some designs of the low-level PoFs may become invalid because they do not fulfill some design constraints any more. Moreover, designs may be displaced over the performance space, becoming dominated, or may be shifted to non-practical regions of the performance space, leaving other more practical regions empty. In case any of these situations occurs, the invalid designs must be identified and discarded for the generation of the higher-level PoF. An illustrative example of this situation is depicted in Fig.2.9.

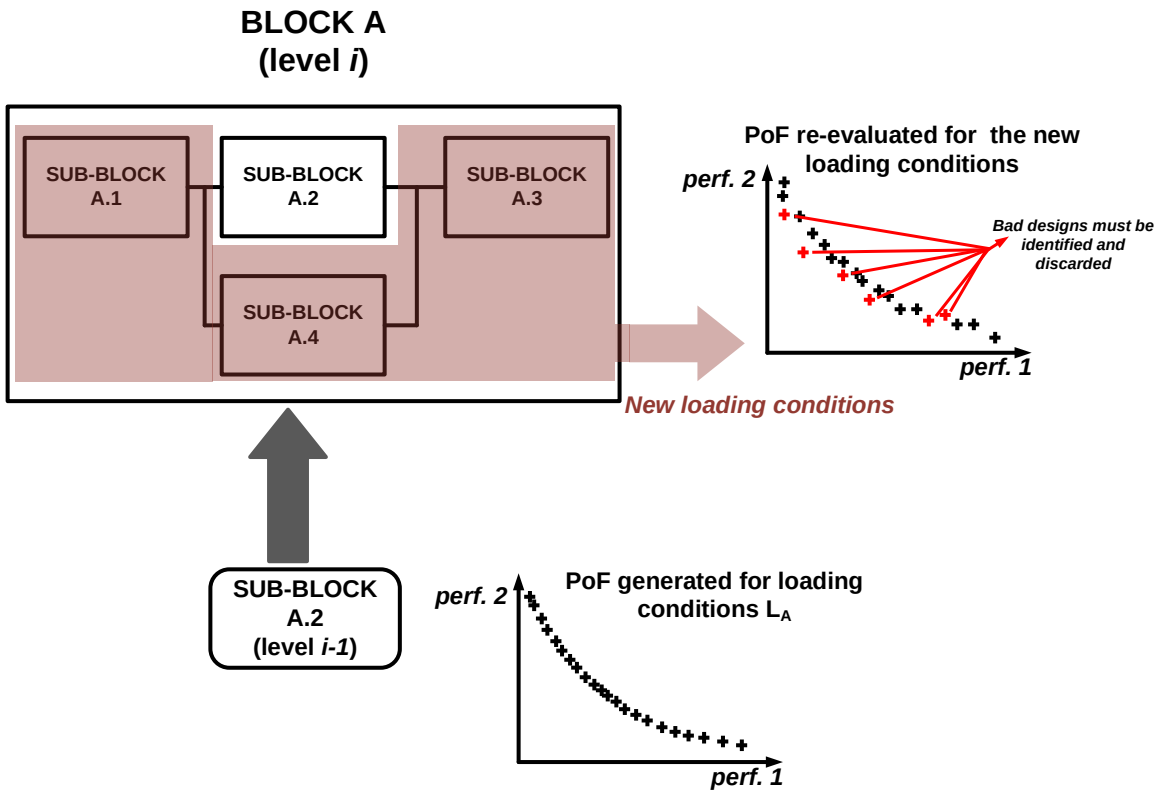


Figure 2.9: Performances of analog circuits must be re-evaluated under the new loading conditions.

This context dependency is a problem that must be solved. For the first time, this work presents an approach for the case of the dependency of the performances of operational amplifiers with their loading conditions. This is one of the most important blocks, present in almost any analog system, and its main performances might be changed by the loading conditions. In order to re-evaluate the amplifiers under the new loading conditions, a new technique that uses the poles and zeroes of the gain and output impedance to calculate the new performances under the new conditions is used. This technique allows to obtain the new values of the performances without needing electrical simulations. This helps reducing the required CPU time and, as it will be explained better in Chapter 4, makes possible to use the technique for the hierarchical composition of PoFs and mm-PoFs.

The second issue that has been considered in this Thesis is related to the inherent difficulty of efficiently exploring multi-dimensional low-level PoFs. In the generation of the PoF of a bottom-level block, the variables that compose the design space are real variables as transistor sizes or the values of resistors and capacitors. Exploring that design space is straightforward because their values have

real meaning, that is, two similar values of resistance represent two similar resistors. In the generation of higher-level PoFs, besides transistors or other devices, the finite set of design solutions of lower-level PoFs are also part of the design space. The problem is that the search over low-level PoFs is more complex as we need to represent each of their design solutions with a set of variables that has a real meaning, that is, that similar values of these variables actually represent similar designs in terms of their performances. Otherwise, the evolutionary algorithm will not be able to explore efficiently the design spaces defined by the low-level PoFs.

If we think in exploring a design space composed by a resistor, the MOEA will look for the correct value of the resistor within a given range. But this is done through the crossover operator and the mutation operator, the latter following some probability density function, e.g., a normal distribution. Given a value of the resistor, the MOEA can move through the range of values, mutating that initial value into another value, slightly different. By doing so, the algorithm can find the correct direction towards the value that best fit to the given problem. Let us think now in a similar problem where, instead of a resistor, the design space is composed of a set of designs of a previously generated PoF. For the MOEA to explore that design space, it is essential to use a proper set of design variables that keep some relationship with the performances of the designs they represent. Otherwise, the probability density function of the mutation operator would be equivalent to a uniform distribution, which would transform the evolutionary process into a completely random search. This fact will be explained in much more detail in Chapter 4. The solution adopted in this Thesis is based on the use of what we denote an index-mapping process, which uses a set of coordinates that are assigned to the designs of low-level PoFs. The values of the coordinates are assigned according to the performances of the designs. By doing so, designs with similar performances will have similar coordinates. This simple concept, illustrated in Fig.2.10 for the case of a 3D PoF that is mapped using two coordinates, allows the evolutionary algorithm to mutate these coordinates as conventional variables. The selection of this method to solve this issue of the hierarchical composition of PoFs will be justified in Chapter 4, where a set of experiments are carried out in order to compare several alternative methods.

2.5 SUMMARY

In this Chapter, the main aspects of the methodology presented in this Thesis have been described. Particular attention has been paid to the generation of PoFs and mm-PoFs of the constitutive blocks of a complex system and to the bottom-up hierarchical composition of these fronts until the Top-level. In the following chapters these aspects will be explained in more detail, discussing their

implementation and supporting the given solutions with experimental results. In Chapter 3, the method developed in this Thesis to generate the PoFs and mm-PoFs of analog circuits is described. Chapter 4 focuses on the implementation issues of the hierarchical composition of those fronts.

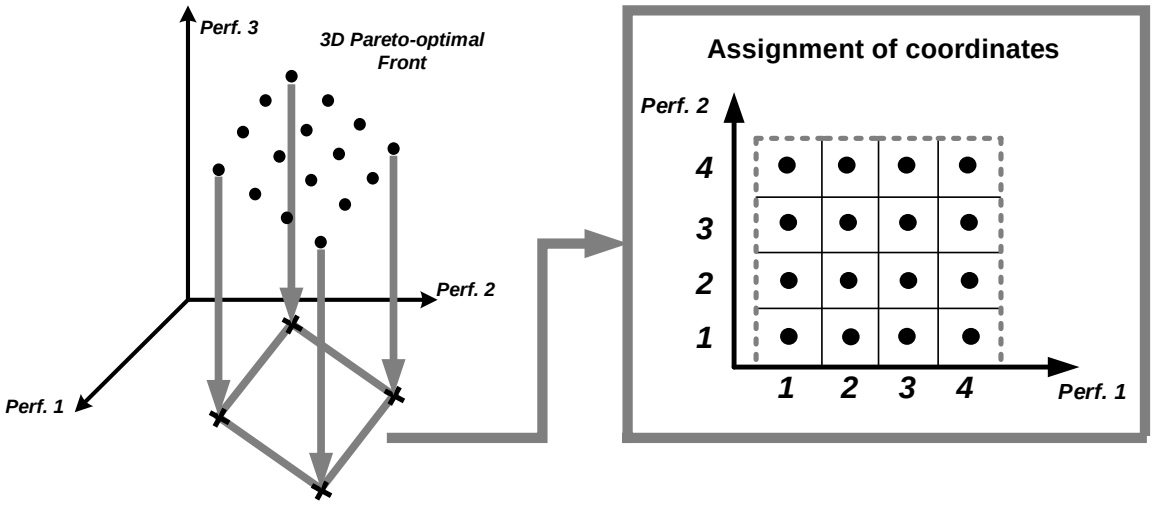


Figure 2.10: Assignment of coordinates to the designs of low-level PoFs for hierarchical exploration.

3

GENERATION OF PARETO-OPTIMAL FRONTS FOR RECONFIGURABLE CIRCUITS

The methodology presented in this Thesis is based on the use of the Pareto-optimal fronts (PoFs) of the analog circuits that constitute a complex system. As it has been explained in the previous chapters, the use of the PoFs, instead of the whole feasible performance space of the blocks, is motivated by the fact that, first, they are less expensive to generate and, second, since they are formed by the designs with the best trade-offs between the circuit performances, any system composed by any of those designs will also be optimal. An important advantage of using PoFs is that they enhance the concept of re-usability, which is a very important characteristic of bottom-up design methodologies. PoFs of basic building blocks can be generated and stored a priori so that they can be used later whenever the blocks are required for the design of a more complex system. Similar to having a library of components, we can build a library of circuits, each represented by its PoF. Fig.3.1 depicts this idea: a library of PoFs of the most basic blocks is already available and the PoFs of the more complex blocks are generated by the hierarchical composition of the PoFs of the low-level blocks.

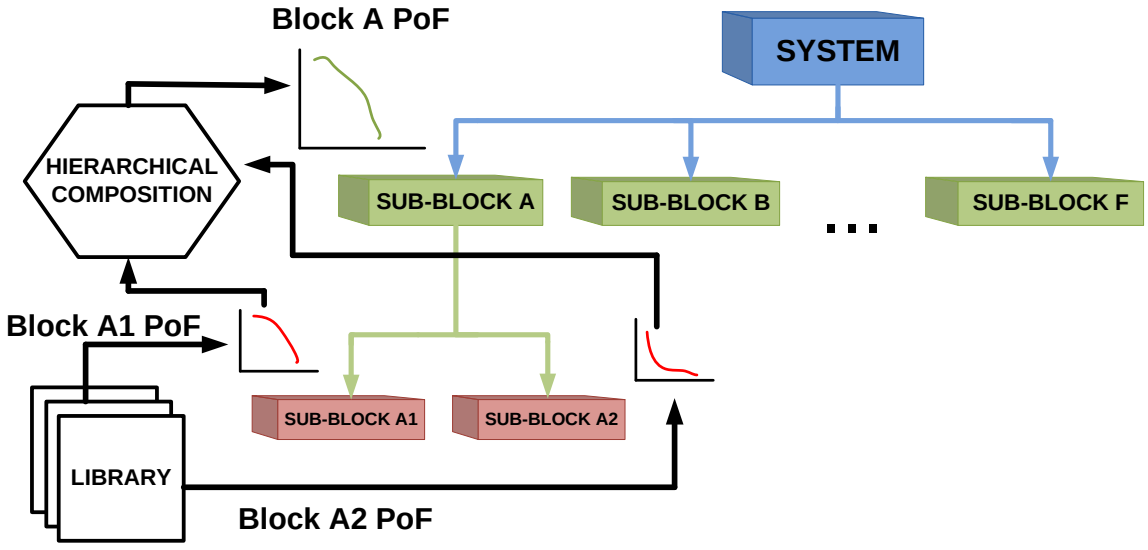


Figure 3.1: Philosophy of the methodology presented in this Thesis. PoFs of basic building blocks can be stored in libraries that can be used in the design of complex systems.

A key contribution of this Thesis, regarding Pareto-optimal Fronts, is how this concept can be extended for reconfigurable circuits, which are of great importance in the design of multi-standard analog and mixed-signal systems. In the present communication scenario, where mobile terminals and other devices must support different standards and provide more and more functionalities, reconfigurable circuits contribute with reduced area occupation and power adaptability. Reconfigurable circuits can be represented using what has been named in this Thesis as multi-mode Pareto-optimal Fronts (mm-PoFs). At present, there are no contributions, neither in the field of Evolutionary Algorithms nor in microelectronics, that covers the generation of such mm-PoFs. Because of this, a new evolutionary algorithm that allows such optimizations has been developed in this Thesis.

In this Chapter first the concept of PoF and how it can be generated using an available multi-objective evolutionary algorithm (MOEA) are explained. Next, the new MOEA developed in this Thesis will be described in detail. Pseudo-code of the functions of the algorithm developed in this Thesis are given in APPENDIX I.

3.1 GENERATION OF PARETO-OPTIMAL FRONTS: GENERAL ASPECTS

The concept of Pareto-optimal Front (PoF) has already been introduced in Chapter 2. PoFs are solutions of **Multi-Objective Optimization Problems** (MOOP), where several design objectives must be optimized while some design constraints are met:

$$\begin{aligned} &\text{maximize/minimize } \vec{y} = \vec{f}(\vec{x}) = (f_1(\vec{x}), f_2(\vec{x}), ..., f_b(\vec{x})) \\ &\qquad\qquad \text{subject to } g_j(\vec{x}) \geq 0, j = 1, 2, ..., k \end{aligned} \tag{3.1}$$

As shown in the previous equation, both design objectives and constraints are functions of a set of design variables, $\vec{x}$. For example, for a circuit the design variables can be the values of resistors and capacitors or transistors sizes; the design objectives can be circuit performances as power consumption and area; and design constraints may be conditions the circuit must fulfill (such as a minimum DC-Gain in the case of an amplifier). A property of optimal solutions of a MOOP is that they are non-dominated between them according to the Pareto-dominance criterion. It establishes that a solution $\vec{a}$ dominates solution $\vec{b}$ ($\vec{a} \prec \vec{b}$) if all design objectives of $\vec{a}$ are better or equal than those of $\vec{b}$, and $\vec{b}$ is strictly better than $\vec{b}$ in at least one design objective. This definition is valid when both individuals fulfill all design constraints. Otherwise, solution $\vec{a}$ dominates solution $\vec{b}$ if $\vec{a}$ violates the design constraints to a lesser extent than $\vec{b}$. On the other hand, a solution $\vec{a}$ is non-dominated if there is no other solution that dominates it.

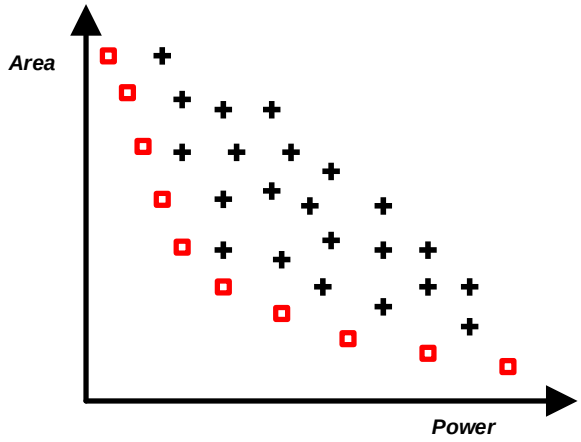


Figure 3.2: Hypothetical PoF of a circuit for area and power consumption.

To illustrate this, let us consider the example shown in Fig.3.2. It represents possible sets of values of area and power consumption of an hypothetical circuit. For any circuit it is always of interest to reduce the power consumption and the area as much as possible. Unfortunately, reducing the power consumption usually requires an increment of the area, and vice-versa. All points in the figure (black crosses and red squares) are part of the feasible space for that hypothetical circuit and for those two conflicting performances, but only red squares are part of the PoF of the circuit. As it can be seen, all red squares are non-dominated and every black cross is dominated by at least one point of the PoF.

MOOPs can be solved using different approaches. A straightforward approach is to transform the MOOP into a single-objective optimization process. This can be done by unifying the multiple objectives into a single cost function, defined as the sum of all design objectives, each one typically scaled by a different weight, as shown in equation 3.2.

$$f(\vec{y}) = w_1 \times y_1 + w_2 \times y_2 + ... + w_b \times y_b \tag{3.2}$$

However, the outcome of a single-objective optimization process is a single solution. Thus, in order to generate the PoF of the circuit, multiple optimizations are required. Besides, in each optimization the weights must be different to obtain different solutions, but how to set the weights properly will be unknown in most cases [53].

Evolutionary algorithms (EAs), on the other hand, are population-based meta-heuristic optimization algorithms that use biology-inspired mechanisms like mutation, cross-over, natural selection, and survival of the fittest in order to improve a set of candidate solutions iteratively [54] [55]. Multi-objective

evolutionary algorithms (MOEAs) are very efficient methods to perform the optimization of multiple, usually conflicting, design objectives, and address the direct generation of the complete PoF [42].

However, none of the available MOEAs is able to solve the problem of optimizing a reconfigurable circuit. For this reason, in this Thesis, a new evolutionary algorithm, able to perform the multi-mode optimization that is needed for the generation of the mm-PoFs of reconfigurable circuits, has been developed by using the MOEA NSGA-II [56] as reference and source of inspiration. It is a population-based MOEA that, due to its efficiency and good performance, became a landmark against which other multi-objective evolutionary algorithms had been compared in the past decade [57]. It also established the structure followed by others MOEAs that came after: a Pareto-dominance selection operator that incorporates reproductive operators, which used iteratively, generate new candidates solutions [58]. The main functions of this MOEA, specially those that will be of interest for a better understanding of the last section of this Chapter, are described in the following section.

3.1.1 *NSGA-II*

An evolutionary algorithm, as its name suggests, evolves a population of individuals through an iterative process, where each iteration is denoted as "generation". In NSGA-II, the first generation consists in the creation of an initial population of N individuals. At this step, each individual is created by assigning random values to its design variables. It is necessary, thus, to establish a priori ranges for each design variable. Design knowledge can be used at this point to introduce solutions that help improving the convergence to the Pareto-optimal region of the performance space. Afterwards, the initial population is evaluated to obtain the values of the design objectives and constraints of each individual. Finally, the individuals are sorted following the Pareto-dominance criterion described at the beginning of this Chapter. An example is shown in Fig.3.3, where two conflicting design objectives are being minimized. The shadowed region represents all possible combinations of the two design objectives, that is, the feasible performance space, while the red-dashed line represents the theoretical PoF that must be found. As it can be seen, the initial population, formed by the black dots and red crosses, is a sampling of the whole space. The red crosses are the non-dominated solutions of this initial population.

After the initial population has been evaluated and classified, the iterative evolutionary process begins. At each generation, individuals from the parent population (the initial population in the first generation) are selected to form the child population, also formed by N individuals. The new individuals in the child

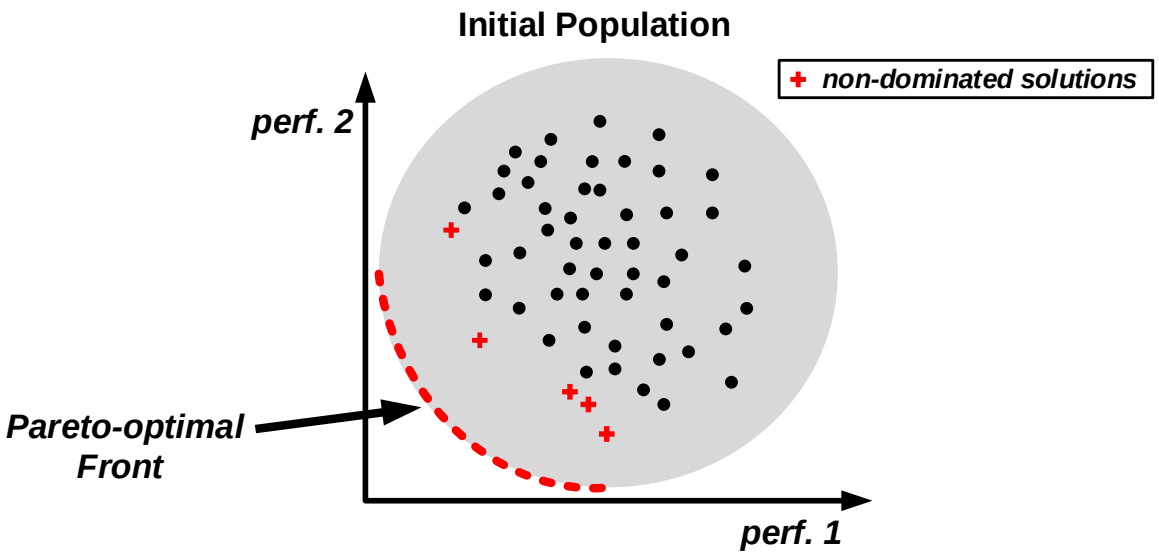


Figure 3.3: Example of the initial population of the evolutionary optimization process. The gray area represents the complete feasible performance space. Black points are solutions of the initial population. Red crosses are the non-dominated solutions of that initial population.

population must compete with those in the parent population, using for this the Pareto-dominance criterion. As a result, the best N individuals among both the child and parent populations are selected to form the new population, which will be the parent population of the next generation of the evolutionary process. The processes involved in a generation of this process are depicted in Fig.3.4 and are described briefly in the following lines.

- **Selection and Cross-over**, where individuals of the parent population compete between them to select individuals that are crossed-over to generate an offspring population of N individuals.
- **Mutation** of the offspring population to produce random variations and generate new and more diverse solutions.
- **Evaluation** of the offspring population. Here the design objectives and constraints of the individuals are obtained. In the case of electronic circuits, the evaluator may be an electrical simulator like HSPICE®.
- **Filling and non-dominated sorting**, where the parent and the offspring populations compete and the N fittest individuals are selected to form the new generation, which will be the parent population of the next generation.

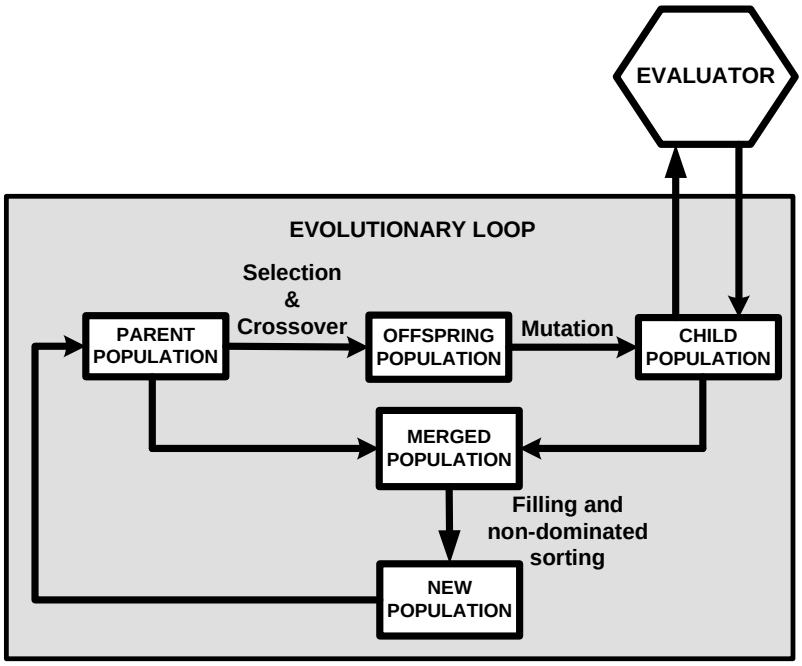


Figure 3.4: Steps of a generation of NSGA-II.

An example is shown in Fig.3.5. Individuals of the parent population are represented in black circles and those of the child population are represented in gray squares. The non-dominated individuals of the previous generation are enclosed in green circles, while the non-dominated individuals of the current generation are enclosed in red squares. As it can be seen, new individuals of the child population have been found that dominate those individuals and, thus, are nearer to the Pareto front. That is, by the cross-over and mutation mechanisms of the MOEA, new *child* individuals have been found that are better, in terms of Pareto dominance, than their *parents*. So, after each generation, solutions nearer to the Pareto front can be found. Let us note here a couple of important things about PoFs. Using a MOEA, the front generated will be only an approximation of the so-called **true PoF**, which is defined as the Pareto front the evolutionary process would obtain if it could explore all possible solutions of the complete feasible performance space. In general, the true PoF is unknown because the computational cost for such exhaustive exploration is typically unaffordable. It is desirable that the front generated is as extensive as possible in order to cover a larger region of the PoF. Besides, it is also desirable that the front generated covers that region as uniformly as possible. This can be achieved by maximizing the minimal crowding distance, which will be explained later and that is basically a measure of the distance of each individual to its nearest neighbours in the design-objective space (or feasible

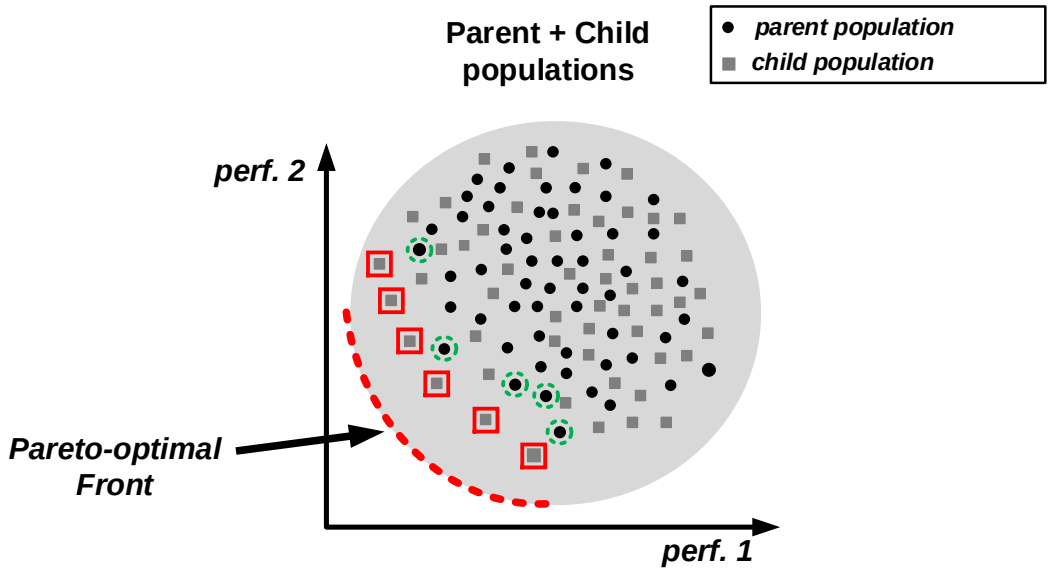


Figure 3.5: Individuals from the parent and the child populations compete to form the new population for the next iteration of the evolutionary process.

performance space). These two aspects, extent and uniformity, are very important in bottom-up design methodologies to ensure diversity of solutions and reduce the loss of valid designs as the PoFs of the circuits are hierarchically composed. The most important processes involved are described in more detail in the following lines.

Tournament Selection and Cross-over

This is the first step in each generation. Here, individuals of the parent population compete between them to select those individuals that are crossed-over to generate the individuals of the offspring population. For this, the individuals in the population are randomly taken in groups of four. The process is depicted in Fig.3.6 for a better understanding. From each one of these groups, two tournaments are performed, from which two parent individuals are selected. This tournament is a Pareto-dominance comparison between the individuals. If as a result of this check the individuals are non-dominated, then the one with larger crowding distance is selected. By doing so, the evolutionary process rewards the individuals that are more separated, which improves the uniformity and the extension of the front generated. Finally, the selected parent individuals are crossed-over to generate two child individuals. Two of the concepts involved in this process, the constraint violation metric and the crowding distance, deserve a little more attention.

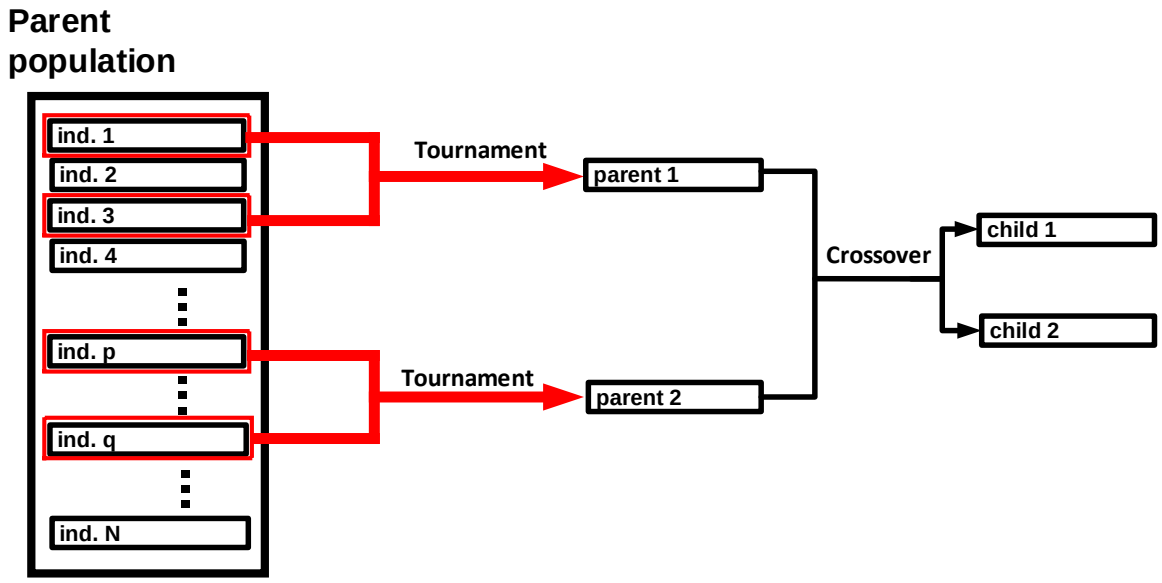


Figure 3.6: Tournament of the individuals in the parent population to generate child individuals.

1. *The constraint violation metric, CV*

   The constraint violation metric is a measure of the quantity of design constraints that are not fulfilled. This metric is used when checking the dominance between two individuals, where first the value of the constraint violation is compared. When both individuals fulfill all design constraints, or when they have the same value of the CV metric, the dominant individual is chosen using the Pareto-dominance criterion. In any other case, the dominant individual will be that with the smaller constraint violation.

2. *The crowding distance metric, CD*

   The crowding distance is a metric used to enhance the extension and uniformity of the density of solutions in the performance space. It is measured as the average distance between an individual and its nearest neighbours in the design objective space. For each individual and for each design objective, the normalized distance to the nearest neighbours on either side of the point considered is calculated. The value of the crowding distance is then the average value of that distance among all design objectives. Fig.3.7 illustrates this concept with 2 design objectives. It is important to note that, for individuals with maximum or minimum value of one or more of the design objectives (in this example, individuals 1 and 4) the assigned value of crowding distance is infinite.

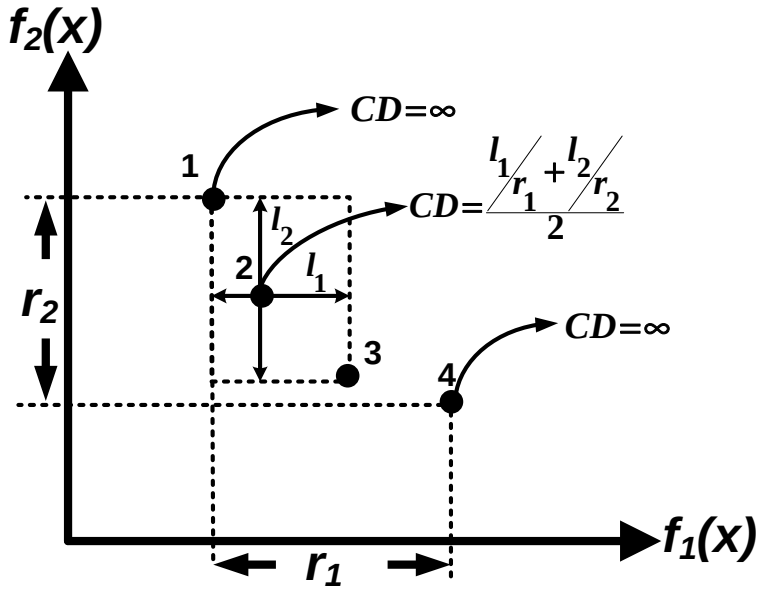


Figure 3.7: Crowding distance of an individual for 2 design objectives.

The use of the crowding distance tries to guarantee a good diversity among population members. This is very important because, besides the convergence to the PoF, it is also desired that it covers the widest frontier of the feasibility space as uniformly as possible. From the point of view of the designer, this increases the probability of a front of being reused, allowing to use designs with very different performance values.

Mutation

Each design variable of each individual in the offspring population has a chance of being mutated. This mutation can randomly change the value of the design variable to any value within the ranges defined by the designer. These are the same ranges used for the creation of the initial population. The probability function gives maximum probability to the current value of the design variable and decreases with the distance to the current value. By doing so, slightly different individuals are generated that, as in natural mutation, may be better in terms of Pareto dominance than the parent. An example is shown in Fig.3.8.

Filling and non-dominated sorting

The parent and mutated populations are combined into the mixed population, whose best individuals are selected for the next iteration of the evolutionary process. For this selection process, the individuals of the mixed population are first

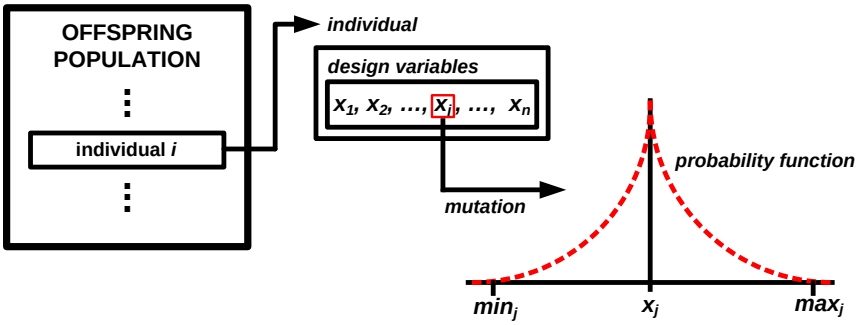


Figure 3.8: Mutation of a design variable of an individual.

sorted in different fronts according to their degree of dominance. For example, front 1 (F1) contains the non-dominated individuals, front 2 (F2) contains individuals dominated by at least one individual in F1, and so on. In order to generate these fronts (F1, F2, ...), NSGA-II takes each individual (let us call this individual "current individual") of the mixed population and compares it to each other individual (that is, performs a dominance check). Several results are possible from this comparison:

- When an individual dominates the "current individual", NSGA-II discards the "current individual" and selects the following one from the mixed population, then repeating the process.
- If both individuals do not dominate each other, the next individual from the mixed population is selected to be compared with the "current individual".
- If the "current individual" dominates the other individual, the latter is marked to be omitted in successive comparisons until the next front is going to be generated.

If no other individuals dominate the current individual, this one is added to an elite list, which constitutes the current front. Once the check has been done for all individuals in the mixed population, the individuals in the elite list form the current front and the crowding distance is calculated for each one. Note then that the crowding distance is calculated between individuals of the same front. After this process has been completed, the elite list is emptied and the process is repeated for the individuals left in the mixed population. The individuals in a same front are non-dominated between them and are dominated by at least one individual from the previous front (except for F1, whose individuals are not dominated) in the ordered list of fronts.

The fronts formed in the previous step are copied to the new population, beginning with F1, following with F2, and so on. This process is shown in Fig.3.9.

If not all the individuals in a front can be added to the new population, they are added in decreasing order of their CD, until the new population is full. Note that in the example shown in Fig.3.9 there is no room in the new population for all individuals in F3, so they are added as explained here. Once the filling process is completed, the new population will be the parent population in the next iteration of the evolutionary process.

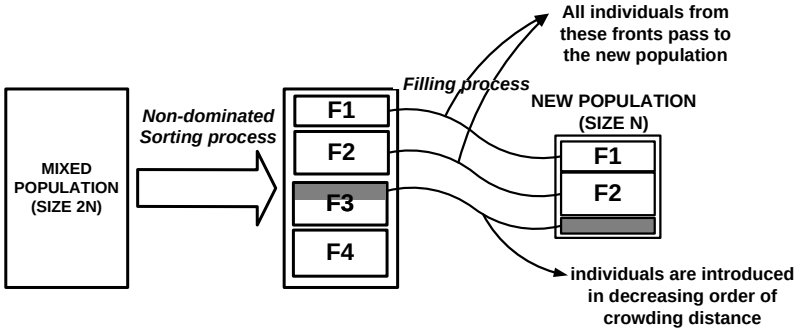


Figure 3.9: Non-dominated sorting and filling processes.

3.1.2 *Example: PoF of an Operational Amplifier*

To illustrate the generation process of a PoF of an electronic circuit, the PoF of an opamp will be generated. For this, the folded-cascode Miller-compensated opamp of Fig.3.10 is used in 0.35-μm CMOS technology.

The set of design variables characterizing each individual (also known as the chromosome) is also depicted. These are transistors sizes, bias current and values of the compensated capacitor and resistor. These variables and their ranges, which have to be specified by the designer, are shown in Table 3.1. The rest of the variables that do not appear in the chromosome are related with the design variables through a set of expressions. This makes the space to be explored smaller and the optimization process more efficient, avoiding many invalid points of the design space that would lead to infeasible designs. These relations are detailed in Table 3.2. Variables w_i and l_i refer to the width and the length of transistor M_i. Most of these functions are needed for the symmetry of the topology (stated as "symmetry"). Expressions 1, 2 and 3 are explained below.

- **Expression 1** ensures that transistors M_{10} and M_{11} still operate in the saturation region for unbalanced operation of the input differential pair. Thus, the following condition must hold:

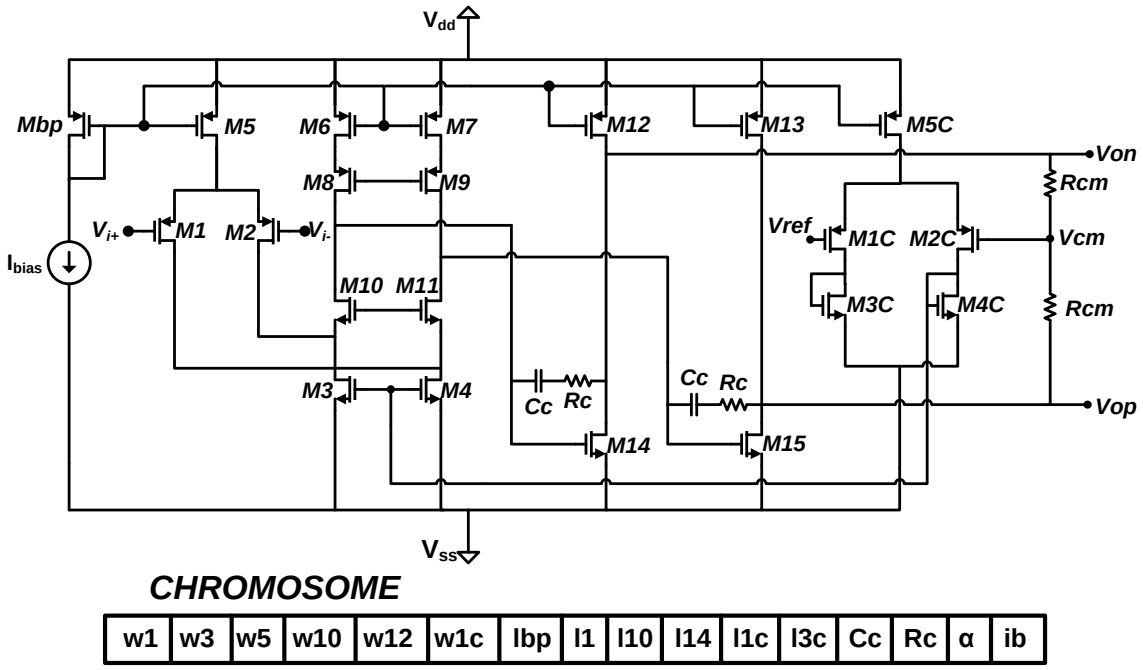


Figure 3.10: Folded-cascade, Miller-compensated operational amplifier used for the examples and the chromosome that characterizes it.

Table 3.1: Design Variables.

Design Variable	Range	Design Variable	Range
w_1	2 - 800 μm	l_{14}	0.35 - 5 μm
w_3	2 - 800 μm	l_{1c}	0.35 - 5 μm
w_5	2 - 800 μm	l_{3c}	0.35 - 5 μm
w_{10}	2 - 800 μm	C_C	0.07 - 2 pF
w_{12}	2 - 800 μm	R_C	0.5 - 5 $k\Omega$
w_{1c}	2 - 800 μm	α	1 - 200
l_{bp}	0.35 - 5 μm	I_{bias}	1 - 10^3 μA
l_1	0.35 - 5 μm		
l_{10}	0.35 - 5 μm		

$$I_6 > I_{bias}/2 \rightarrow I_6 = (0.5 + \kappa) \cdot I_{bias} \tag{3.3}$$

where $\kappa \cdot I_{bias}$ is the minimum current flowing through M_{10} and M_{11} to ensure saturation operation. Typically $\kappa = 0.1$, so that $I_6 = 0.6 \cdot I_{bias}$. This relationship

Table 3.2: Dependent Variables.

Dependent Variable	Relationship	Why?
w_2	$= w_1$	symmetry
w_4	$= w_3$	symmetry
$w_1 1$	$= w_1 0$	symmetry
$w_1 3$	$= w_1 2$	symmetry
$w_b p$	$= w_5$	symmetry
$w_6, w_7, w_8, w_9, w_{5c}$	$= 0.6 \cdot w_5$	Expression 1
$l_3, l_4, l_5, l_6, l_7, l_8, l_9, l_{12}, l_{13}, l_{5c}$	$= l_{bp}$	symmetry
l_2	$= l_1$	symmetry
l_{11}	$= l_{10}$	symmetry
l_{15}	$= l_{14}$	symmetry
w_{14}, w_{15}	$= \frac{\alpha}{\beta/2} \cdot \frac{w_{12}}{w_5} \cdot I_{bias} \cdot l_{14}$	Expression 2
w_{2c}	$= w_{1c}$	symmetry
l_{2c}	$= l_{1c}$	symmetry
l_{4c}	$= l_{3c}$	symmetry
w_{3c}, w_{4c}	$= \frac{0.2027 \cdot l_{3c} \cdot w_3}{w_5 \cdot l_{bp}}$	Expression 3

between currents translates directly into a relationship between the width of the transistors:

$$\frac{I_{bias}}{w_5} = \frac{I_6}{w_6} \implies w_6 = \frac{I_6}{I_{bias}} \cdot w_5 = 0.6 \cdot w_5 \tag{3.4}$$

- **Expression 2** is used to maintain a constant current density flowing through the output transistors M_{15} and M_{14}. By doing so, their overdrive voltage is constrained to vary over a range such that points of the design space featuring better output swing are favored. Design variable α represents the overdrive voltage of transistors M_{14} and M_{15}:

$$\alpha = \frac{1}{v_{ov}^2} = \frac{1}{\left(V_{GS_{14,15}} - V_{th}\right)^2} \tag{3.5}$$

where v_{ov} is the overdrive voltage, and V_{Tn} is the threshold voltage. By impossing that the current through transistor M_{14} is equal to that of transistor M_{12}:

$$\frac{\beta/2}{\alpha}\frac{w_{14}}{l_{14}} = I_{12} = \frac{w_{12}}{w_5} \cdot I_{bias} \tag{3.6}$$

Expression 2 is obtained by isolating w_{14} from this last equation:

$$w_{14} = \frac{\alpha}{\beta/2} \cdot \frac{w_{12}}{w_5} \cdot I_{bias} \cdot l_{14} \tag{3.7}$$

- **Expression 3** ensures that cascode transistors M_3 and M_4 provide enough current. Transistor M_3 must drive a current greater than $I_{M5}/2$ in the balanced point. Thus:

$$I_{M3} = I_{M10} + \frac{I_{M5}}{2} \tag{3.8}$$

Since $I_{M3} = (S_{M3}/S_{M3C}) \cdot I_{M3C}$ and $I_{M10} = (S_{M6}/S_{M5}) \cdot I_{M5}$ (where S_{MX} is the aspect ratio, w_X/l_X), the correct sizing of transistor M_{3C} is given by the following expression:

$$S_{M3C} = \frac{S_{M5} \cdot S_{M3}}{2 \cdot S_{M6} + S_{M5}} \tag{3.9}$$

Since $S_{M6} = 0.6 \cdot SM5$, the expression for the width of transistor M_{3C} is:

$$w_{3c} = \frac{0.6 \cdot w_3}{2.2 \cdot l_{bp}} l_{3c} \tag{3.10}$$

The experiment that will be used to generate the PoF will have the following characteristics:

- The design objectives will be to maximize the DC-Gain and the unity-gain frequency (fu), and to minimize the power consumption and the area occupation.
- The constraints are shown in Table 3.3. In the last row, dm is defined as:

$$dm = \frac{V_{DS}}{v_{ov}} \geq 1.1, \tag{3.11}$$

Table 3.3: Constraints applied to the optimization problem.

Constraint	Values
Phase Margin (PM)	$60^\circ \leq \text{PM} \leq 90^\circ$
Output Swing (OS)	$\geq 3.6V$
dm (for each transistor)	≥ 1.1

being V_{DS} the drain-source voltage and v_{ov} the overdrive voltage. This is necessary to ensure the transistors are always working in the saturation region.

- The evaluator used to measure design objectives and constraints of the individuals is HSPICE®. For the communication with the evaluator, the optimizer store in a file the information that characterizes all the individuals (a file containing design variables of all individuals created in the current generation) and fed it to the evaluator. By doing so, the circuit matrices are calculated only once and the evaluation of an individual only requires a substitution of the parameters of those matrices. This reduces significantly the CPU Time of the evaluation.

- The experiment is carried out in a 0.35-μm CMOS technology with $\pm$1.5-V supply voltages.

- The **population size** is fixed to 1000 individuals and the number of generations is set to 100.

- The PoF is generated for a load of a 20 kΩ resistor and a 1.0pF capacitor.

The projection of the PoF of the amplifier onto different planes of the design objectives is shown in Fig.3.11. In the figure, each point represents a different design of the amplifier. It is important to note that all designs in the obtained PoF are non-dominated among them. However, as in this case there are four design objectives, this is more difficult to observe than in the case of only two design objectives. To illustrate this, let us take designs A, B and C, which are marked in the Figure. As it can be seen in the projection onto the DC-gain-fu plane, designs A and B have a better trade-off between those objectives than design C. But, as it can be seen in the other projection of the PoF, design C has a better trade-off between the power consumption and the area than designs A and B and, therefore, the three designs are non-dominated between them.

Once the procedure to generate the PoF of an analog circuit has been described, the next section will focus on how to extend the same technique to the generation

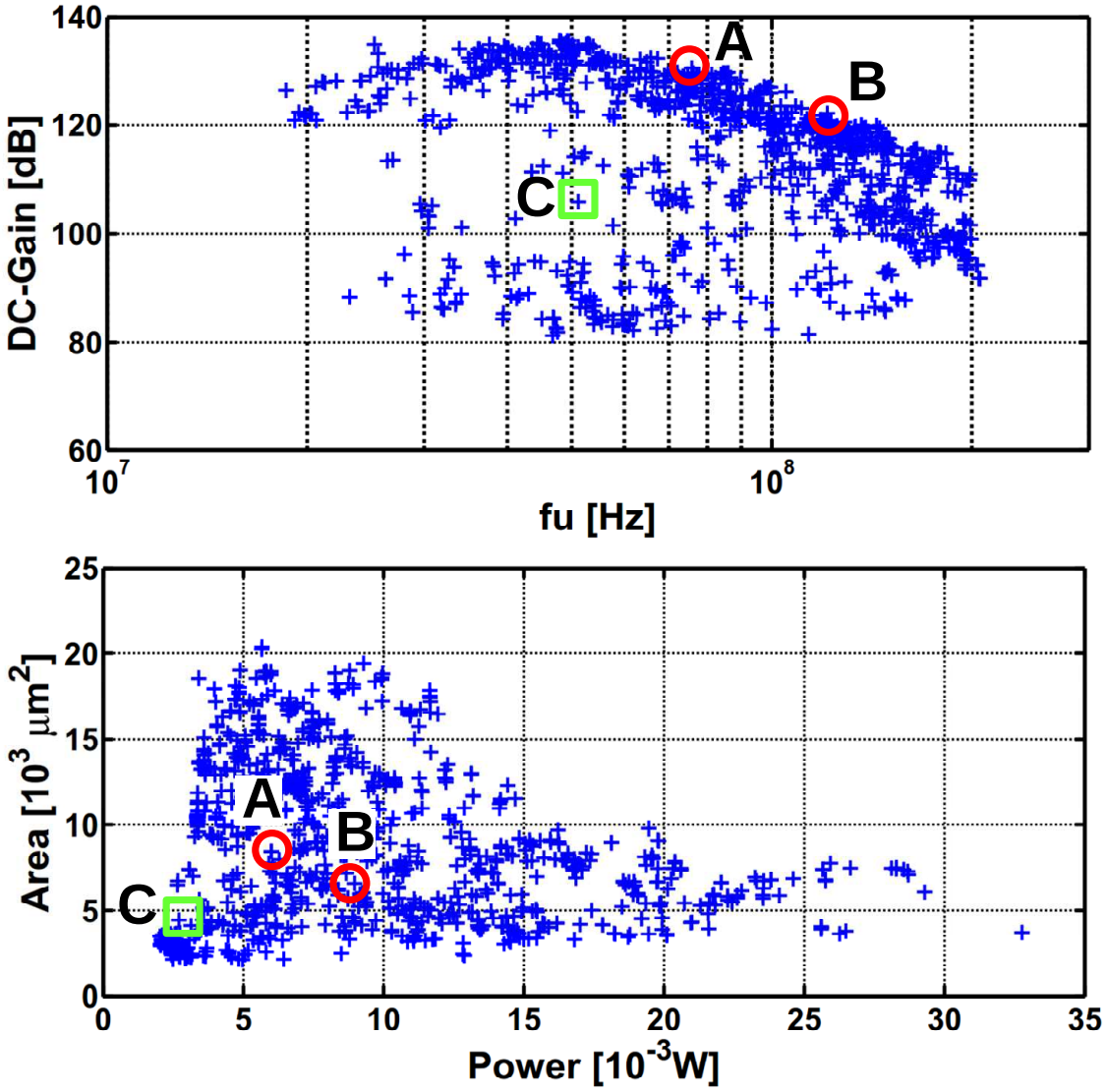


Figure 3.11: Projection of the PoF onto the DC-Gain-fu and the power-area planes.

of mm-PoFs of reconfigurable analog circuits. As it will be discussed, this entails the definition of a new dominance criterion that takes into account the dominance between the different operation modes of a same individual as well as the dominance between the different operation modes of different individuals. Besides, concepts that have been introduced in this Chapter such as individuals, constraint violation or crowding distance, among others, get a new significance in the case of reconfigurable circuits. In order to include these new ideas into an evolutionary optimization process, a new evolutionary algorithm will be implemented taking as reference NSGA-II, which has been described in detail in this Chapter. As it will be explained in the following sections, a set of modifications must be introduced in the structures and processes that are used for the generation of single-mode PoFs.

3.2 PARETO-OPTIMAL FRONTS FOR RECONFIGURABLE CIRCUITS

A reconfigurable circuit is a circuit that is able to change one or some of its design parameters to provide a different set of specifications. For example, an operational amplifier that is able to change its input stage to provide a different gain. Reconfigurable circuits are used in systems that need to support multiple standards, where their power adaptability is advantageous. Besides, the area also benefits from the use of such circuits as they use the same hardware in multiple operation modes, being able to include more functionalities in the same space.

Let us remind two concepts that will be used later in this Chapter. The first is the **reconfiguration strategy**. It establishes how the reconfiguration is achieved. In the example of the amplifier, it is desired to change the gain value. This can be achieved by different strategies, one of them by changing the width of the transistors of the input stage. The second concept is the **reconfiguration directive**, which establishes how the change established by the reconfiguration strategy is carried out. Using the same example, the reconfiguration directive would establish how the width of the transistors of the input stage is changed between operation modes.

Once these concepts have been clarified, the next question is how the idea of PoF can be extended to reconfigurable circuits. The proposed solution in this Thesis is based on the use of what we have called multi-mode Pareto-optimal Fronts (mm-PoFs). It is a new form of PoF that captures the reconfiguration capabilities of circuits. As previously discussed, dominance plays a central role in the definition and generation of PoFs. Obviously this concept has to be redefined for mm-PoFs. Let us consider the example shown in Fig.3.12, where two individuals that operate in 3 different operation modes are compared. As it can be seen, if the two design objectives are being minimized, all the modes of individual i are dominated by some mode of individual j and, thus, we can say that the individual i is dominated by individual j. However, a regular MOEA is not able to distinguish

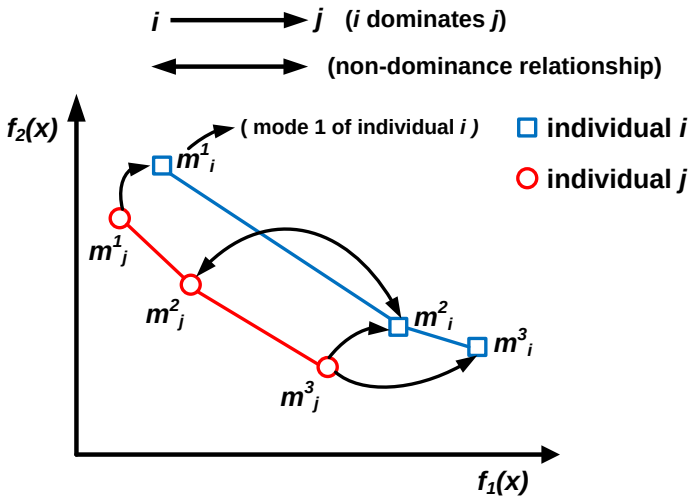


Figure 3.12: Multi-mode Pareto dominance example.

between operation modes and, thus, the optimization problem in this case would be equivalent to one with 6 design objectives (f_1 mode 1, f_2 mode 1, f_1 mode 2, and so on). This means that, when comparing two individuals, the comparison would be carried out only between the same corresponding modes, that is, mode 1 of individual i with mode 1 of individual j, and so on. As a result, a regular MOEA would decide that both individuals are non-dominated between them because it is not able to detect that mode 2 of individual i is dominated by mode 3 of individual j.

To solve these limitations of regular MOEAs, a new class of algorithms, able to perform a new multi-mode dominance check between individuals, is necessary to generate mm-PoFs of reconfigurable circuits. As it has been noted, mm-PoFs are the extension of the concept of PoFs to reconfigurable circuits. Therefore, mm-PoFs can be seen as solutions of a new type of problems, that we have named Multi-Mode MOOPs (M^3OOPs), where each solution, or individual, operates under different set-up conditions. Let us denote the operation for each set of conditions the "modes" of the individual and suppose we have m different operation modes. Then, each individual could be decomposed as follows:

$$ind_i \rightarrow \left(ind_i^1, ..., ind_i^m\right) \tag{3.12}$$

That is, each operation mode of each individual can be treated as an individual itself. Now it seems natural to think that each of those modes has its own design objectives and constraints. If in a MOOP we have a set of b design objectives, in a M^3OOPs we have a set of $m \times b$ design objectives:

$$\vec{f} = \{f_1, ..., f_b\} \rightarrow \vec{f} = \left\{f_1^1, ..., f_b^1, f_1^2, ..., f_b^2, ...f_b^1, ..., f_b^m\right\} \tag{3.13}$$

And the same reasoning can be applied to the set of constraints.

In addition, the set of design variables can be divided into the common design variables - those that are the same in all operation modes - and the reconfigurable design variables, which vary between the operation modes and are responsible for the reconfiguration of the circuit itself:

$$\vec{x} = \vec{x}^0 \cup \vec{r} = \left\{{x_1}^0, ..., {x_n}^0\right\} \cup \left\{r_1, ..., r_p\right\}, \tag{3.14}$$

where $\vec{x}^0$ is the set of common design variables and $\vec{r}$ the reconfigurable variables. For example, let us consider a low-pass filter that changes the value of the resistor to change the cut-off frequency for several operation modes. In this case, the resistor would be a reconfigurable variable and the rest of variables would be common to all operation modes.

3.2.1 *Multi-mode Evolutionary Algorithm*

In this section we will describe the new dominance criterion necessary to solve M^{3}OOPs (what we call multi-mode Pareto-dominance criterion), as well as the new algorithm that has been developed to implement this new dominance criterion. Let us consider a M^{3}OOPs where 2 design objectives ($f_1(\vec{x})$ and $f_2(\vec{x})$) must be maximized for 3 operation modes. First of all, from a designer's perspective, it is desired that circuit performances on each operation mode of the same individual are non-dominated between them. This is illustrated in Fig.3.13(a), where 3 operation modes of the same individual are depicted, and, as it can be seen, mode 3 is dominated by mode 1. Thus, a Pareto-dominance check must be done between the modes of each individual.

Second, when comparing two different individuals, the Pareto-dominance check must be done between all modes of the individuals cross-wise, that is, comparing all modes of each individual to all modes of all other individuals. Otherwise, as it has been explained, individuals may be marked as non-dominated between them when actually one of them is clearly better in terms of Pareto dominance. In Fig.3.13(b), two competing solutions are shown. As it is indicated, the two modes of individual 2 are dominated by mode 2 of individual 1 and, thus, individual 2 is dominated by individual 1. Therefore, multi-mode dominance criteria must contemplate two different aspects:

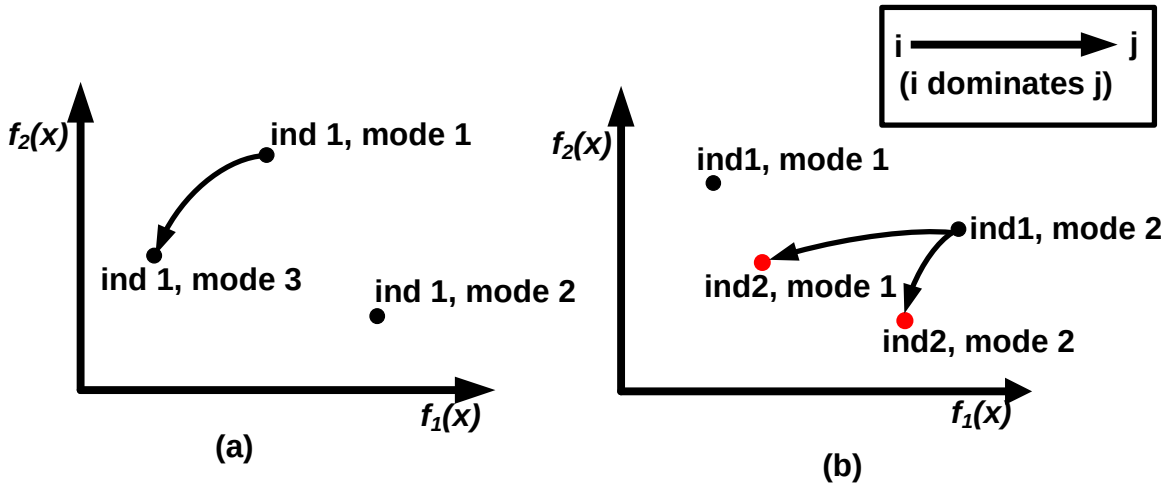


Figure 3.13: (a) Dominance between modes of the same individual (intra-individual dominance check). (b) Dominance between two competing solutions (inter-individual dominance check)

- **Intra-individual dominance**, which compares all modes of the same individual and identifies the dominated modes. The modes that are dominated by other modes of the same individual are called intra-dominated modes. As it has been stated, intra-dominated modes are useless and thus they will never be used.
- **Inter-individual dominance**, which compares between modes of different individuals. The dominated modes identified at this step are called inter-dominated modes.

Besides this new dominance criteria, other aspects of MOEAs like NSGA-II must be adapted to perform multi-mode optimization. This includes new definitions for the crowding distance and the constraint violation metrics. As explained in section 3.1.1, these are used in the selection of individuals from the parent population to form the offspring population and in the dominance check between individuals. The implementation of the new functions are detailed in the following paragraphs.

New Structure for the Individuals

New characteristics of the individuals must be defined so the algorithm can differentiate between the different operation modes. This can be seen in Fig.3.14.

- **Design variables:** as it has been said, they constitute the chromosome of the individual. For multi-mode optimization, they are classified into

regular variables, those which do not change between operation modes, and reconfigurable variables, which change between modes.

- **Design objectives, constraints and crowding distance** are defined for each operation mode separately. However, we also define a global constraint violation and crowding distance for each individual as the average value of them among the different operation modes.
- **Dominated modes** indicates the number of dominated modes of the individual. This value takes into accounts the modes dominated by both the same and by other individuals. This value will be used to compare individuals in several situations that will be described later on.

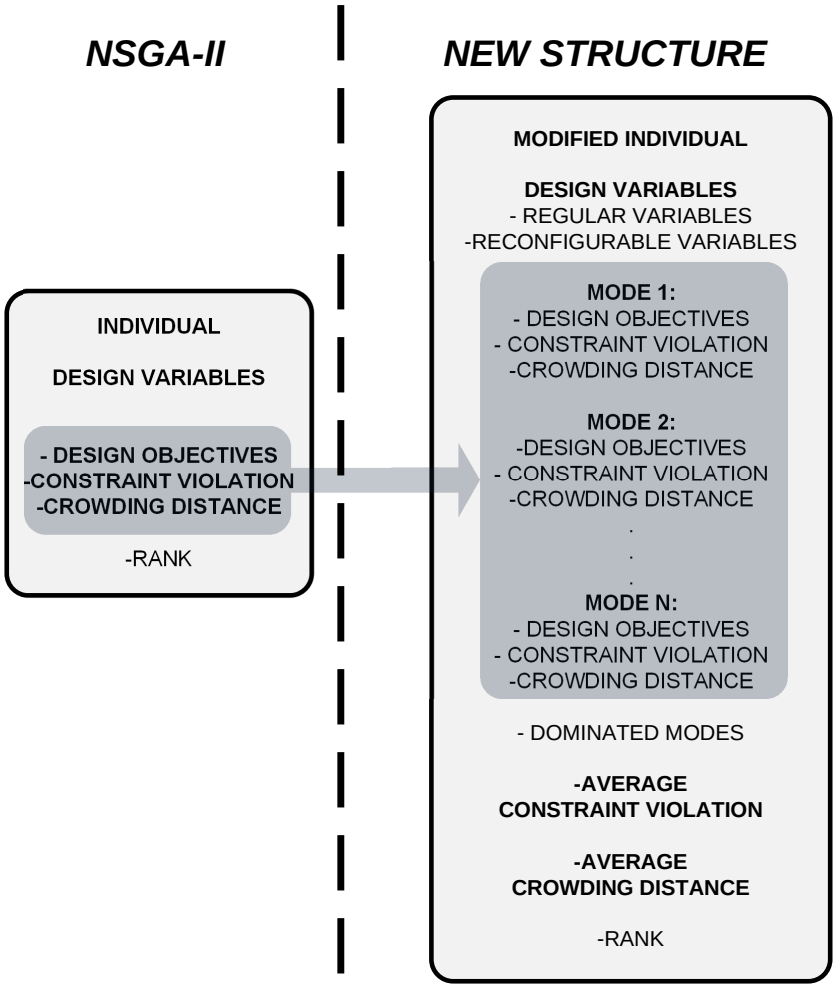


Figure 3.14: New structure of the individuals necessary for multi-mode optimization.

Intra-individual Dominance Check

The goal of this dominance check is to identify modes of an individual dominated by any of its other modes. The necessity for this is obvious: intra-dominated modes will be never desired or used and, thus, they must be identified and discarded. For a reconfigurable design, it is important that the different operation modes at least fulfill the design constraints. For this reason, in this check first the constraint violation of the modes is compared. If it is the same, or has zero value, then a Pareto-dominance comparison between the design objectives of the modes is carried out. The dominated modes are marked as "intra-dominated modes".

Inter-individual Dominance Check

This dominance check, which is performed between different individuals, is carried out exhaustively cross-wise, i.e., all modes of an individual are compared to all modes of another individual. First, each intra-dominated mode and those modes that violate constraints are marked as dominated modes. By doing so, these modes are not considered when checking the Pareto-dominance between the modes of the individuals, avoiding unnecessary checks. As depicted in the flow in Fig.3.15, different scenarios are possible when deciding which individual is dominant:

- **Case** 1**.** Both individuals violate constraints in all operation modes: in this case the one with smaller constraint violation is chosen as dominant. This scenario is quite common at early generations of the evolutionary process. By giving preference to individuals with smaller constraint violation we are helping the evolutionary process to move to feasible regions of the performance space.

- **Case** 2**.** One of the individuals violate constraints in all operation modes while the other fulfills constraints in at least one mode: the second one is chosen. As in the previous case, here we are giving preference to feasible designs over unfeasible ones. It is important to note that when these two first scenarios take place, the evolutionary process is still positioning itself in a feasible region of the performance space, and the optimization stage has not begun.

- **Case** 3**.** Both individuals fulfill constraints in at least one operation mode: in this case the constraint violation is compared (this helps the algorithm to achieve populations free of constraint violation). If it is the same for both individuals, then the number of dominated modes is compared. For this, we establish the multi-mode dominance criterion, which states that a multi-mode individual, $\vec{b}$, is dominated by another multi-mode individual, $\vec{a}$, if all operation modes of $\vec{b}$ are dominated by operation modes of $\vec{a}$. This definition implies that two multi-mode individuals are non-dominated if each has at least one mode that is not dominated by modes of the other individual.

There is a good reason behind this multi-mode dominance criterion. If an individual has at least one operation mode that is not dominated by any other mode of any other individual, that means that the individual is interesting from the point of view of a designer because, although the rest of modes of the individual are dominated, it has an operation mode that is good enough and, thus, the evolutionary algorithm should keep that individual.

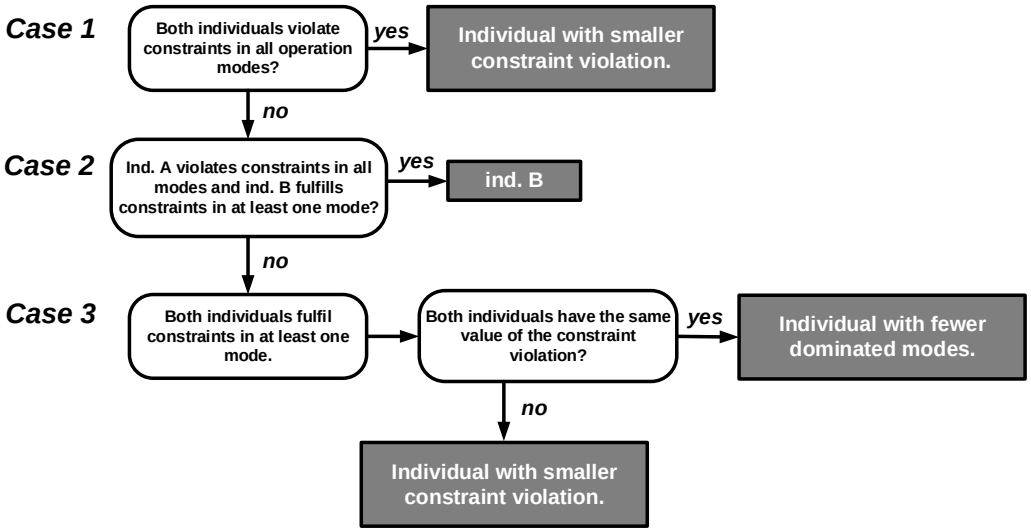


Figure 3.15: Possible cases in the inter-individual dominance check. Grey boxes indicate the individual that wins the dominance check.

In Fig.3.16 an example is shown where the modes of two individuals are compared (in this case there are not any intra-dominated modes). As it can be seen, mode 1 of individual 1 violates the design constraints while all the modes of individual 2 fulfills them. On the other hand, mode 2 of individual 1 dominates modes 1 and 2 of individual 2 and mode 3 of individual 1 dominates mode 3 of individual 2. As a result, individual 2 is dominated by individual 1.

New Tournament Selection Criteria

At this step, as explained in section 3.1.1, the best individuals of a population are selected to generate the individuals of the offspring population. This selection is carried out by chosing individuals of the parent population randomly, and comparing them with the inter-individual dominance check. If the individuals are non-dominated, then the one with larger crowding distance is selected. Afterwards, the selected individuals generate new individuals that will form the offspring population. For this, an auxiliary population is generated that stores each mode of

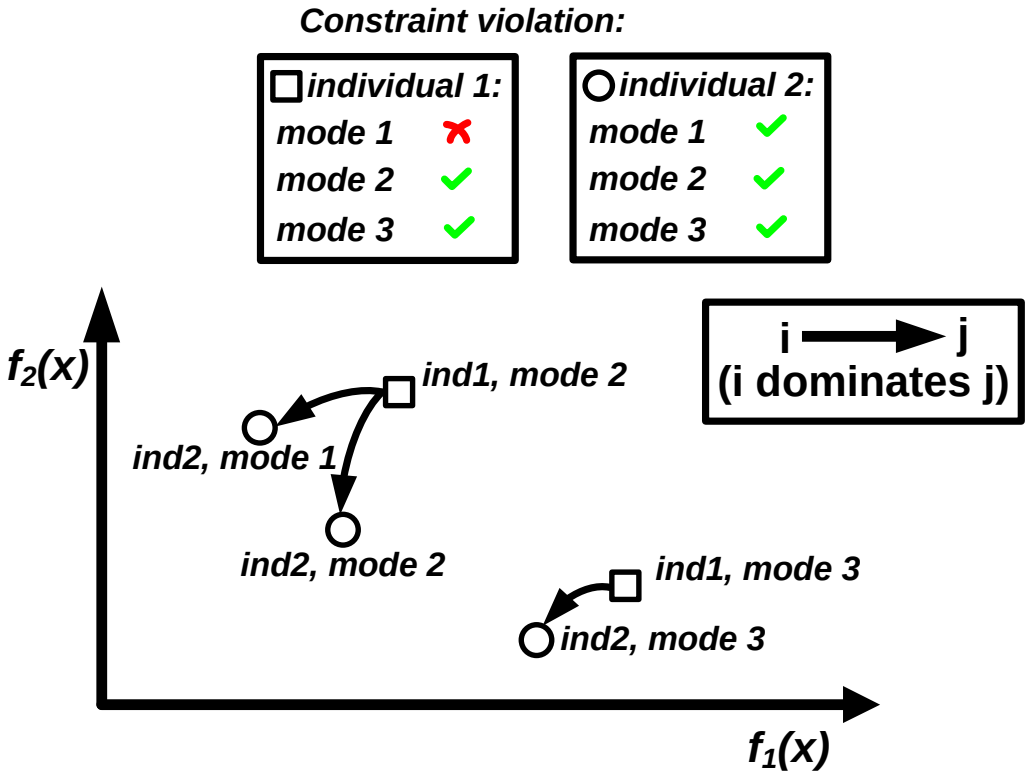


Figure 3.16: Inter-individual dominance check for 3 operation modes and 2 design objectives that are maximized. Only non intra-dominated modes that fulfill constraints are shown in this comparison.

each individual separately. By doing so, each mode of the multi-mode individuals can be handled as individuals themselves. The crowding distance is first calculated between the individuals of this auxiliary population. Later, the crowding distance of the multi-mode individuals is calculated as the average value of the crowding distance of its operation modes. An example is shown in Fig.3.17, where the crowding distance of three multi-mode individuals of two operation modes is calculated. As it can be seen, the modes of the individuals are overlapped, and, therefore, the distance between them must be measured separately, that is, as if the modes were independent individuals. Afterwards the global crowding distance of the multi-mode individual is defined as the average value of the distances of its modes. In this example, the crowding distance of individuals 1 and 3 is infinite because one of their operation modes are at one end of the front. The calculation of the crowding distance of the modes of individual 2 is also shown in the Figure.

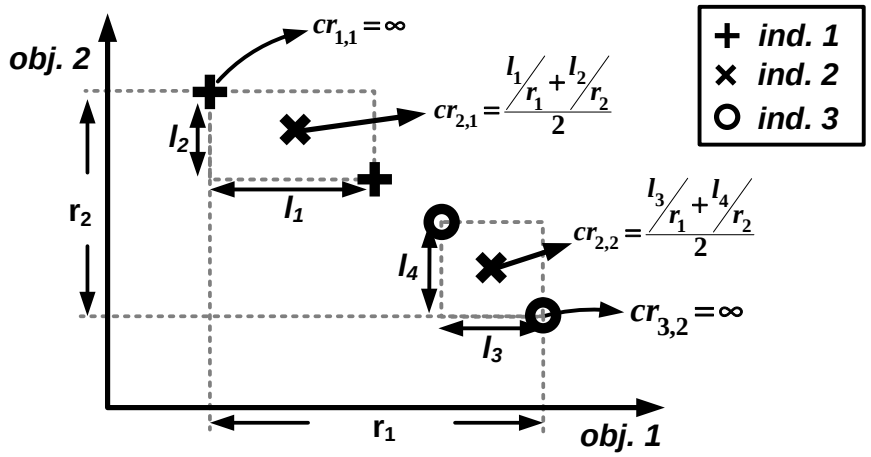


Figure 3.17: Example of multi-mode calculation of the crowding distance.

3.2.2 *Example: mm-PoF of a Reconfigurable Amplifier*

The same circuit from the previous section can be used to illustrate how to generate a mm-PoF for 2 operation modes. The circuit is intended to operate in different modes to provide greater bandwidth at the expense of the power consumption. In this case, the reconfigurable strategy will be the change of be the bias current (I_b), which will be the only reconfigurable variable. It will change from I_{bias} for operation mode 1 to $2 \times I_{bias}$ for operation mode 2. This is the reconfiguration directive. The reason behind this is that the unity-gain frequency (fu) is proportional to the transconductance of the input transistors:

$$f_u \propto g_{m1}/C_C \tag{3.15}$$

Since the transconductance of MOS transistors is proportional to the drain current, $g_m \propto \sqrt{I_d}$, it can be said that the fu of the amplifier is proportional to the bias current.

The design objectives and constraints, which are the same from previous section but for each operation mode, as well as details about reconfiguration strategies and directives, are shown in Table 3.4. Different projections of the generated mm-PoF are shown in Fig.3.18. It has been obtained for a population size of 1000 individuals and 100 generations of the optimization process. Blue crosses are performances of the reconfigurable designs operating in the first operation mode and red circles are those of the designs operating in the second operation mode. As depicted with the points connected with the black line, each pair of blue and red points represents the same individual.

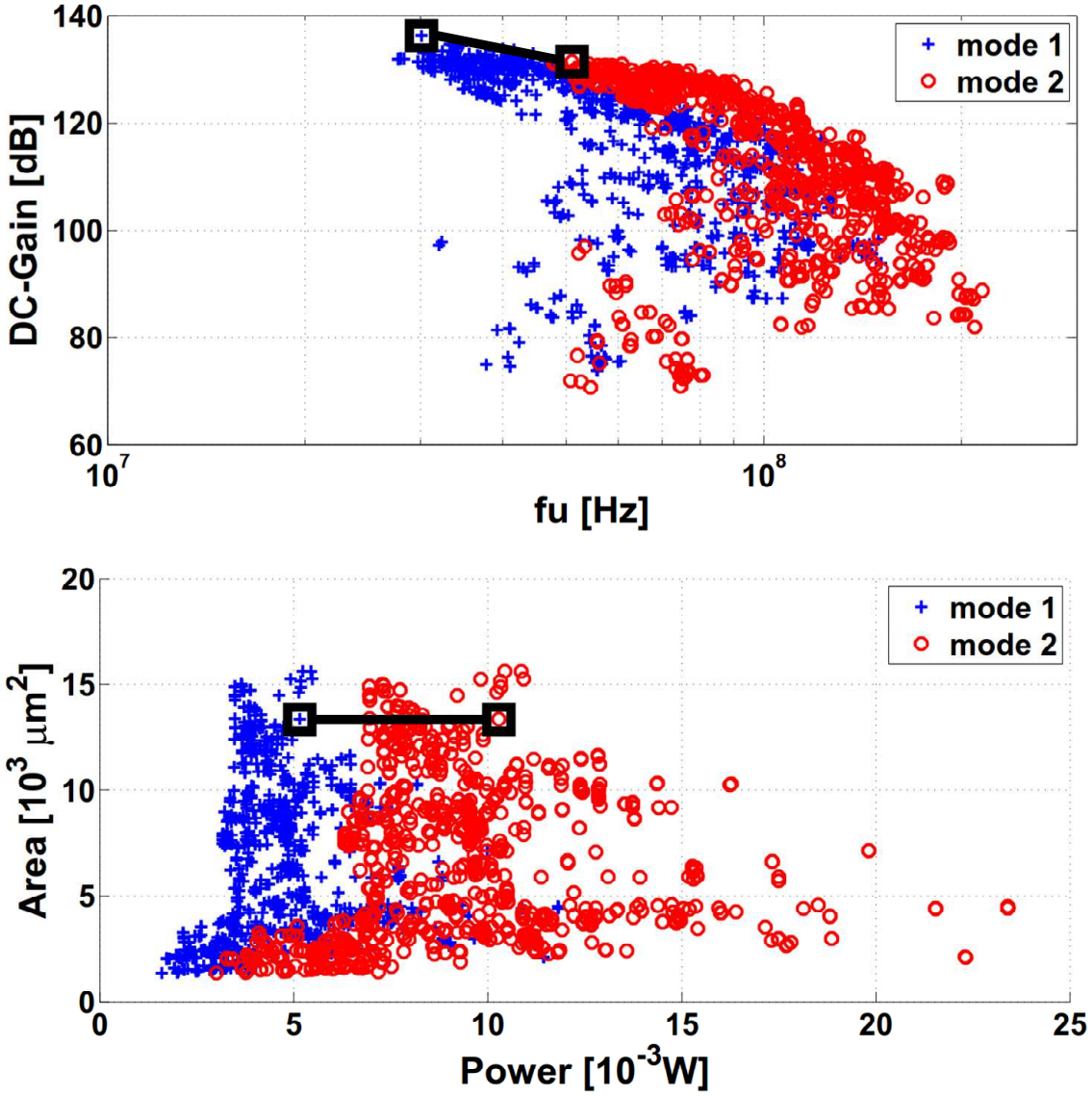


Figure 3.18: Projection of the mm-PoF onto the DC-Gain-fu and the power-area planes.

As it can be seen, as the reconfiguration directive consists in doubling the bias current, the mode 2 of the opamp provides greater fu, as expected. On the other hand, mode 2 consumes more power. This means that, for an application where two different specifications of fu are required, power consumption could be saved using reconfigurable designs, since the same amplifier could be used with a lower current for the lower fu (mode 1), and a higher current for the higher fu (mode 2) avoiding using a non-reconfigurable amplifier with the higher current that can fulfill the two fu specifications.

Table 3.4: Design objectives and Reconfigurability characteristics for the generation of the mm-PoF.

	MODE 1	**MODE 2**
Design Objectives	DC-Gain (*max*) fu (*max*) power (*min*) area (*min*)	DC-Gain (*max*) fu (*max*) power (*min*) area (*min*)
$\boldsymbol{I_{bias}}$	I_b	$2 \times I_b$

To illustrate the necessity for a new type of evolutionary algorithm to generate these mm-PoFs, let us consider an optimization problem for the same circuit but, for a better visualization, with only 2 design objectives (DC-Gain and fu) and 2 operation modes. Considering the same reconfiguration strategy and directive from the previous example, we try to generate the mm-PoF using the evolutionary algorithm NSGA-II and the new algorithm developed in this Thesis. In the first case, the optimization problem will be treated as a single-mode multi-objective optimization problem with 4 design objectives and 24 design constraints (the design constraints are the phase-margin, the output swing and the operation regime of all transistors). In the second scenario, where the new algorithm is used, the optimization problem will be treated as a multi-mode multi-objective optimization problem with 2 modes, each one with 2 design objectives and 12 design constraints.

The results provided by NSGA-II are shown in Fig.3.19. In order to check if this is effectively a mm-PoF, let us focus on the two highlighted multi-mode individuals. As it can be seen, one of them is dominated by the other: both modes of individual B are dominated by the second mode of individual A and, thus individual B is of no interest for the bottom-up design methodology presented here. This is due to the fact that, as there are two operation modes, the algorithm is optimizing four design objectives and is not able to compare the operation modes cross-wise. Unless it can be guaranteed that no individual such as B will be in the final front, it can not be said that these results represent the mm-PoF of the circuit under consideration. In this particular case, due to the reconfiguration strategy and directive, there is no intra-dominated modes (modes that are dominated by modes of the same individual). As it has been explained, increasing the bias current will always produce an increase of the unity-gain frequency and a decrease of the DC-Gain. For any other case, it would not be possible to guarantee that there would not be intra-dominated modes.

The mm-PoF provided by the new algorithm developed in this Thesis is shown in Fig.3.20. After examining the solutions of this front, neither inter-dominated

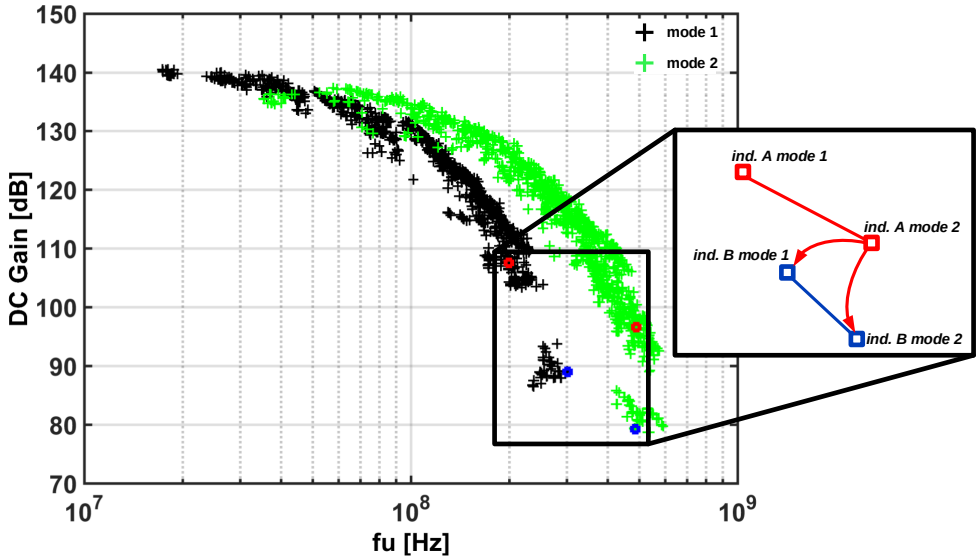


Figure 3.19: Mm-PoF generated using NSGA-II.

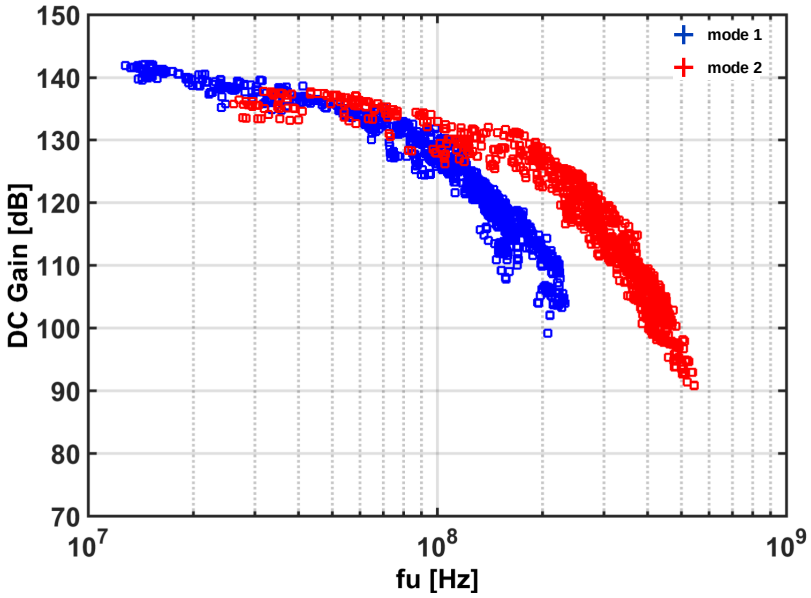


Figure 3.20: Mm-PoF generated using the evolutionary algorithm developed in this Thesis.

individuals nor intra-dominated modes are found. These results demonstrate the necessity of considering the new multi-mode dominance criterion, implemented in the new evolutionary algorithm that has been described in this Chapter. The problems illustrated in this simple example would be even worse when considering

3 or 4 design objectives, which is usual in circuit optimization problems. Moreover, when considering the hierarchical composition of mm-PoFs, these problems tend to accumulate, that is, a degradation of the PoF at one level will produce a degradation of the PoF at the next higher hierarchical level. This would lead, at the end, to something much worse than the mm-PoF of the system at the top-level that would be obtained using the new evolutionary algorithm.

3.3 RECONFIGURABLE VS. SINGLE-MODE CIRCUITS: APPLICATION

Advantages of the use of reconfigurable circuits in multi-standard scenarios were explained in Chapter 1. Let us illustrate these advantages by trying to solve an hypothetical problem with the use of the single-mode and multi-mode PoFs generated in this Chapter. In the case considered, the opamp of Fig.3.10 must fulfill the 2 sets of specifications defined in Table 3.5. These sets of specifications can be covered by three means: by one multi-mode design, where each operation mode covers one set of specifications; by one single mode design that covers the two sets simultaneously; or by two single mode solutions, each one covering one set of specifications. The PoF and mm-PoF of sections 3.1.2 and 3.2.2 will be used to search for valid solutions.

Table 3.5: Sets of specifications.

	$DC-Gain$ **[dB]**	fu **[MHz]**
spec set A	>110	>60
spec set B	>90	>100

The multi-mode designs from the mm-PoF that can be used and the single-mode designs from the single-mode PoF that fulfill both sets of specifications simultaneously are shown in Fig.3.21, where projections onto the DC-Gain-fu and area-power planes are represented. As it can be seen in Fig.3.21(b), there are multi-mode designs with a much better trade-off between the area and the power consumption than those of the valid single-mode designs. These multi-mode designs are connected with a black line in the Figure, and illustrate how the power consumption can be reduced while the circuit works in operation mode 1, using also a smaller area than the single mode designs. Even more, there are multi-mode solutions with lower power consumption in both operation modes than the single-mode solutions. This is due to the fact that the single-mode solutions that fulfill both sets of specifications are in the region with highest values of DC-Gain and fu and, therefore, the values of area and power consumption of those solutions are worse. Multi-mode solutions, on the other hand, present better area and power

consumption trade-offs because their operation modes do not have to fulfill the two sets of specifications.

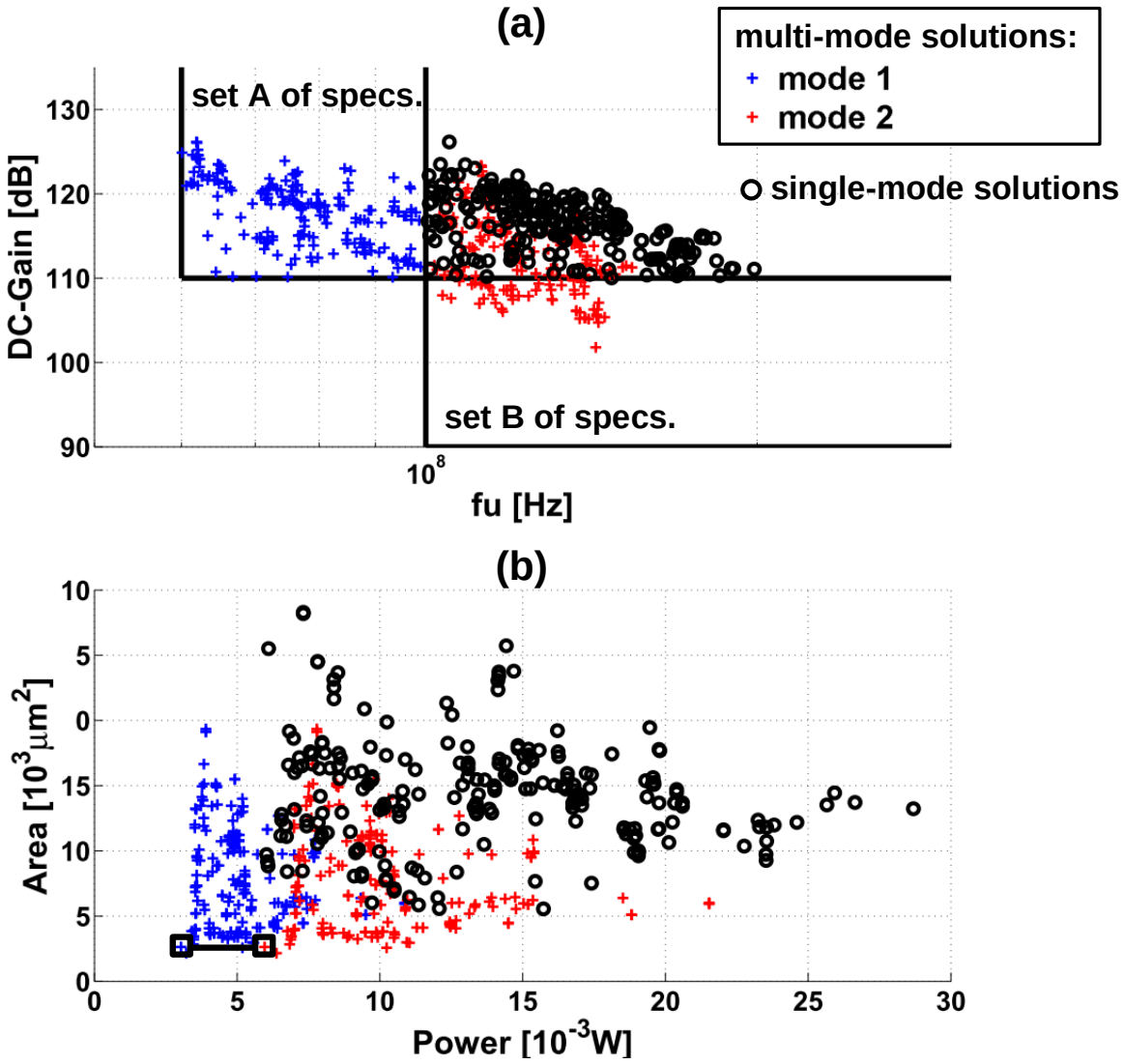


Figure 3.21: Performances of valid multi-mode solutions and single-mode solutions that fulfill both sets of specifications.

On the other hand, in Fig.3.22 the multi-mode designs from the mm-PoF that fulfill the two sets of specifications, and the solutions from the single-mode PoF that can be combined to fulfill the two sets of specifications are depicted together. That is, to fulfill the two sets of specifications using single-mode designs, a design that fulfills set A of specifications must be used with another design that fulfills set B of specifications. As it can be seen in Fig.3.22(b), there are single mode

designs with better area and power consumption trade-offs than some of the multi-mode solutions. However, as two single-mode solutions are required in this case (one black square for set A of specifications and other green square for set B of specifications) the total area of two single-mode solutions will be much larger and, thus, the use of a multi-mode design is a much better option.

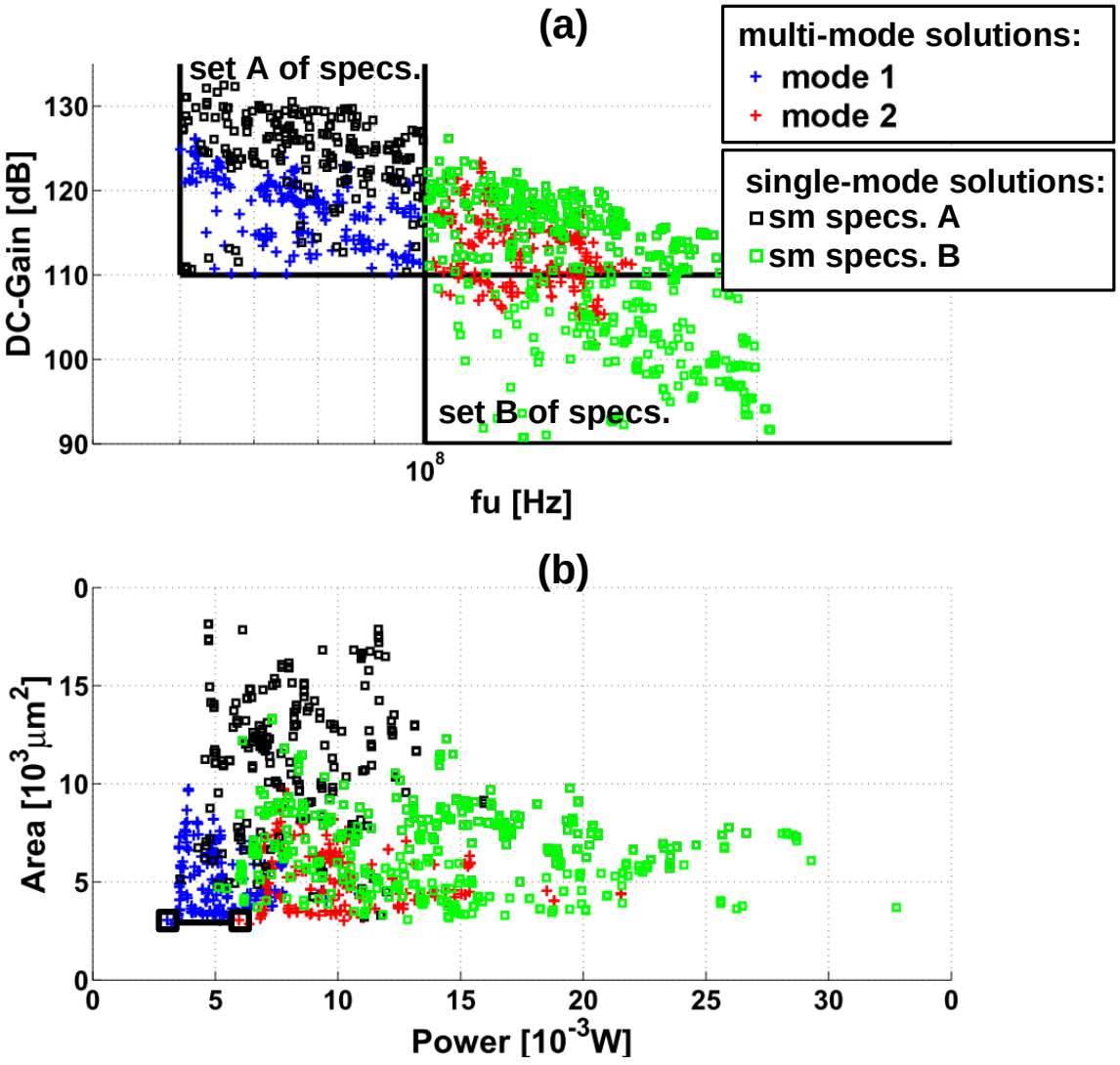


Figure 3.22: Performances of valid multi-mode solutions and single-mode solutions.

3.4 SUMMARY

In this Chapter a new evolutionary algorithm has been introduced. The algorithm is able to generate PoFs of reconfigurable analog circuits, which we have called multi-mode PoFs (mm-PoFs). This is one of the pillars the methodology presented in this Thesis is supported on. The next Chapter focuses in another pillar of the methodology, which is the composition of PoFs and mm-PoFs, from the bottom up to the top-level of the hierarchy in which an electronic system is decomposed. Two key issues of this hierarchical composition are covered here. The first one is related to the dependency of some performances of analog circuits with their surrounding circuitry. The second issue is related to the difficulty of integrating the exploration of the PoFs of low-level blocks into the generation of the PoF of higher-level blocks. New and efficient solutions are developed for both issues supported by experimental results.

4

HIERARCHICAL COMPOSITION OF PARETO-OPTIMAL FRONTS

One of the pillars of the methodology proposed in this Thesis is the generation of the PoFs and mm-PoFs of each building block at each level of the hierarchy in which a system has been decomposed. The method to generate the PoFs and mm-PoFs of basic building blocks has been described in chapter 3. At the next step of the methodology, these PoFs of basic building blocks must be used to generate the PoFs of higher-level blocks. That is, the PoFs of basic building blocks are part of the design space of the higher-level blocks. On the other hand, as explained in chapter 2, there are still open issues in the hierarchical composition of PoFs. The first issue is that some performances of analog circuits depend on their surrounding circuitry. This means that the PoFs of these circuits will be also different depending on those conditions. Therefore, a method that allows updating the PoFs of analog circuits and obtain the performances of their constitutive design points in different contexts is necessary in order to avoid the repetitive generation of PoFs each time different conditions are imposed. Besides, the method must guarantee that no loss of information occurs, that is, that the transformed PoF is equivalent to that which would be generated for the new conditions.

The second issue considered here concerning the hierarchical composition of PoFs is how they can be explored during the generation of PoFs of higher-level blocks. As it will be explained, a special type of design variables must be used to explore low-level PoFs efficiently. Here, several methods are considered and compared to each other in order to choose the best method that will be used in the experimental results of this Thesis.

4.1 CONTEXT DEPENDENT PERFORMANCES OF ANALOG CIRCUITS

Multi-objective bottom-up design methodologies rely on the one-time generation and composition of lower level PoFs, and assume that these hyper-surfaces[1] are independent of higher level performance specifications. However, some performances of some circuit blocks are dependent on their surrounding circuitry, like the dependence of many performances of many analog circuits on the loading conditions, i.e. the load connected at the output of the circuit. As these are not known until the low-level PoF designs are going to be used, this implies that, in these cases, the low-level PoFs should be generated multiple (hundreds or

1 A Pareto-optimal front forms a N-1 dimensional hyper-surface in the N-dimensional objective space.

thousands) times, depending on the population size and the number of generations for which the high-level PoF is generated. In particular, one of the most used blocks in any analog system is the amplifier, whose performances are very dependent on the loading conditions and will be used as an example. Regarding this specific problem, a technique able to transform a complete PoF of operational amplifiers, generated for some known loading conditions, to any other loading conditions, without using electrical simulators and thus reducing drastically the CPU time, is presented in [59].

The transformation technique can be used in different scenarios. For example, when the final loading conditions are known, that is, they are fixed from the beginning of the generation of the PoF of a complex block that uses PoFs of more basic blocks. In this case, the transformation technique has to be used only once at the beginning of the process to obtain the PoFs of amplifiers under those loading conditions. A different scenario would be a bottom-up methodology, where the final loading conditions are not known because they are part of the search space for the generation of the higher-level PoFs. In this case, the transformation technique has to be used dynamically during the generation of the higher-level PoFs. In the following lines, the transformation technique is explained in detail.

4.1.1 *Load Transformation Technique for Operational Amplifiers*

The goal of this transformation technique is to obtain the performances of an amplifier under some loading conditions without using electrical simulation. For this, the technique uses the known performances under other loading conditions where the circuit has been evaluated, as well as the poles and zeros of the gain and the output impedance under those loading conditions, to obtain the transfer function of the amplifier. Afterwards, using the transfer function and a representation of the circuit with the hybrid-2 parameters [60], it is possible to obtain the performances of the amplifier under any other loading conditions without additional electrical simulations. In this section this mechanism is explained in detail.

An operational amplifier can be viewed as a two-port like the one shown in Fig.4.1. Voltage v_1 and current i_1 represent the differential input voltage and current, respectively. Voltage v_2 and current i_2 represent the output voltage and current, respectively. A priori, any two-port matrix characterization of the amplifier can be considered. However, the two-port matrix parameters must be selected intelligently, so that a load-independent characterization of the operational amplifier can be obtained more easily. For this, a characterization with the hybrid-2 parameters fits perfectly:

Figure 4.1: Two-port representation of an operational amplifier.

$$\begin{aligned} i_1 &= h'_{11} \cdot v_1 + h'_{12} \cdot i_2 \\ v_2 &= h'_{21} \cdot v_1 + h'_{22} \cdot i_2 \end{aligned} \tag{4.1}$$

where h'_{11} is the input impedance, h'_{12} is the inverse current gain, h'_{21} represents the voltage gain of the amplifier without any load and h'_{22} is the output impedance. The voltage gain and output impedance when the load Z_L is considered, as shown in Fig.4.2, can be obtained from equation (4.1) and the constitutive equation:

$$v_2 = -Z_L \cdot i_2 \tag{4.2}$$

yielding the following expressions:

$$A_v(s) = \frac{h'_{21}(s)}{1 + \frac{h'_{22}(s)}{Z_L(s)}} \tag{4.3}$$

$$Z_o(s) = h'_{22}(s)$$

Equation 4.3 allows to obtain the hybrid-2 parameters h'_{21} and h'_{22} from the voltage gain, $A_v(s)$, and output impedance, $Z_o(s)$, for some known load conditions, and vice versa, to obtain the voltage gain $A_v(s)$ and output impedance $Z_o(s)$ for some other load from the hybrid-2 parameters h'_{21} and h'_{22}. Moreover, a particular case is when $Z_L \to \infty$. In this case, h'_{21} is identical to $A_v(s)$. This equation is the key to developing the technique, which proceeds as described in the following lines: (the process is also displayed in Fig.4.3.)

1. Generate the PoF of the performances of interest for some known load conditions.

2. For each individual of this PoF, store pole and zero locations of the $Z_o(s)$ and the voltage gain $A_v(s)$, both being frequency dependent functions, as well as their DC values. This information can be retrieved from common electrical simulators.

3. Use equations 4.3 to extract the hybrid parameters $h'_{21}(s)$ and $h'_{22}(s)$ for each individual; this means extracting DC values and both, poles and zeros. Note that, from basic circuit theory, the poles of $h'_{21}(s)$ and $h'_{22}(s)$ are identical.

4. Apply 4.3 to obtain the voltage gain $A_v(s)$ for the new arbitrary load conditions from the previously calculated hybrid parameters.

5. Obtain the performance parameters (DC-Gain, fu and phase margin(PM)) by simple processing of the magnitude and phase of the transfer function under the new loading conditions, $A_v(s)$.

Some of these steps are explained in more detail in the following lines. The pseudo-code of the transformation technique is given in APPENDIX II.

4.1.1.1 *Calculation of the hybrid-2 parameters*

As it has been explained, the gain of the amplifier for a given initial load can be expressed in terms of the hybrid-2 parameters:

$$A_v(s) = \frac{h'_{21}(s)}{1 + \frac{h'_{22}(s)}{Z^i_{LOAD}(s)}} \tag{4.4}$$

where $Z^i_{LOAD}(s) = \left[G^i_L + sC^i_L\right]^{-1}$.
As it has been said, function $h'^{(s)}_{22}$ is the output impedance:

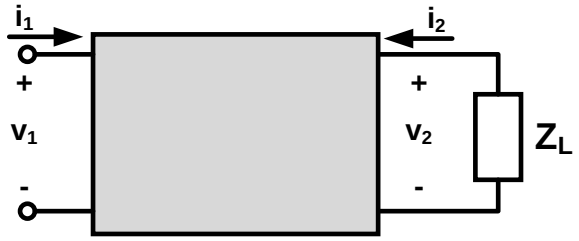


Figure 4.2: Two-port with an arbitrary load.

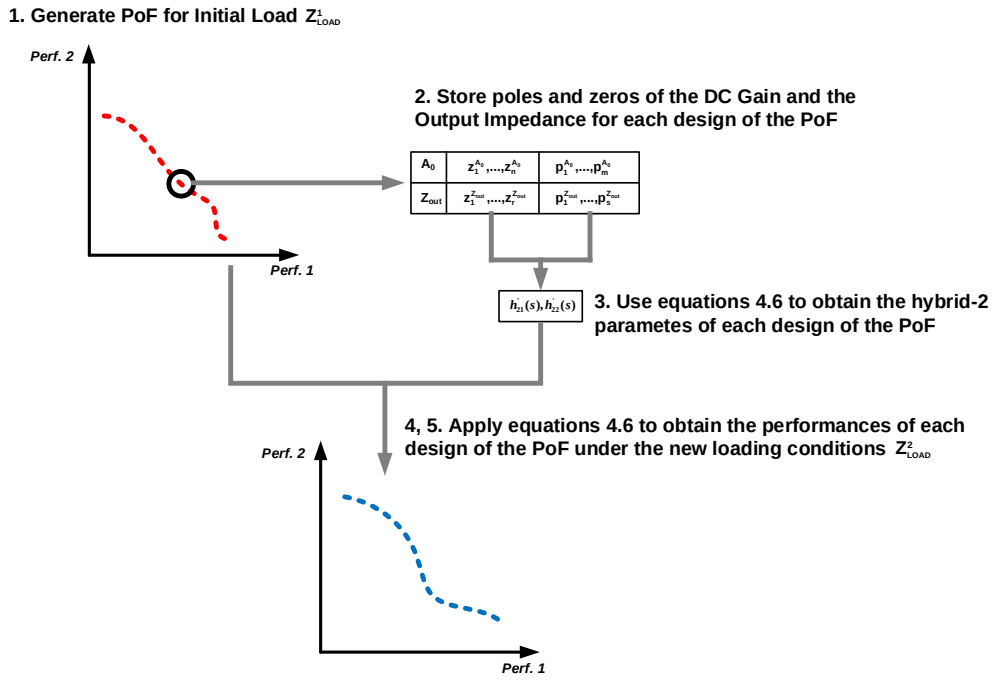


Figure 4.3: Steps to transform a PoF from initial load Z^1_{LOAD} to Z^2_{LOAD}.

$$h'_{22}(s) = Z_{out}(s) = K_{Zout}\frac{\prod(s - zr_j)}{\prod(s - pr_j)} \tag{4.5}$$

where zr_j and pr_j are the zeros and poles of the output impedance. Since the transfer function for the initial load impedance is known, the function $h'_{21}(s)$ can be extracted from 4.4:

$$h'_{21}(s) = \frac{K \cdot Z^i_{LOAD}(s) \cdot \prod(s - pr_j) + K \cdot K_{Zout} \cdot \prod(s - zr_j) \cdot \prod(s - z_j)}{Z^i_{LOAD}(s) \cdot \prod(s - pr_j) \cdot \prod(s - p_j)} \tag{4.6}$$

where K is a constant value and p_j and z_j and the poles and zeros of the gain.

4.1.1.2 *Calculation of the performances in the final loading conditions*

The transfer function for an arbitrary load can be obtained by simply substituting Eq.4.6 into Eq.4.4:

$$A_v^f(s) = \frac{h'_{21}(s)}{1 + \frac{h'_{22}}{Z^f_{LOAD}(s)}} = \\ = K \cdot Z^f_{LOAD}(s) \cdot \prod (s - pr_j) \frac{Z^i_{LOAD}(s) \cdot \prod (s - pr_j) + K_{Zout} \cdot \prod (s - zr_j) \cdot \prod (s - z_j)}{Z^f_{LOAD}(s) \cdot \prod (s - pr_j) + K_{Zout} \cdot \prod (s - zr_j)} \tag{4.7}$$

where $Z^f_{LOAD}(s)$ is the final load impedance and K and K_{Zout} can be obtained from the poles and zeros of the gain and the output impedance, as well as from their DC values:

$$K = A_{DC} \frac{\prod (-p_j)}{\prod (-z_j)} \\ K_{Zout} = Z^{DC}_{Out} \frac{\prod (-pr_j)}{\prod (-zr_j)} \tag{4.8}$$

where Z^{DC}_{Out} is the DC value of the output impedance.

The performances under the new loading conditions can be obtained by processing the transfer function. The DC-Gain is obtained for $s = 0$:

$$A^f_{DC} = A^0_{DC} \frac{\prod (-p_j) \prod (-pr_j)}{\prod (-z_j)} \frac{1 + G^i_L \cdot Z^{DC}_{out} \cdot \prod (-z_j)}{G^i_L + G^i_L \cdot G^f_L \cdot Z^{DC}_{out}} \tag{4.9}$$

where A^0_{DC} is the DC value of the initial gain and G^f_L is the transconductance of the final load impedance. The unity-gain frequency, on the other hand, is calculated by searching the frequency at which the magnitude of the transfer function is 1. For this, the Bolzano's Theorem [61] is applied. Finally, the phase-margin is obtained by adding the contribution of each pole and each zero of the transfer function at the unity-gain frequency.

The results provided by the transformation technique are very accurate, as it will be shown below. Besides, the required CPU time to evaluate the circuits under the new load is much smaller than that used by transistor-level electrical simulators. These advantages will be clearer in the example presented next.

4.1.2 *Application example*

Let us consider the PoF of the amplifier in section 3.1.2 of chapter 3, which was generated for a load of a 20k Ω resistor and a 1.0 pF capacitor. The front will

be transformed to the new loading conditions of the parallel connection of a 10 kΩ resistor and a 2.5 pF capacitor. This will be done by HSPICE® simulation and by using the transformation technique described here. The front for the new loading conditions obtained with the transformation and by HSPICE® simulation are shown in Fig.4.4.

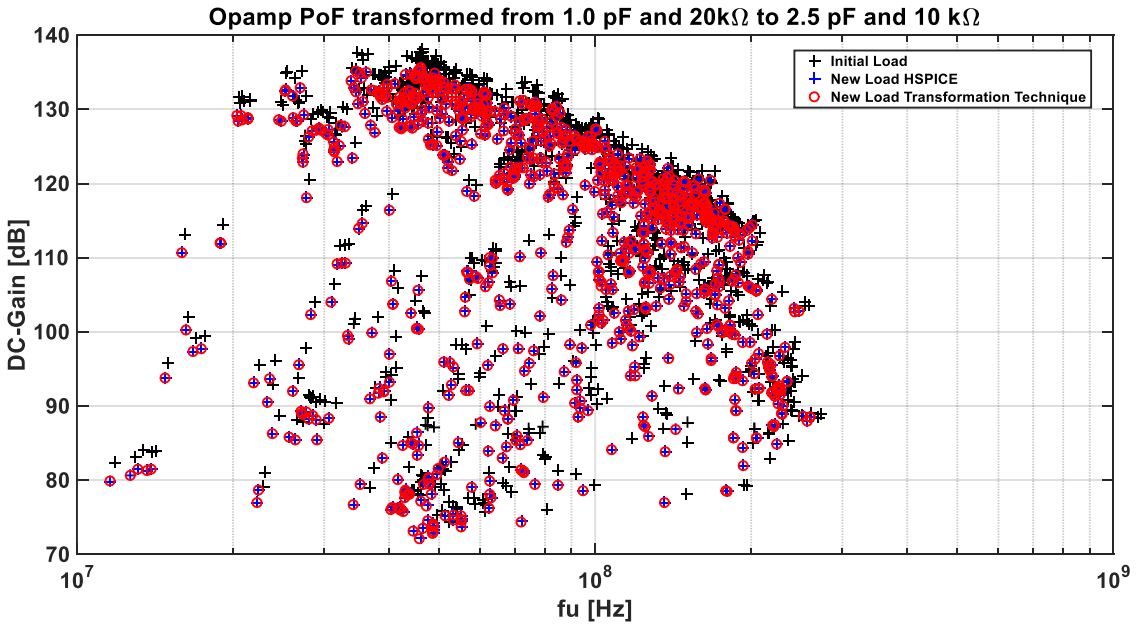


Figure 4.4: Projection of the PoF of the amplifier, both in the initial and in the final loading conditions.

As it can be seen, the new values of the performances provided by the transformation technique and by the HSPICE® simulation are practically identical. The transformation technique takes around 2.0 seconds to obtain the new values for the 1000 individuals of the opamp front. On the other hand, the evaluation of the same solutions for the new loading conditions by using HSPICE® simulator takes 38 seconds. It is important to note that this value is obtained by using a data-sweep analysis, which allows to evaluate all the solutions in the opamp front within a single run of the evaluator. This technique, as explained in section 3.1.2 of chapter 3, reduces significantly the CPU time of the evaluation.

Although 38 seconds may seem a quite acceptable time, let us see this number under a different light, with the optimization of a higher-level block, where the fronts of amplifiers must be explored and let us consider that the optimization is done with a population of 100 individuals. Each time a new individual is generated, the opamp fronts must be transformed to the new conditions imposed by the rest

of design variables of that individual. This means that, at each generation of the optimization process, up to 100 re-evaluations of the performances of the fronts may be required. That is 63.3 minutes if the re-evaluations are done with HSPICE® simulator. On the other hand, the load transformation technique would take only 3.3 minutes. This allows to use the technique when opamp fronts must be used in a hierarchical composition of PoFs without impacting the CPU time.

So far we have not considered an important aspect that is key for the transformation technique to be valid. This transformation technique assumes that no loss of information happens when transforming a PoF to a different load. That is, it assumes that all the information of the PoF in the final loading conditions can be obtained from the PoF in the initial loading conditions. But for this to be true we must be able to guarantee that a dominated point in the initial objective space is not transformed into a non-dominated point of the final objective space, since in the technique we are using, only dominated points of the initial PoF are being transformed. This means that, if some individuals of the PoF under the new loading conditions came from points of the performance space dominated by their PoF, they would never be available with this transformation technique and, thus, we would lose information.

In order to obtain the conditions under which it can be guaranteed that there is not any loss of information when transforming a PoF to different loading conditions, we are going to consider a PoF with two design objectives in the initial and final space. And we are going to consider the partial derivatives of each objective in the final space with respect to the objectives in the initial space:

$$\left.\frac{\delta f_1}{\delta g_1}\right|_{x_f} \quad , \quad \left.\frac{\delta f_1}{\delta g_2}\right|_{x_f} \tag{4.10}$$

$$\left.\frac{\delta f_2}{\delta g_1}\right|_{x_f} \quad , \quad \left.\frac{\delta f_2}{\delta g_2}\right|_{x_f}$$

where f_1 and f_2 are the objectives in the final space, g_1 and g_2 are the objective in the initial space, and x_f is a point in the final space. Let us consider that all partial derivatives are non-negative and that at least one is strictly positive:

$$\left.\frac{\delta f_1}{\delta g_1}\right|_{x_f} > 0 \quad , \quad \left.\frac{\delta f_1}{\delta g_2}\right|_{x_f} \geq 0 \tag{4.11}$$

$$\left.\frac{\delta f_2}{\delta g_1}\right|_{x_f} \geq 0 \quad , \quad \left.\frac{\delta f_2}{\delta g_2}\right|_{x_f} \geq 0$$

Assume that a dominated point in the initial space is mapped to a sample of the PoF in the final space. If these derivatives are non-negative, this means that if the dominated point in the initial space is shifted in the direction at which g_1 and g_2 increase, the mapped point in the final space will shift in the direction at which objectives f_1 and f_2 also increase. But this is contradictory with the fact that the mapped point was in the PoF since it is dominated by the shifted point. Therefore, these conditions guarantee that there is no loss of information.

Suppose now that the derivatives of one of the objectives in the final space are non-positive and that at least one derivative is strictly negative:

$$\left.\frac{\delta f_1}{\delta g_1}\right|_{x_f} \geq 0 \quad , \quad \left.\frac{\delta f_1}{\delta g_2}\right|_{x_f} \geq 0 \tag{4.12}$$

$$\left.\frac{\delta f_2}{\delta g_1}\right|_{x_f} \leq 0 \quad , \quad \left.\frac{\delta f_2}{\delta g_2}\right|_{x_f} \leq 0$$

In this case, we cannot guarantee that the dominated point does not map to a point of the PoF in the final space.

Assume now that the derivatives of f_1 and f_2 with respect to g_1 are non-negative, and one of them is strictly positive:

$$\left.\frac{\delta f_1}{\delta g_1}\right|_{x_f} \geq 0 \quad , \quad \left.\frac{\delta f_1}{\delta g_2}\right|_{x_f} \leq 0 \tag{4.13}$$

$$\left.\frac{\delta f_2}{\delta g_1}\right|_{x_f} \geq 0 \quad , \quad \left.\frac{\delta f_2}{\delta g_2}\right|_{x_f} \leq 0$$

In this case, if we shift the dominated point in the direction at which g_1 increases and g_2 does not change, the mapped point in the final space will shift in the direction at which f_1 and f_2 increase. But this is, once again, contradictory with the assumption that the point was in the PoF. Therefore, this condition is sufficient to guarantee that we are not losing information.

We can also analyze the situation in which the derivative of f_1 with respect to g_1 and the derivative of f_2 with respect to g_2 are non-negative:

$$\left.\frac{\delta f_1}{\delta g_1}\right|_{x_f} \geq 0 \quad , \quad \left.\frac{\delta f_1}{\delta g_2}\right|_{x_f} \leq 0 \tag{4.14}$$

$$\left.\frac{\delta f_2}{\delta g_1}\right|_{x_f} \leq 0 \quad , \quad \left.\frac{\delta f_2}{\delta g_2}\right|_{x_f} \geq 0$$

After some manipulation of Eq.4.31 we arrive at:

$$\left|\frac{\delta f_1}{\delta g_1}\right| - \left|\frac{\delta f_1}{\delta g_2}\right| > \left|\frac{\delta f_2}{\delta g_1}\right| - \left|\frac{\delta f_2}{\delta g_2}\right| \tag{4.15}$$

However, this condition is difficult to check in practical situations. Therefore, we are going to consider that a sufficient condition is that the **derivatives of the objectives in the final space are non-negative in at least one of the objectives in the initial space, and that at least one of them is strictly positive.**

In our case, we are dealing with four objectives: DC-Gain, Unity-gain frequency (fu), phase-margin and DC output impedance. The first step to find the conditions we are looking for is, thus, to obtain analytical expressions of the objectives in the final space with respect to those in the initial space and then see if the condition stated above holds true. Let us consider a two-pole model for the voltage gain of the amplifier with the initial and the final loading conditions shown in the following equation:

$$A_{vi}(s) = \frac{A_{ddi}}{\left(1+\frac{s}{p_{1i}}\right)\left(1+\frac{s}{p_{2i}}\right)} \tag{4.16}$$

$$A_{vf}(s) = \frac{A_{ddf}}{\left(1+\frac{s}{p_{1f}}\right)\left(1+\frac{s}{p_{2f}}\right)}$$

where subscripts i and f refer to initial and final, respectively.

On the other hand, the voltage gain of the amplifier without any load and the output impedance can be expressed, considering also the two-pole model:

$$h'_{21}(s) = \frac{A_{ddNL}}{\left(1+\frac{s}{p_{NL1}}\right)\left(1+\frac{s}{p_{NL2}}\right)} \tag{4.17}$$

$$h'_{22}(s) = \frac{Z_o\left(1+\frac{s}{z_{ozero}}\right)}{\left(1+\frac{s}{p_{NL1}}\right)\left(1+\frac{s}{p_{NL2}}\right)}$$

Taking this and equation 4.3 into account, and assuming an output load represented by a capacitor and a resistor, the voltage gain with the initial and the final loads can be expressed as shown in equation 4.18.

$$A_{vi}(s) = \frac{A_{ddNL}}{\left(1+\frac{s}{p_{NL1}}\right)\left(1+\frac{s}{p_{NL2}}\right) + Z_o\left(1+\frac{s}{z_{ozero}}\right)(sC_{Li}+G_{Li})} \tag{4.18}$$

$$A_{vf}(s) = \frac{A_{ddNL}}{\left(1+\frac{s}{p_{NL1}}\right)\left(1+\frac{s}{p_{NL2}}\right) + Z_o\left(1+\frac{s}{z_{ozero}}\right)(sC_{Lf}+G_{Lf})}$$

By equating equations 4.16 and 4.18 at low frequencies:

$$A_{ddi} = \frac{A_{ddNL}}{1+Z_oG_{Li}} \tag{4.19}$$

$$A_{ddf} = \frac{A_{ddNL}}{1+Z_oG_{Lf}}$$

From equation 4.19, the voltage gain at the final loading conditions can be expressed in terms of the voltage gain at the initial loading conditions:

$$A_{ddf} = \frac{A_{ddi}\,(1+Z_oG_{Li})}{1+ZoG_{Lf}} \tag{4.20}$$

The gain bandwidth product and the tangent of the phase margin are:

$$GB = A_{dd}\cdot|p_1| \tag{4.21}$$

$$tan\,(PM) = tp = \frac{|p_2|}{A_{dd}\cdot|p_1|}$$

Analytical expressions for the two poles of the amplifier can be obtained by equating the expressions for the voltage gain in the initial loading conditions in equations 4.16 and 4.18. This leads to:

$$\left(1+\frac{s}{p_{NL1}}\right)\left(1+\frac{s}{p_{NL2}}\right)=\frac{A_{ddNL}\left(1+\frac{s}{p_{1i}}\right)\left(1+\frac{s}{p_{2i}}\right)}{A_{ddi}}-Z_o\left(1+\frac{s}{z_{ozero}}\right)\left(sC_{Li}+G_{Li}\right) \tag{4.22}$$

Replacing this in the expression for the voltage gain in the final loading conditions in equation 4.18 we obtain:

$$A_{vf}=\frac{A_{ddNL}}{\frac{A_{ddNL}}{A_{ddi}}\left(1+\frac{s}{p_{1i}}\right)\left(1+\frac{s}{p_{2i}}\right)Z_o\left(1+\frac{s}{z_{ozero}}\right)\left[s\left(C_{Lf}-C_{Li}\right)+\left(G_{Lf}-G_{Li}\right)\right]} \tag{4.23}$$

Assuming that the poles of equation 4.23 are split enough, which happens in the cases of interest, they can be obtained as the ratio of the polynomial coefficients:

$$p_{1f}=\frac{\frac{A_{ddNL}}{A_{ddi}}+Z_o\left(G_{Lf}-G_{Li}\right)}{\frac{A_{ddNL}}{A_{ddi}}\left(\frac{1}{p_{1i}}+\frac{1}{p_{2i}}\right)+\frac{Z_o}{z_{ozero}}\left(G_{Lf}-G_{Li}\right)+Z_o\left(C_{Lf}-C_{Li}\right)} \tag{4.24}$$

$$p_{2f}=\frac{\frac{A_{ddNL}}{A_{ddi}}\left(\frac{1}{p_{1i}}+\frac{1}{p_{2i}}\right)+\frac{Z_o}{z_{ozero}}\left(G_{Lf}-G_{Li}\right)+Z_o\left(C_{Lf}-C_{Li}\right)}{\frac{A_{ddNL}}{A_{ddi}}\frac{1}{p_{1i}p_{2i}}+\frac{Z_o}{z_{ozero}}\left(C_{Lf}-C_{Li}\right)}$$

Replacing equations 4.20 and 4.21:

$$p_{1f}=\frac{1+Z_oG_{Lf}}{\left(1+Z_oG_{Li}\right)\left(\frac{A_{ddi}}{GB_i}+\frac{1}{GB_i\cdot tp}\right)+\frac{Z_o}{z_{ozero}}\left(G_{Lf}-G_{Li}\right)+Z_o\left(C_{Lf}-C_{Li}\right)} \tag{4.25}$$

$$p_{2f}=\frac{\left(1+Z_oG_{Li}\right)\left(\frac{A_{ddi}}{GB_i}+\frac{1}{GB_i\cdot tp}\right)+\frac{Z_o}{z_{ozero}}\left(G_{Lf}-G_{Li}\right)+Z_o\left(C_{Lf}-C_{Li}\right)}{\left(1+Z_oG_{Li}\right)\frac{A_{ddi}}{GB_i^2\cdot tp}+\frac{Z_o}{z_{ozero}}\left(C_{Lf}-C_{Li}\right)}$$

Therefore, the gain bandwidth product and the tangent of the phase-margin in the final loading conditions can be expressed:

$$GB_f = \frac{A_{ddf}\left(1 + Z_o G_{Li}\right)}{\left(1 + Z_o G_{Li}\right)\left(\frac{A_{ddi}}{GB_i} + \frac{1}{GB_i \cdot tp}\right) + \frac{Z_o}{z_{ozero}}\left(G_{Lf} - G_{Li}\right) + Z_o\left(C_{Lf} - C_{Li}\right)} \tag{4.26}$$

$$tp_f = \frac{\left[\left(1 + Z_o G_{Li}\right)\left(\frac{A_{ddi}}{GB_i} + \frac{1}{GB_i \cdot tp_i}\right) + \frac{Z_o}{z_{ozero}}\left(G_{Lf} - G_{Li}\right) + Z_o\left(C_{Lf} - C_{Li}\right)\right]^2}{A_{ddi}\left(1 + Z_o G_{Li}\right)\left[\left(1 + Z_o G_{Li}\right)\frac{A_{ddi}}{GB_i^2 \cdot tp_i} + \frac{Z_o}{z_{ozero}}\left(C_{Lf} - C_{li}\right)\right]}$$

Now that we have obtained the objectives under the final loading conditions as functions of the objectives in the initial loading conditions, the signs of the derivatives of the four performances at the final performance space with respect to the same performances of the original load conditions have to be studied. Here, we can consider the tangent of the phase margin instead of the phase margin itself since the sign of both derivatives is the same. If we consider the derivative of the phase margin at the final loading conditions with respect to any performance at the original loading conditions:

$$\frac{\delta PM}{\delta f} = \frac{\delta PM}{\delta tp}\frac{\delta tp}{\delta f} = \frac{1}{1 + tp^2}\frac{\delta tp}{\delta f} \tag{4.27}$$

it becomes clear that the sign of both derivatives is the same.

If, on the other hand, we consider the derivative of any performance at the final loading conditions with respect to the phase margin at the original performance space:

$$\frac{\delta f}{\delta PM} = \frac{\delta f}{\delta tp}\frac{\delta tp}{\delta PM} = \frac{1}{\left[cos\left(PM\right)\right]^2}\frac{\delta f}{\delta tp} \tag{4.28}$$

it also becomes clear that the sign of both derivatives is the same.

Let us now look at the derivatives of the different performance objectives for the final load conditions. The DC output impedance is independent of the loading conditions, $Z_{of} = Z_{oi} = Z_o$. Therefore:

$$\frac{\delta Z_{of}}{\delta A_{ddi}} = 0; \frac{\delta Z_{of}}{\delta Z_{oi}} = 1; \frac{\delta Z_{of}}{\delta GB_i} = 0; \frac{\delta Z_{of}}{\delta tp_i} = 0 \tag{4.29}$$

If we consider the derivatives of the DC-Gain:

$$\frac{\delta A_{ddf}}{\delta A_{ddi}} = \frac{1 + Z_o G_{Li}}{1 + Z_o G_{Lf}}$$

$$\frac{\delta A_{ddf}}{\delta Z_{oi}} = \frac{A_{ddi}\left(G_{Li} - G_{Lf}\right)}{\left(1 + Z_o G_{Lf}\right)^2} \tag{4.30}$$

$$\frac{\delta A_{ddf}}{\delta GB_i} = 0$$

$$\frac{\delta A_{ddf}}{\delta tp_i} = 0$$

The first equation in 4.30 is always positive. For the second equation to be non-positive -consider that the DC-Gain is maximized but the output impedance is minimized- it must be verified that:

$$G_{Lf} \geq G_{Li} \tag{4.31}$$

Let us consider now the derivatives of the gain-bandwidth product. Its derivative with respect to the DC-Gain is:

$$\frac{\delta GB_f}{\delta A_{ddi}} = \frac{\left(1 + Z_o G_{Li}\right)\left[\frac{1+Z_o G_{Li}}{GB_i \cdot tp_i} + \frac{Z_o}{z_{ozero}}\left(G_{Lf} - G_{Li}\right) + Z_o\left(C_{Lf} - C_{Li}\right)\right]}{\left[\left(1 + Z_o G_{Li}\right)\left(\frac{A_{ddi}}{GB_i} + \frac{1}{GB_i \cdot tp_i}\right) + \frac{Z_o}{z_{ozero}}\left(G_{Lf} - G_{Li}\right) + Z_o\left(C_{Lf} - C_{Li}\right)\right]^2} \tag{4.32}$$

This derivative is guaranteed to be positive if:

$$\begin{aligned} G_{Lf} &\geq G_{Li} \\ C_{Lf} &\geq C_{Li} \end{aligned} \tag{4.33}$$

The derivative with respect to the gain-bandwidth product is:

$$\frac{\delta GB_f}{\delta GB_i} = \frac{A_{ddi}\left(1 + Z_o G_{Li}\right)^2\left(\frac{A_{ddi}}{GB_i}\right) + \frac{1}{GB_i \cdot tp_i}}{\left[\left(1 + Z_o G_{Li}\right)\left(\frac{A_{ddi}}{GB_i} + \frac{1}{GB_i \cdot tp_i}\right) + \frac{Z_o}{z_{ozero}}\left(G_{Lf} - G_{Li}\right) + Z_o\left(C_{Lf} - C_{Li}\right)\right]^2} \tag{4.34}$$

which is always positive.

The derivative with respect to the output impedance is:

$$\frac{\delta GB_f}{\delta Z_o} = \frac{-A_{ddi}\left[\frac{1}{z_{ozero}}\left(G_{Lf}-G_{Li}\right)+\left(C_{Lf}-C_{Li}\right)\right]}{\left[\left(1+Z_oG_{Li}\right)\left(\frac{A_{ddi}}{GB_i}+\frac{1}{GB_i\cdot tp_i}\right)+\frac{Z_o}{z_{ozero}}\left(G_{Lf}-G_{Li}\right)+Z_o\left(C_{Lf}-C_{Li}\right)\right]^2} \tag{4.35}$$

Once again, in this case the Gain-bandwidth product is usually maximized and, as said before, the output impedance is usually minimized. Thus, this derivative is guaranteed to be non-positive if:

$$\begin{aligned} G_{Lf} &\geq G_{Li} \\ C_{Lf} &\geq C_{Li} \end{aligned} \tag{4.36}$$

Finally, the derivative with respect to the tangent of the phase-margin is:

$$\frac{\delta GB_f}{\delta tp_i} = \frac{A_{ddi}\left(1+Z_oG_{Li}\right)^2\frac{1}{GB_i\cdot tp_i^2}}{\left[\left(1+Z_oG_{Li}\right)\left(\frac{A_{ddi}}{GB_i}+\frac{1}{GB_i\cdot tp_i}\right)+\frac{Z_o}{z_{ozero}}\left(G_{Lf}-G_{Li}\right)+Z_o\left(C_{Lf}-C_{Li}\right)\right]^2} \tag{4.37}$$

that is always non-negative.

Let us consider now the derivatives of the tangent of the phase margin in the final space. If we consider the derivative with respect to the tangent of the phase margin in the original load:

$$\begin{aligned} \frac{\delta tp_f}{\delta tp_i} = {} & \frac{\left[\left(1+Z_oG_{Li}\right)\left(\frac{A_{ddi}}{GB_i}+\frac{1}{GB_i\cdot tp_i}\right)+\frac{Z_o}{z_{ozero}}\left(G_{Lf}-G_{Li}\right)+Z_o\left(C_{Lf}-C_{Li}\right)\right]}{A_{ddi}\left(1+Z_oG_{Li}\right)\left[\left(1+Z_oG_{Li}\right)\frac{A_{ddi}}{GB_i^2\cdot tp_i}+\frac{Z_o}{z_{ozero}}\left(C_{Lf}-C_{Li}\right)\right]^2}\cdot \\ & \cdot\left\{\frac{A_{ddi}}{GB_i^3\cdot tp_i^2}\left(1+Z_oG_{Li}\right)^2\left(A_{ddi}-\frac{1}{tp_i}\right)+\frac{Z_o}{z_{ozero}}\frac{A_{ddi}\left(1+Z_oG_{Li}\right)}{GB_i^2\cdot tp_i^2}\right. \\ & \left.\cdot\left(G_{Li}-G_{Lf}\right)+\frac{Z_o\left(1+Z_oG_{Li}\right)}{GB_i\cdot tp_i^2}\left(\frac{A_{ddi}}{GB_i}-\frac{2}{z_{ozero}}\right)\left(C_{Lf}-C_{Li}\right)\right\} \end{aligned} \tag{4.38}$$

If we consider that for all performance values of interest:

$$A_{ddi} - \frac{1}{tp_i} \geq 0 \quad \text{and} \quad \frac{A_{ddi}}{GB_i} - \frac{2}{z_{ozero}} \geq 0 \tag{4.39}$$

then, this derivative is guaranteed to be non-negative if:

$$\begin{aligned} G_{Lf} &\geq G_{Li} \\ C_{Lf} &\geq C_{Li} \end{aligned} \tag{4.40}$$

Therefore, by looking at the derivatives of the four objectives at the final space with respect to the phase margin at the initial objective space it can be checked that the conditions $G_{Lf} \geq G_{Li}$ and $C_{Lf} \geq C_{Li}$ guarantee that a Pareto front can be safely transformed, without any loss of information, by generating a front for a lower load capacitance and higher load resistance, and transforming the resulting front to the final load conditions.

These conditions tell us whether there will be information loss or not when transforming a PoF of amplifiers to a load that is different than that for which it was generated. In the case they are not fulfilled, the transformed PoF will not be valid and, therefore, a new PoF would need to be generated for the new loading conditions. In a bottom-up design methodology, the loading conditions imposed to a low-level PoF are variable, that is, each generated high-level individual will impose different loading conditions to the amplifiers of the lower-level PoF. Therefore, this lower-level PoF must be transformed to the loading conditions impose by that high-level individual in order to check the validity of the amplifiers for that design. This idea is illustrated in Fig.4.5. As it can be seen, a number of P design variables of the higher-level block define the loading conditions that will be seen by the lower-level block. Using these variables, the new loading conditions are estimated and the lower-level PoF can be transformed to those new conditions. In this case, if the transformation conditions are not fulfilled, a new PoF must be generated. This is unaffordable in terms of CPU time because the number of PoFs that would need to be generated is proportional to the population size and the number of generations for which the high-level PoF is generated. In order to mitigate this problem, it is necessary to work with a library of PoFs, where each one has been generated for a different load. By doing so, we can be sure that, for every possible load imposed by a high-level block, there will be at least one low-level PoF that fulfills the transformation conditions, avoiding the repetitive and time-consuming process of generating a new low-level PoF.

Another reason for working with a library of PoFs is related to an important effect that may take place when transforming a PoF to a different loading conditions. As it has been explained, in this transformation there is usually a loss

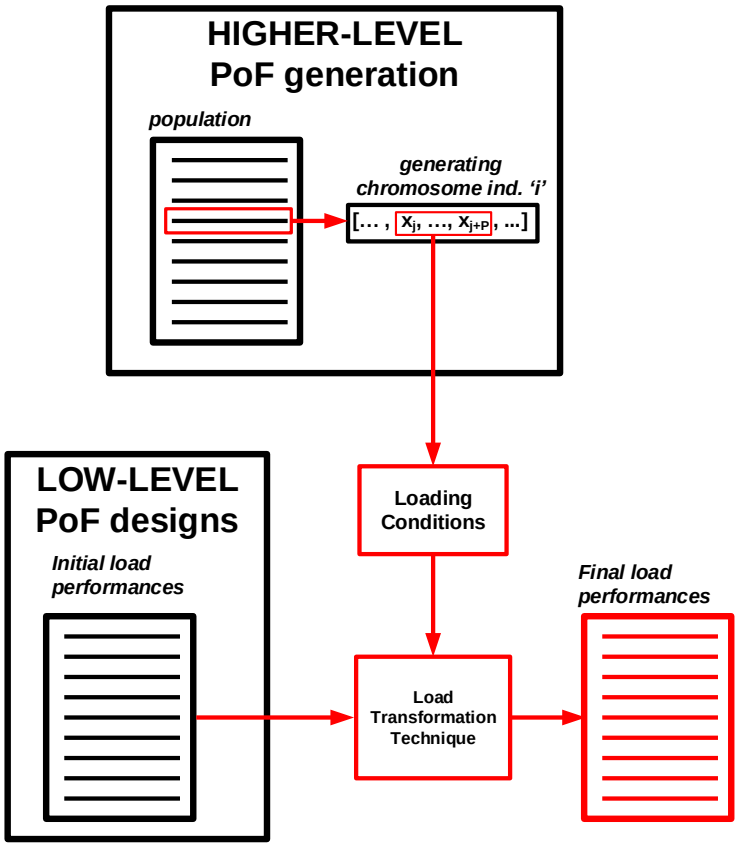


Figure 4.5: Use of the load transformation technique when the final loading conditions are variable.

in terms of diversity of solutions as not all transformed points will remain useful. Since each design point changes its performances when the load conditions change, this change may shift the specifications to useless values, e.g., the phase margin of some design points may become negative or the DC-Gain may decrease too much. Therefore, the density of points in the transformed Pareto front is usually lower than in the original front.

Quality of PoFs is usually associated to diversity (the range of performance objectives that is covered by the front and the uniform distribution of points in the front) and convergence (how close is the front to the ideal performance front). In terms of convergence, if a transformed front is compared to another performance front generated for the final loading conditions, some points will be dominated by the latter and some points of the latter will be dominated by those of the former. This is not strange as PoFs are an approximation to the ideal front (the evolutionary optimization algorithm generating the front stops after a finite number of generations). In fact, the same phenomenon can be observed if the fronts

of two different executions of the optimization algorithm (of stochastic nature) for exactly the same conditions are compared.

There is, thus, some degradation in terms of diversity, usually more important as the difference between the initial and final loading conditions becomes larger. This is quite logical as the transformation to new loading conditions implies a displacement of the points of the Pareto front in the performance space. Multi-objective optimization algorithms are usually designed to optimize the diversity of points in the Pareto front. As the transformation procedure is non-linear with respect to the performance objectives, it is obvious that diversity will change. To illustrate this, let us consider the Miller two-stage operational amplifier whose schematic is shown in Fig.4.6.

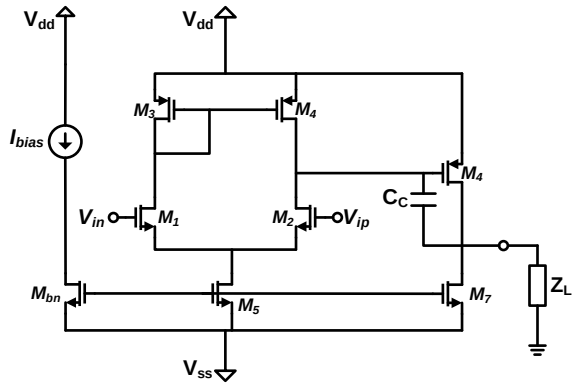


Figure 4.6: Miller two-stage operational amplifier.

Different projections of a PoF of this amplifier, generated for the design objectives DC-gain, fu, output impedance (Z_0) and phase-margin (PM), and for a capacitive load of 1 pF, are shown in Fig.4.7. If this PoF is transformed using the transformation technique presented in this Chapter to a new loading conditions of 2 pF and 50 kΩ, we obtain the PoF shown in Fig.4.8:

On the other hand, when a new PoF of the amplifier is generated by running the optimizer with the electrical simulator for these new loading conditions ($2pF$ and $50k\Omega$), we obtain the PoF shown in Fig.4.9. As it can be observed, the quality of the transformed PoF in terms of diversity is worse than that of the PoF that is generated directly for the final loading conditions. This is due to the reasons mentioned above: some designs of the original PoF are not valid in the final load space, either because they become dominated by other individuals or because they no longer fulfill the design constraints. By working with a library of PoFs, all fronts of the library can be transformed to the new load, each one contributing with different design points, so that the quality of the transformed PoFs is similar to that of the PoF generated

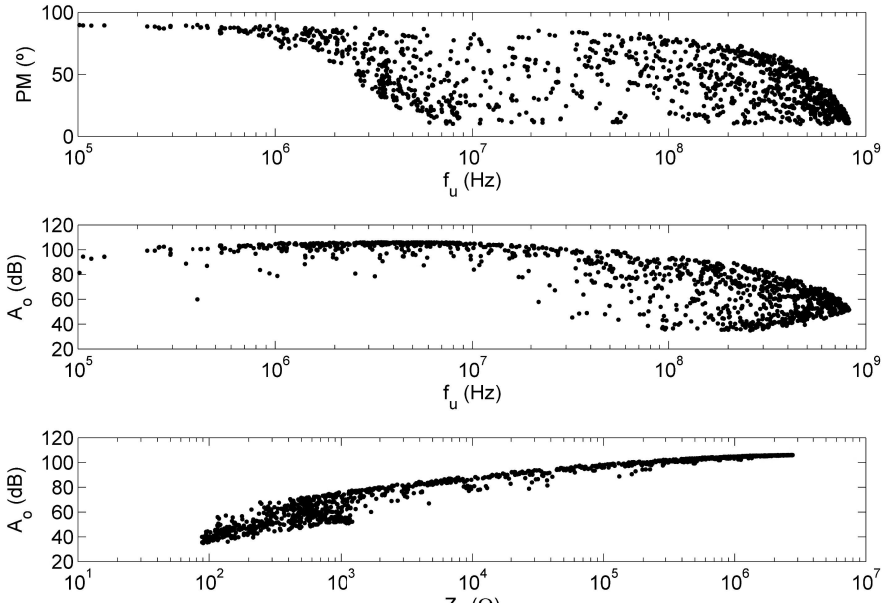


Figure 4.7: Projections of the PoF generated by the multi-objective optimization algorithm for a capacitive load of 1 pF.

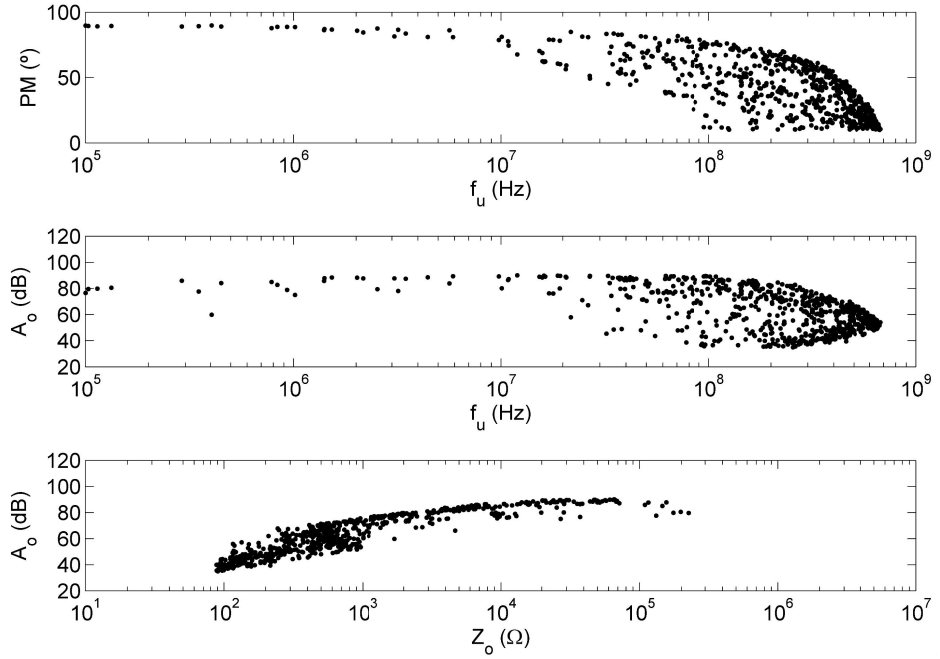


Figure 4.8: Projections of the PoF obtained by the transformation procedure for a load of 2 pF and 50 kΩ.

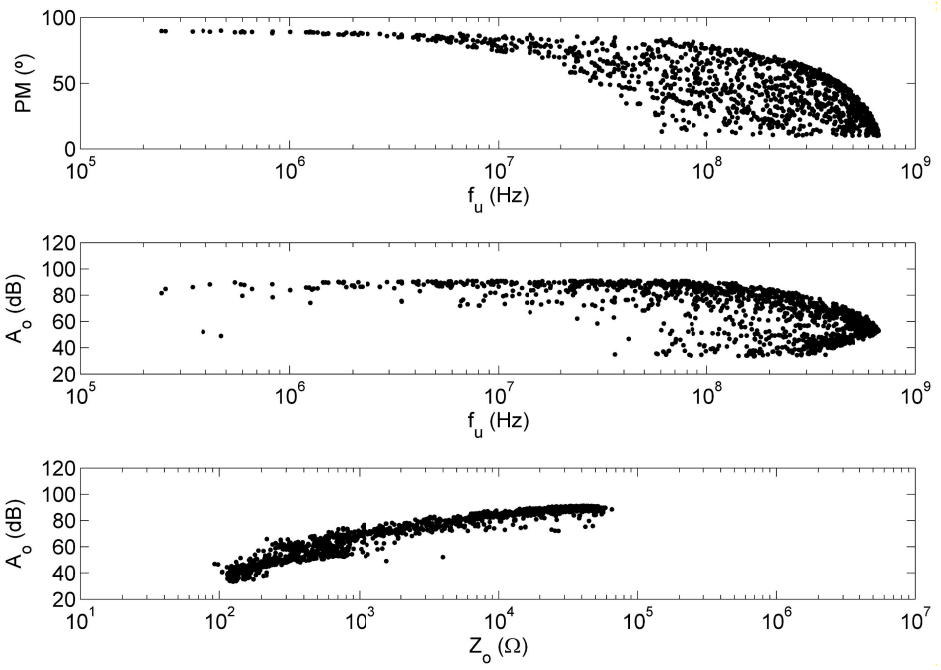


Figure 4.9: Projections of the PoF generated by the multi-objective optimization algorithm for a capacitive load of 2 pF and 50 kΩ

for the new loading conditions. This procedure will be illustrated later on in the application examples that are presented in the following chapters.

4.2 SORTING POFS FOR HIERARCHICAL COMPOSITION

The second issue that has been considered in this Thesis is related to how to perform the exploration of low-level PoFs when they are part of the design space of higher-level blocks. This idea is described in the following section. As it will be shown, this aspect has a critical impact in the convergence to the best trade-off regions during the generation of PoFs of high-level blocks.

Low-level PoFs are part of the design space of higher-level blocks and, as such, they must be explored during the generation of their PoFs. That is, just as during the generation of a PoF the optimizer must explore the ranges of the design variables, it also has to consider all possible combinations of the designs of lower-level PoFs. The simplest solution for this is to assign an integer value to each individual of a low-level PoF, and use this index as a design variable during the generation of the higher-level PoF. Let us denote these variables that represent individuals of low-level PoFs as ***indexing variables***. This is depicted in Fig.4.10. Unfortunately, in general the values of these indexes may not be correlated just as

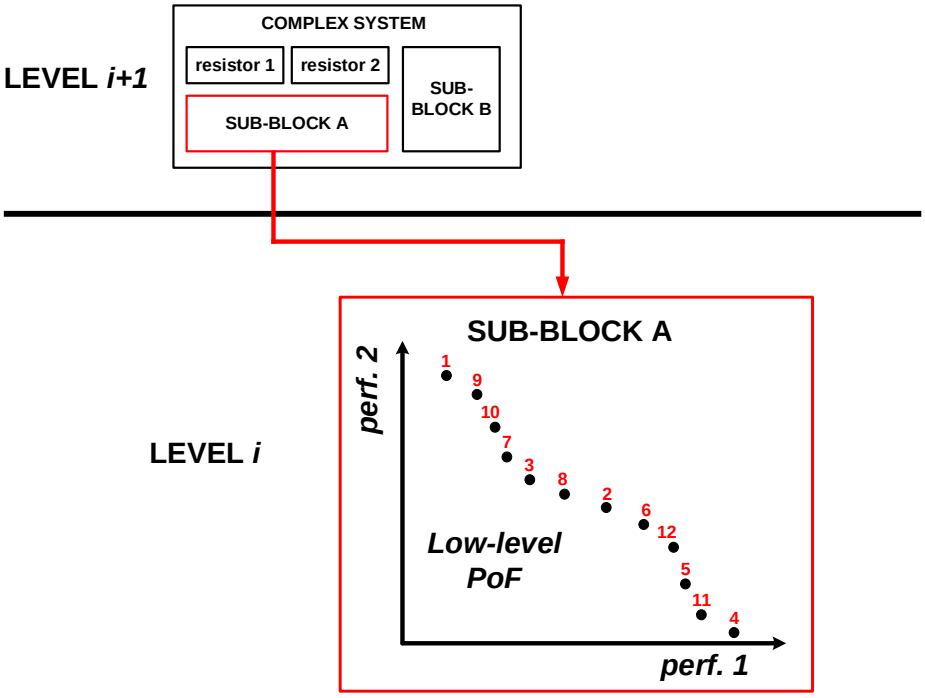


Figure 4.10: The points of PoFs of low-level blocks that are part of the search space must be indexed.

it happens in the example shown in the figure. That is, close values may represent individuals (or designs) with completely different performances. This may degrade the efficiency of the low-level PoF exploration. Mutation operators in EAs perform small changes on the design variables. For instance, for a resistance, a real value is used as a design variable, and that real value is directly the value of the resistance. During the generation of a PoF, the mutation operator changes slightly that real value to generate a slightly different resistance, as it is shown in Fig.4.11. On the other hand, that will not happen if the values of a design variable are not correlated. An example is also shown in Fig.4.11 where, as it can be seen, individuals of a low-level PoF with index values 1, 2 and 3 are in different regions of the PoF. As a result, a mutation around individual 1 may jump to a completely different region of the PoF instead of exploring the region around that individual. As a consequence, the mutation operation is transformed into a completely random variation.

It can be concluded that, in general, indexing variables can not be mutated directly. A simple sorting of the individuals of low-level PoFs will solve this problem only when the number of performances of the low-level PoF is two. In any other case, the mutation of such variables must be done indirectly. Two different sorting techniques have been proposed in this work, based on index mapping

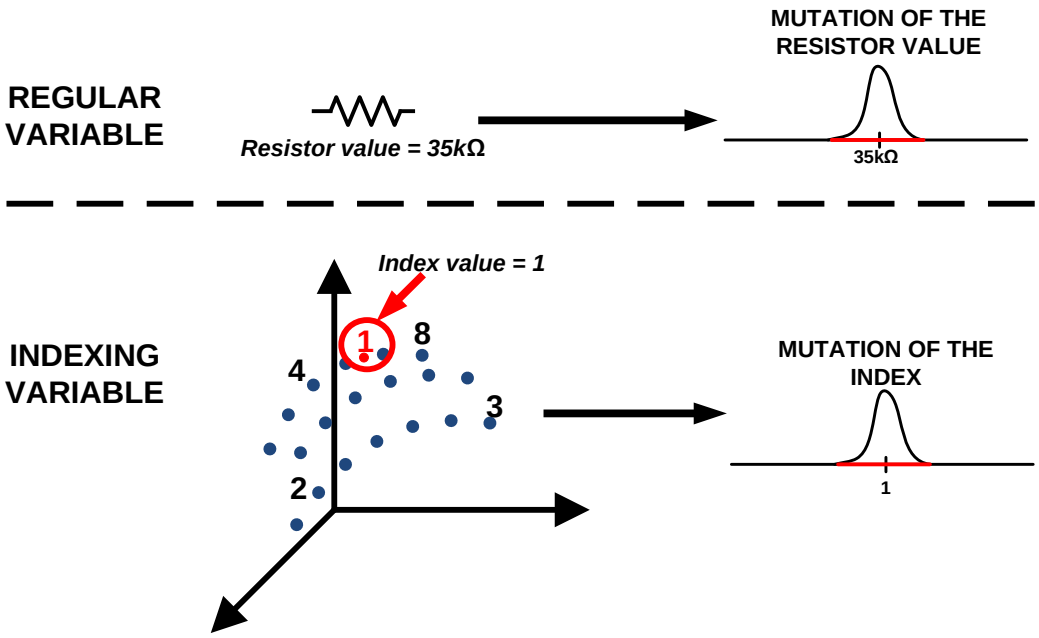


Figure 4.11: Mutation operation for regular and indexing design variables.

techniques and the use of real performance values. These techniques are compared to more traditional solutions based on sorting with respect to a reference point, showing the benefits of the new approaches. All techniques are described in the following lines, as well as the experiments that have been carried out to compare them.

4.2.1 *Method I: Sorting Around a Reference Individual*

In this approach, an indexing variable is used to represent each individual of a low-level PoF. Each time that the indexing variable is mutated, the distance in the design objective space of each individual of the front to the reference individual, which is that pointed by the current value of the indexing variable, is calculated. The distance metric that is used can be Euclidean or Manhattan, the latter measured as the distance between two points using a grid-based path, that is, using strictly horizontal and vertical paths on a grid.

After assigning the distance to each individual, whether Euclidean distance or Manhattan distance, a position is assigned to each individual according to the value of that distance. By doing so, the reference individual always has position 0. Thus, a mutation of the position will provide the position of the new individual. In other words, the indexing variable is mutated using the relative positioning of the individuals with respect to the reference individual as variable. An example is

shown in Fig.4.12, where the individuals around a reference individual are sorted using the Euclidean distance to that reference individual in the design objective space.

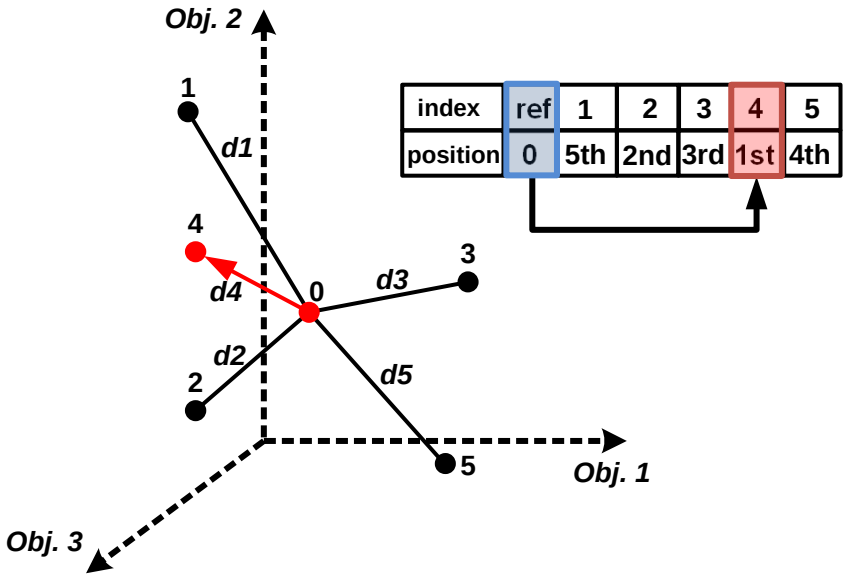


Figure 4.12: Sorting individuals around the reference individual and use of the position as variable.

To illustrate the difference between using the Euclidean or the Manhattan distance, let us consider the example shown in Fig.4.13, where three individuals are represented in the plane formed by two unitary performances. In the figure, the Manhattan distance between individuals A and B would be of 6, different to the euclidean distance, which is of $3\sqrt{2}$. On the other hand, the Euclidean distance between individuals A and C is of 5, which in this case is equal to the Manhattan distance. If A is the reference individual, the use of the Euclidean distance in the sorting procedure prioritizes individual B, because lower distances are more likely, while the use of the Manhattan distance prioritizes individual C, which only differs in performance 1 with respect the reference individual.

Using the method previously described requires a separate sorting for each individual of the low-level PoF. This sorting must be performed only once at the beginning of the generation of higher-level PoF if the loading conditions for the low-level block are fixed. However, in the case these conditions change during the optimization process, the sorting must be performed each time a mutation occurs because the performances of the individuals of the low-level PoF will be different and, thus, the sorting will be also different. This is a drawback of this approach,

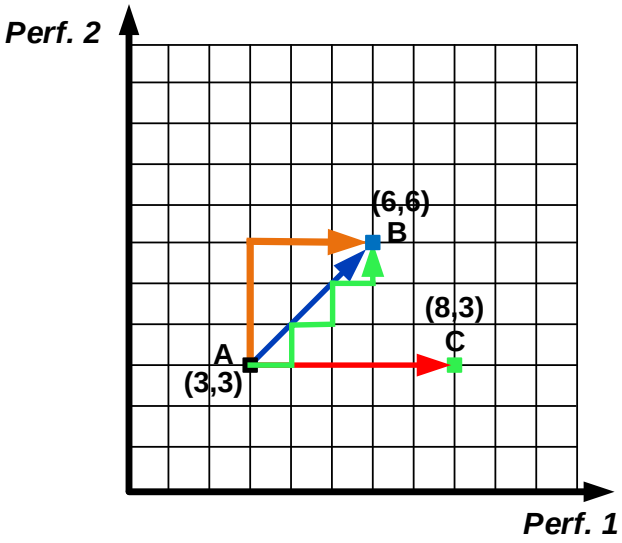


Figure 4.13: Difference between Euclidean and Manhattan distances. The blue line represents the Euclidean distance between individuals A and B. The orange and green dashed lines represent equivalent Manhattan distances between those same individuals. Red line represents both the Euclidean and the Manhattan distances.

since performing a sorting process at each mutation can increased significantly the CPU time required for the generation of higher-level PoFs.

4.2.2 *Proposed Approach I: Index-mapping*

This approach is based on the use of a set of coordinates to map $N-1$ design objectives of a N-Dimension low-level PoF. By doing so, each individual of a low-level PoF can be represented by a set of coordinates instead of with a single indexing variable. As a PoF generated for n design objectives is an hyper-surface of dimension $n-1$, a set of only $n-1$ coordinates is necessary to map the PoF. An example is shown in Fig.4.14, where a set of 2 coordinates is assigned to each individual of a 3D front. As it can be seen, individuals of the low-level PoF with similar performances will have similar coordinates. Therefore, these coordinates can be mutated as regular variables and only a unique sorting process is required at the beginning of the optimization process. However, as in the sorting process based on the use of the distance, the mapping process and the assignment of coordinates to the individuals of the PoF will be performed only once in the case the loading conditions imposed to the low-level block are fixed. When these conditions change

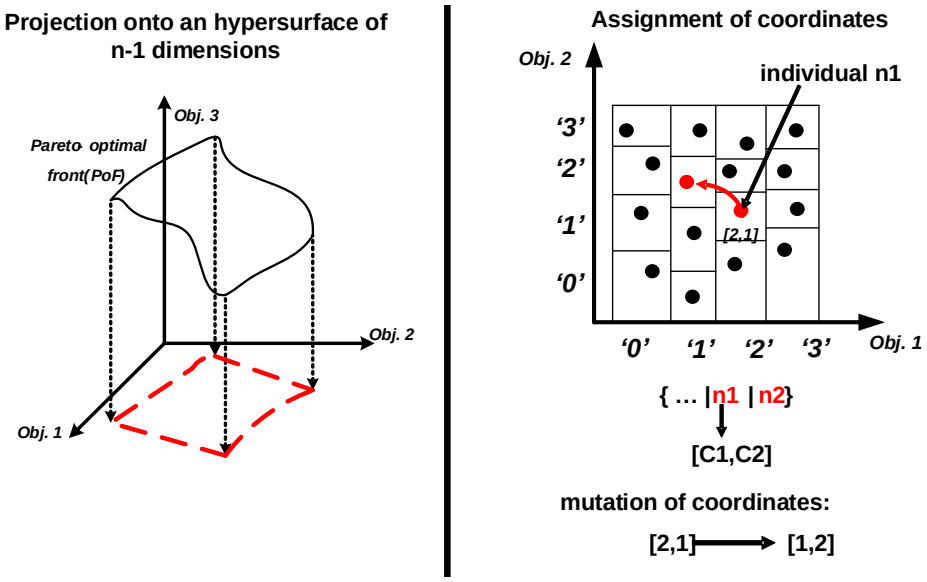


Figure 4.14: Index-mapping process for a low-level PoF.

during the optimization process, the mapping and assignment of coordinates must be performed each time a mutation occurs.

On the other hand, with this approach each performance of the low-level PoF is treated as an independent coordinate or design variable. In EAs, where the probability of a mutation is small, having several coordinates that act as design variables increases the probability of changing the individual, since only the change of one of the coordinates is enough to jump to another individual of the low-level PoF.

4.2.3 *Proposed Approach II: Use of Real Values*

In this approach, the real values of the performances of the low-level PoFs are used directly as design variables in the upper level. The ranges of these variables are those covered by the low-level PoF. An example is shown in Fig.4.15, where a 3D PoF is projected onto the plane of two design objectives. As in the Index-mapping method, here a PoF generated for n design objectives can be explored using only $n-1$ design objectives as design variables. As it can be seen, the maximum and minimum values of design variables 1 and 2 are defined as the maximum and minimum values reached by the PoF in each design objective. This means that the search space will be that delimited by the dashed lines. When the algorithm creates new individuals, giving random values of these variables within the ranges defined before, it is quite probable that the values do not correspond exactly to

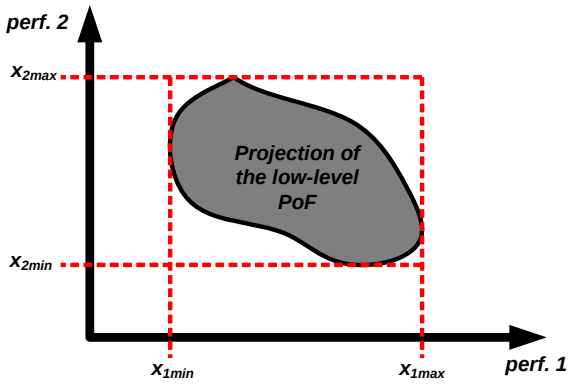


Figure 4.15: Projection of a 3D PoF onto the plane formed by two design objectives.

any individual of the low-level PoF and, thus, these values are not valid. Instead, the algorithm must search the nearest individual to the result point and update the values of the variables with the real values of the individual, as depicted in Fig.4.16. This process must be done each time a mutation or crossover occurs. As in the Index-mapping approach, here each low-level performance is treated as an independent variable and thus the advantages of the previous approach are preserved.

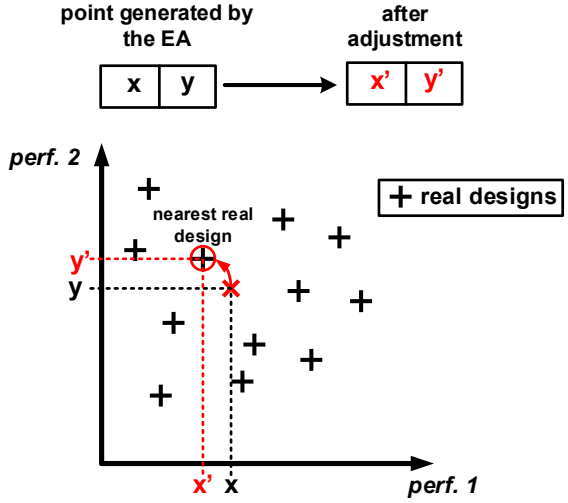


Figure 4.16: Assignment of real values.

It is important to note that, as the ranges of the design variables cannot change during the optimization process, their ranges are defined in a fixed load space. On the other hand, the search of the nearest individual must be performed among

those individuals that are non-dominated in the final loading conditions, that is, among those individuals that are not dominated by any other individual and which are valid in terms of the design constraints.

This approach presents a drawback that must be taken into account. As it can be seen in Fig.4.15, the ranges of the design variables used to explore the low-level PoFs do not have into account the shape of the PoF, only the maximum and minimum values that are achieved. As a consequence, it may occur that a lot of points of the hyperspace defined by the ranges of the design variables are empty of individuals. This affects adversely into the exploration of the low-level PoF by the evolutionary algorithm, as the solutions of the front that are in the frontier will be favored each time a point in an empty region is considered.

4.2.4 *Comparison of the different Approaches*

In order to compare the approaches described in this section for the exploration of low-level PoFs, the generation of the PoF of an active filter by hierarchically composing PoFs of operational amplifiers will be used as demonstration vehicle. The schematic of the filter is shown in Fig.4.17. As it can be seen, it is a current-driven fully-differential RC-active Tow-Thomas second-order low-pass filter. In this case, besides the passive network of resistors and capacitors, the operational amplifiers will be also part of the design space and they will be selected from PoFs of amplifiers that have been generated previously.

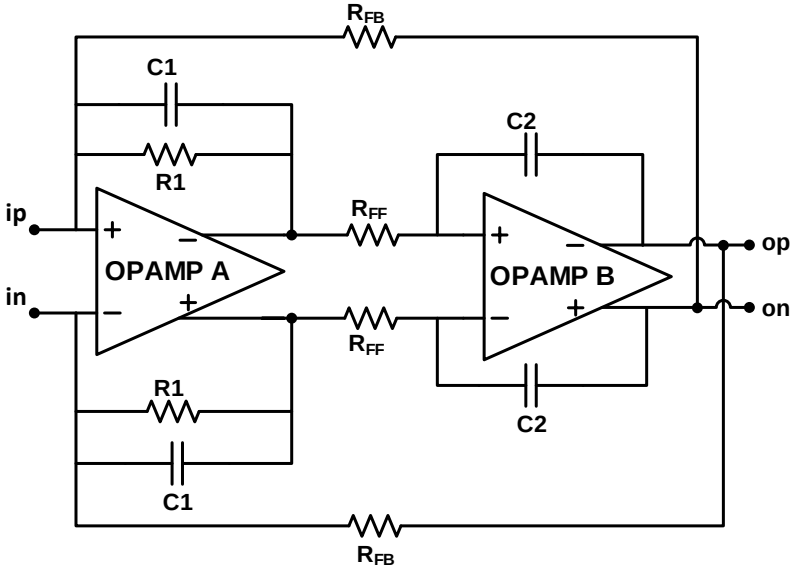


Figure 4.17: Continuous-time low-pass active filter.

The comparison of the different approaches will be done by measuring the convergence ratio of the solutions provided by each approach to the **true PoF**. The true-PoF, as defined previously in chapter 3, is a continuous region in the performance space, limited in number only by the grid of the design variables, while the solutions provided by EAs are only small finite sets that approximate that region. Thus, in order to be able to measure that convergence to the true-PoF, the passive network of the filter will be fixed. By doing so, the only design space is that formed by the low-level PoFs of amplifiers and the true-PoF can be obtained by exhaustive search over all the possible combinations of amplifiers.

The values of the passive devices are those shown in Table 4.1. These values have been chosen to guarantee the correct operation of the filter using ideal amplifiers.

Table 4.1: Elements of the Passive Network.

Element	**Value**	
R_1	30 kΩ	
R_{ff}	10 kΩ	
R_{fb}	2.85 kΩ	
C_1, C_2	23 pF	
Load OA. 1	R_{LOAD}	27.8 kΩ
	C_{LOAD}	3.8 pF
Load OA. 2	R_{LOAD}	23.3 kΩ
	C_{LOAD}	4.7 pF

The passive devices define an equivalent load for each amplifier of the filter, which are also shown in the table. Two PoFs of amplifiers will be generated, one for each one of these equivalent loading conditions, using the methodology described in chapter 3. The same folded-cascode with Miller compensation topology will be used and the design objectives will be, as in chapter 3, the DC-Gain, the unity-gain frequency, the power consumption and the area. More details about the generation of these PoFs are in section 3.1.2 of chapter 3.

The filter will be designed to provide specific DC-Gain and bandwidth while optimizing the area and the power consumption. These specifications are shown in Table 4.2. The true PoF is obtained after measuring 10^6 possible combinations of amplifiers (the PoFs of amplifiers are formed of 10^3 individuals each one). It is shown in Fig.4.18. As it can be seen, it is composed of only 16 solutions.

As it has been discussed above, in order to compare the different approaches for the exploration of low-level PoFs, the PoF of the filter will be generated using each of them. By doing so, and as we have obtained the true-PoF of the

Table 4.2: Design Objectives and Specifications for the generation of the true-PoF of the filter.

	Name	Treatment
Design Objectives	area	minimize
	power	minimize
Specs.	DC-Gain	> 50 dB
	fcut	< 6.0 MHz

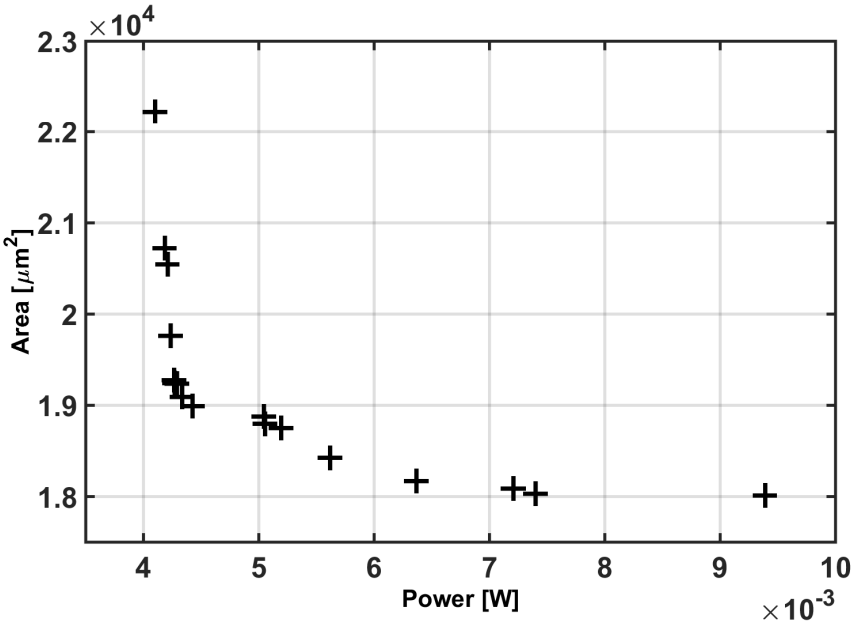


Figure 4.18: True Pareto-optimal front of the filter when the passive devices are fixed.

filter, the convergence to that true-PoF for each approach can be measured. The design variables used to explore the low-level PoFs of amplifiers will be different depending on the approach. For the approaches based on the use of the Euclidean and the Manhattan distances, an indexing variable will be used to represent each amplifier of the filter. In the case of the Index-mapping approach, 3 coordinates will be used to represent each amplifier of the filter. Note that the PoFs of amplifiers have been generated for 4 design objectives. Therefore, the individuals of the PoFs can be characterized with 3 coordinates. For the same reason, for the approach that uses real values of the lower-level performances as variable, 3 real variables will be used for each amplifier of the filter. Additionally, another approach where each amplifier of the filter is represented by one indexing variable and this variable is

mutated directly, without any of the approaches explained here, is also considered. We denote this approach as *NO SORTING*. This will serve to show the necessity of using methods like the approaches described here to efficiently explore low-level PoFs, that is, that indexing variables can not be mutated as regular variables.

In order to compare the approaches statistically, 100 runs of each approach are carried out. Each run uses a different seed, which is a parameter used by the EA for several steps of the optimization, like the generation of the initial population or the mutation operation, which use randomness. The use of this parameter makes each run different, beginning with different initial populations and leading to different final results (i.e., different individuals). In each run, the PoF of the filter will be generated for a population size of 100 individuals and using 50 generations of the evolutionary process. The convergence ratio of each approach to the true-PoF will be measured using the mean values of the number of solutions of the true-PoF that are found at each generation. That is, for each generation of each run of each approach, the number of solutions of the true-PoF that have been found is measured. Afterwards, the mean values at each generation can be calculated. The results obtained from this calculation are shown in Fig.4.19.

As it can be seen, the Real Values approach finds the largest number of solutions of the true PoF, although the Index-mapping method finds a similar number of solutions but much faster than the rest of approaches. At generation 20, the Index-mapping approach has found more than twice the number of solutions of the true-PoF found by the rest of approaches. This demonstrates that the Index-mapping method allows a faster convergence to better regions of the design objective space. This is a very important aspect of the optimization process. While in this experiment the time per generation was similar for all approaches and it took around 20 seconds, in real design problems, however, that time may be much higher. For instance, in those design problems where electromagnetic and layout simulations are required, such as design optimization of inductors [62] or generation of layout-aware PoFs of analog circuits [63], the CPU time required for each generation of the evolutionary process may vary from several minutes to even hours. It is clear that, in those scenarios, the number of generations required to converge to the PoF is a critical factor that must be taken into account.

The two-set coverage metric (CS) [64] can be used to compare the methods that have been studied here. This metric is defined as:

$$C(B,A) = \frac{|\{a \in A | \exists b \in B, b \prec a\}|}{|A|} \tag{4.41}$$

where $b \prec = a$ means that individual a is dominated by individual b. The CS metric is thus a measure of the number of individuals from front A that are dominated by individuals from front B. The mean values of the CS between the different

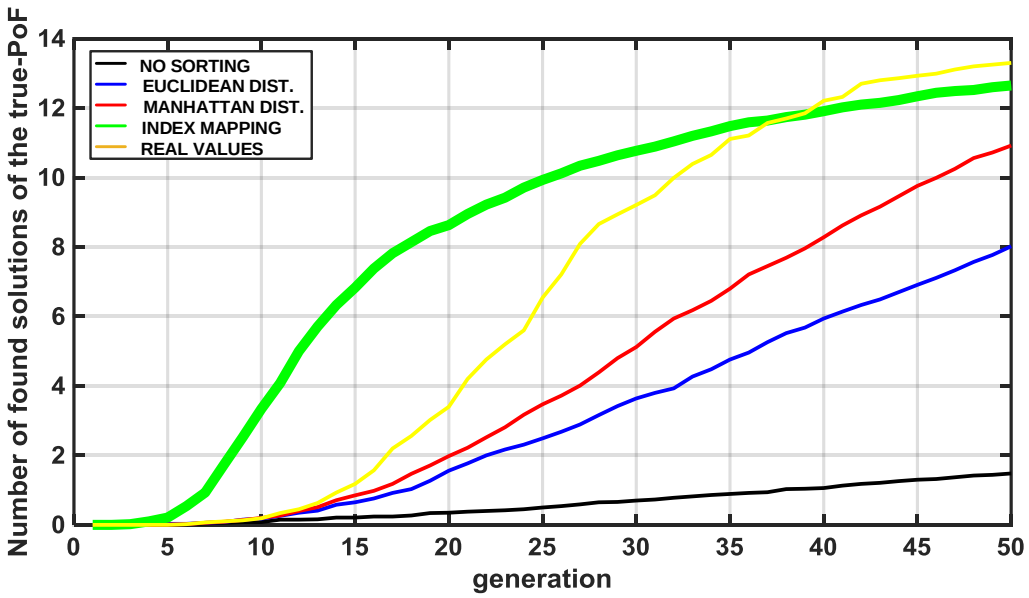


Figure 4.19: Mean values of the number of solutions of the true PoF that are found by each approach at each generation.

approaches at different generations are shown from Table 4.3 to Table 4.5. In the tables, each cell (i, j) shows the result of the CS metric as $C(j, i)$. That is, it shows the coverage of the fronts generated by the approach in column j over the fronts generated by the approach in row i. As it can be seen, at generation 10 the results obtained with the Index-mapping approach dominate the rest of approaches by more than 80% according to the CS metric. In the case of the *Real Values* approach this dominance is of around 64%. At generation 25, the *Real Values* approach has reached the *Index-Mapping* approach in terms of dominance and both still dominate the rest of approaches. While the dominance of the *Index-Mapping* and the *Real Values* approaches over the *Manhattan Distance* approach is around 50%, the dominance of the latter over the first one is only around 15%. In the successive generations, the *Index-Mapping* and the *Real Values* approaches get the best results in terms of dominance over the rest of the approaches. At generation 50, the *Real Values* obtains better results than the *Index-Mapping* approach. However, the latter is preferable. First, in the Index-Mapping method, every possible combination of coordinates corresponds univocally to an individual of the low-level PoF. Therefore, there are no empty regions in the hyperspace defined by the ranges of the indexing variables, as it happens with the *Real Values* approach. Second, the *Index-Mapping* has the fastest convergence to better regions of the objective performance space at early stages of the optimization process. It has also been demonstrated that, in terms of dominance, the results obtained with this approach at the final generations

of the evolutionary process are similar to those obtained by the rest of approaches. This means that this approach is able to obtain better results in less generations of the evolutionary process, which, as it has been explained, is a critical factor that must be taken into account. Therefore, the Index-mapping approach will be used in the experiments presented in the next chapters of this Thesis.

Table 4.3: Mean values of the coverage metric at generation 10.

	NO SORTING	EUCLIDEAN DIST.	MANHATTAN DIST.	INDEX MAPPING	REAL VALUES
NO SORTING		0.5003	0.5493	0.8817	0.5303
EUCLIDEAN DIST.	0.3680		0.5317	0.8410	0.4993
MANHATTAN DIST.	0.2937	0.4097		0.8230	0.4170
INDEX MAPPING	0.0607	0.0763	0.0897		0.1415
REAL VALUES	0.2473	0.3383	0.3623	0.6418	

Table 4.4: Mean values of the coverage metric at generation 25.

	NO SORTING	EUCLIDEAN DIST.	MANHATTAN DIST.	INDEX MAPPING	REAL VALUES
NO SORTING		0.6273	0.7493	0.8313	0.8423
EUCLIDEAN DIST.	0.1493		0.4537	0.6077	0.6310
MANHATTAN DIST.	0.0947	0.2533		0.4983	0.5203
INDEX MAPPING	0.0370	0.0830	0.1097		0.1662
REAL VALUES	0.0340	0.1080	0.1560	0.2665	

Table 4.5: Mean values of the coverage metric at generation 50.

	NO SORTING	EUCLIDEAN DIST.	MANHATTAN DIST.	INDEX MAPPING	REAL VALUES
NO SORTING		0.6713	0.7323	0.7243	0.7863
EUCLIDEAN DIST.	0.0627		0.3497	0.3393	0.3767
MANHATTAN DIST.	0.0397	0.1460		0.1897	0.2030
INDEX MAPPING	0.0447	0.0933	0.1057		0.1241
REAL VALUES	0.0197	0.0687	0.1003	0.0826	

4.3 SUMMARY

In this Chapter, new solutions to two important implementation issues of the hierarchical composition of PoFs have been developed. These are, first, the dependency of some performances of analog circuits with their surrounding circuitry and, second, the integration and exploration, during the generation of the PoFs of higher-level blocks, of previously generated fronts of lower-level blocks. In the following chapter, the methodology presented in this Thesis is applied in the design of an important analog system: an active, reconfigurable low-pass filter. All the aspects of the methodology described in this Thesis are used in the design

process: from the generation of the PoFs and mm-PoFs of the most basic blocks, to the hierarchical composition of those fronts from the Bottom-level up to the Top-level.

5 DESIGN EXAMPLE I: CONTINUOUS-TIME LOW-PASS FILTER

In this chapter, the generation of the Pareto-optimal front of a continuous-time, low-pass filter will be used as demonstrator vehicle of the design methodology proposed in this Thesis. The filter, whose schematic is shown in Fig.5.1, is the same that was used in section 4.2.4. First, a single-mode PoF of the filter performances will be generated by hierarchically composing the PoFs of the amplifiers. The results obtained following this methodology will be compared with traditional methodologies, by selecting a set of designs of the generated filter PoF and completing their design with a traditional top-down design flow. Afterwards, a multi-mode PoF of the filter will be generated using mm-PoFs of amplifiers. In this experiment, the area and the power consumption of two operation modes will be minimized while fulfilling the specifications for two different standards. In both experiments, the methods presented in chapter 4 are used: the load transformation technique for operational amplifiers and the Index-mapping technique to explore the low-level fronts of amplifiers.

5.1 FILTER OPERATION

The filter will be optimized to be used in a quadrature transmit interface. Essentially, such systems provide the interface between complex digital signals coming from the baseband digital processors and complex analog signals in quadrature phase (channels I and Q) for the RF transceiver. The IQ Digital-to-Analog (IQ DA) transmit interface system presented in [65] and whose functional block diagram is shown in Fig.5.2 will be considered as the target system of the filter designed in this chapter. This system provides two fully-differential channels in quadrature phase (90° phase shift) between the input digital ports and the output analog ports. Each channel is formed by a digital processing unit for signal shaping and interpolation (SINC), a Digital-to-Analog Converter (DAC) employing current-steering circuit techniques, the continuous-time second-order low-pass filter (CT-LP Filter), where this work is focused, and a first-order programmable-gain amplifier (PGA). An additional calibration unit is employed to adjust the unavoidable offsets and mismatches between both channels. A control unit is also used in order to control the functionality and calibration of the complete system.

The system operates as follows. The 16-bit input digital data (*bi* and *bq*) is oversampled by the interpolating filter to obtain a good spectral purity, thus

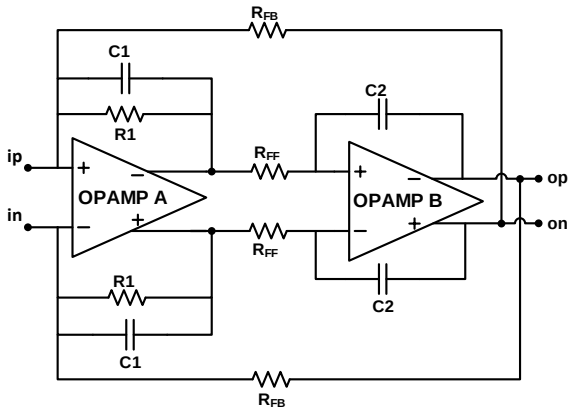


Figure 5.1: Continuous-time low-pass active filter.

relaxing the required resolution of the DAC. Next, the results are applied to the DAC, which has a fully-differential current-steering implementation and employs a segmented structure leading to a good linearity as well as to an optimum area and power dissipation. The purpose of the CT-LP filter is to attenuate the image components of the baseband spectrum at multiples of the clock frequency, to smooth the output signals generated by the preceding segmented current-steering DAC, as well as to provide current-to-voltage conversion. The purpose of the PGA, on the other hand, is to provide a digitally-controlled DC amplification of the differential output signal delivered by the CT-LP filter, to enforce the image rejection function of the CT-LP filter, and to support the buffering of its output differential signal to the external load of the chip, in order to directly drive commercially available RF modulators with no need of external components.

The IQ DA interface features programming capabilities by which different wireless standards can be supported and several operation modes can be used. This is done by circuit reconfiguration, which is controlled by digital signals (*sinc[1:0]*, *std[2:0]*, *outlev[2:0]*, enmint, econm, ontra and cal in Fig.5.2). This reconfigurability is accomplished by the DAC block, the PGA and the filter. In particular, reconfigurability in the filter is carried out by specifying different settings for its passive elements, which is controlled by the digital signal *std[1]*. Further analysis of the filter behavior is detailed in the following lines.

The transfer function of the filter is shown in Eq.5.1. It is obtained from basic circuit theory and assuming ideal opamps with infinite gain and bandwidth.

$$F(s) = \frac{V_o}{I_{in}}(s) = \frac{G_{FF}}{G_{FB}G_{FF} + G_1C_2s + C_1C_2s^2} \tag{5.1}$$

The following parameters can be extracted from this equation:

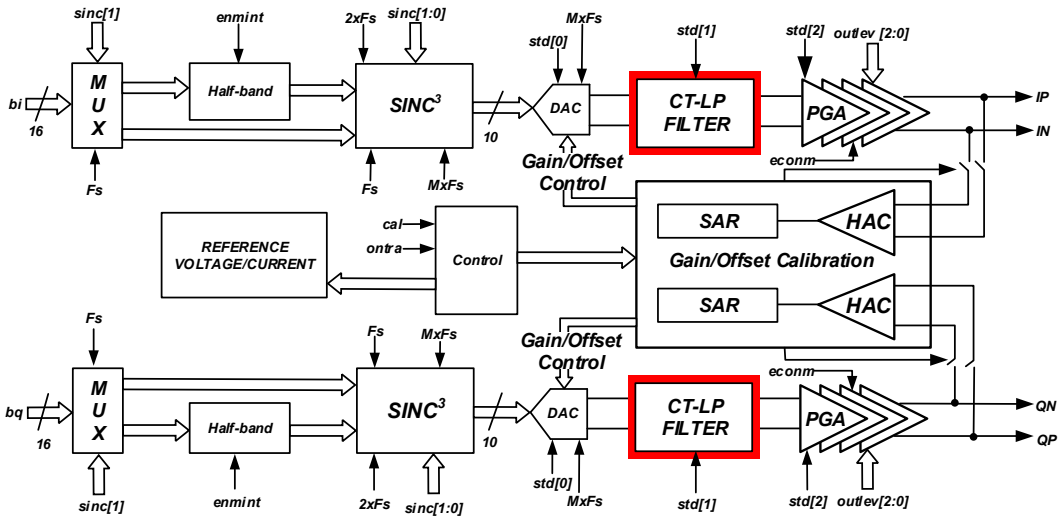


Figure 5.2: Diagram of the IQ DA transmit interface.

$$K = \frac{1}{G_{FB}} \qquad Q = \frac{1}{G_1}\sqrt{\frac{C_1 G_{FB} G_{FF}}{C_2}} \qquad \omega_n = \sqrt{\frac{G_{FB} G_{FF}}{C_1 C_2}} \tag{5.2}$$

where K is the DC-Gain of the filter and is defined by the overall feedback resistance R_{FB}, Q is the quality factor and ω_n its natural frequency. Assuming that the full-scale output current of the preceding DA converter takes a fixed value I_{FS}, the value of R_{FB} must guarantee a given full-scale output voltage V_{FS} according to:

$$R_{FB} = \frac{V_{FS}}{I_{FS}} \tag{5.3}$$

Other constraints among the passive elements can be derived. The quality factor is fixed to $Q = 1/\sqrt{2}$. This ensures a maximally-flat transfer of the baseband signal to the filter output. The natural frequency of the filter is defined by setting the cut-off frequency of the filter, $f_{p,CTF}$, in accordance to the minimum image rejection imposed by the standard:

$$\omega_n = 2\pi f_{p,CTF} \tag{5.4}$$

Additionally, imposing $C_1 = C_2$ is a convenient choice to improve matching. Using only two design variables, $rr1$ (the value of resistor R_1) and fn (the natural frequency of the filter), all passive devices are defined by these constraints.

5.2 GENERATION OF THE SINGLE-MODE PARETO-OPTIMAL FRONT OF THE CT-LP FILTER

The PoF of the filter will be generated by hierarchical composition of a set of PoFs of amplifiers that will be generated for different loading conditions. Additionally to the indexing variables that will be used to explore the low-level PoFs of amplifiers, other regular design variables will be used to define the values of the elements of the passive network of the filter. As explained in section 5.1, these variables are the value of resistor R_1 ($rr1$) and the natural frequency of the filter (fn). The rest of components are defined from these values, as shown in Table 5.1. Additionally, the width of resistors R_1, R_{FF} and R_{FB} are also treated as design variables. The ranges of these variables have been chosen taking into accounts the technology that is used as well as design issues for the proper operation of the filter.

Table 5.1: Design Variables of the Filter.

	Name	**Min. value**	**Max. value**
Independent variables	$rr1$	$20 \cdot 10^3\ \Omega$	$200 \cdot 10^3\ \Omega$
	fn	$70 \cdot 10^4$ Hz	$120 \cdot 10^4$ Hz
	w_{R_1}	0.75 μm	1.25μm
	$w_{R_{FF}}$	0.75 μm	1.25μm
	$w_{R_{FB}}$	0.75 μm	1.25μm
	Name	**Relation**	
Dependent variables	R_{FF}	$R_{FF} = \frac{2rr1^2}{R_{FB}}$	
	C	$C = \sqrt{\frac{1}{4\pi f_n^2 R_{FB} R_{FF}}}$	

The design objectives and constraints are detailed in Table 5.2. The constraints, depicted in Fig.5.3, are the requirements for the GSM standard. *Att.1* to *Att.3* are measurements of the attenuation at multiples of the sampling frequency for GSM (1083.3kHz). Parameters *dimar 1* and *dimar 2* are differences of these attenuations (as defined in Fig.5.3) and are used to ensure that the attenuation decreases with the frequency.

In this experiment, the components of the passive network of the filter are handled as design variables. Therefore, the loads seen by the amplifiers in the filter will take different values during the optimization process. As explained at the end of section 4.1, it is useful to work with a library of PoFs of basic building blocks generated for different loading conditions to ensure enough diversity of solutions when transforming the low-level PoFs to the different load values that

Table 5.2: Design Objectives and Constraints for the Optimization of the Filter.

	Name	Treatment
Design Objectives	area	minimize
	power	minimize
Constraints	Att.1	> 30 dB
	Att.2	> 30 dB
	Att.3	> 30 dB
	dimar 1	< 1
	dimar 2	< 1
	DC-Gain	> 50 dB
	fcut	< 6.0 MHz

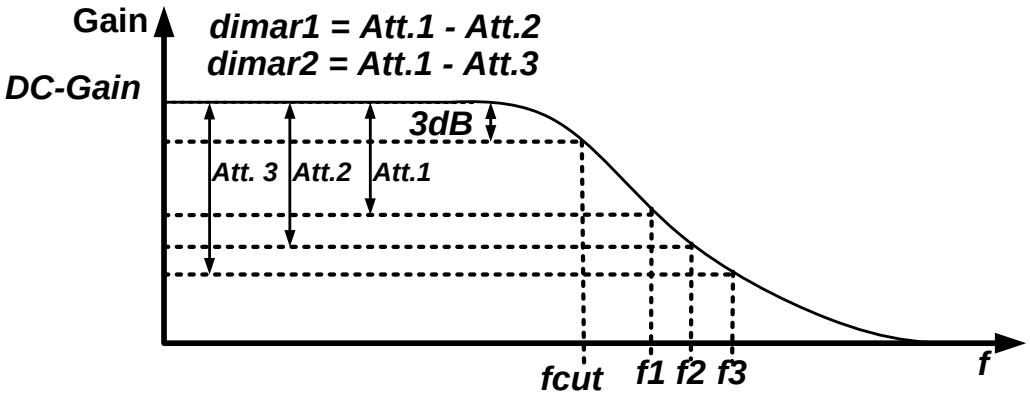


Figure 5.3: Constraints of the filter for the GSM standard.

are possible when generating the PoFs of higher-level blocks. Therefore, and as illustrative example of how this library could be initially generated, a study of the possible load values seen by the amplifier in the filter case will be performed and a set of PoFs of amplifiers will be generated for different loading conditions according to the results of that study.

Fronts of Amplifiers for different loads

In order to determine the ranges of the loads imposed by the passive network of the filter during the optimization process, a sweep analysis of the design variables $rr1$ and fn, which define all the components of the passive network, is done. Ideal models of the amplifier are used for this analysis. Although the results are not very

accurate, they can be used as a good estimation of the ranges of the loads that we are looking for. These values are shown in Fig.5.4. As it can be seen, the resistive load seen by OPAMP B is $3.57 \cdot 10^3\ \Omega$, which is the parallel of R_{FB} and the load resistance of the filter of value $20 \cdot 10^3\ \Omega$. In order to cover these ranges, 8 different opamps fronts will be generated for the loading conditions shown in Table 5.3. The first 4 fronts will be used for OPAMP A of the filter and the last 4, which are generated for a resistive load of $3.57 \cdot 10^3\ \Omega$, for OPAMP B. Each PoF of amplifiers will be generated for a population size of 300 individuals and using HSPICE® as circuit evaluator. The design objectives and constraints will be the same used in section 3.1.2.

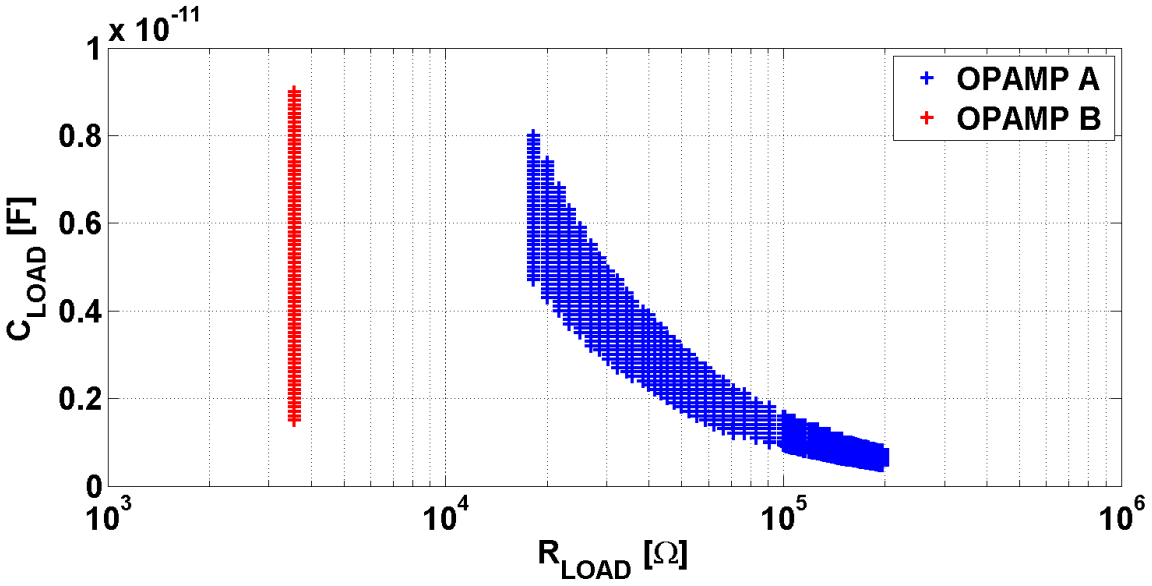


Figure 5.4: Estimation of the ranges of the loads seen by the opamps in the filter.

Table 5.3: Loading conditions for the generation of the PoFs of amplifiers.

Amplifier PoF	R_{LOAD}	C_{LOAD}
1	$20 \cdot 10^3\ \Omega$	6.0 pF
2	$80 \cdot 10^3\ \Omega$	3.0 pF
3	$140 \cdot 10^3\ \Omega$	2.0 pF
4	$200 \cdot 10^3\ \Omega$	1.0 pF
5-8	$3.57 \cdot 10^3\ \Omega$	$[1.0 - 3.0 - 5.0 - 8.0]$ pF

Performance space exploration of low-level PoFs of amplifiers

As already explained, the design variables that will be considered for the generation of the PoF of the filter are, additionally to the elements of the passive network, a set of indexing variables that will be used to represent designs of the lower-level PoFs of amplifiers. The variables that define the passive network, rr_1, fn, w_{R_1}, $w_{R_{FF}}$ and $w_{R_{FB}}$ are real variables and, as such, they can be mutated as regular variables. On the other hand, for the exploration of the fronts of amplifiers, the Index-mapping method described in section 4.2.2, will be used. For this, as the PoFs of amplifiers have been generated for 4 design objectives (DC-Gain, unity-gain frequency (fu), power consumption and area), 3 coordinates are used to define each opamp of the filter. That is, 6 variables in total, 3 for OPAMP A and 3 for OPAMP B. Therefore, as depicted in Fig.5.5, each individual of the filter population will be characterized by 11 design variables.

Figure 5.5: Design variables that characterize each filter.

The exploration of the low-level PoFs of amplifiers is carried out using the two sets of indexing variables. At the beginning of the optimization process, all PoFs of amplifiers are transformed once to a no-load space, that is, $C_L = 0$ and $G_L = 0$. By doing so, all points of all fronts are in the same space, and a set of coordinates can be assigned to each one of them. Variables $C1.1$ to $C1.3$ are assigned for OPAMP A, while variables $C2.1$ to $C2.3$ are assigned for OPAMP B. These coordinates will be always relative to the no-load space. The mutation of each set of indexing variables is done as explained in the following lines and is depicted in Fig.5.6:

1. First, all the design variables (including the set of indexing variables) are mutated. Afterwards, the loading conditions seen by the corresponding amplifier (OPAMP A or OPAMP B) are estimated from the new values of R_1 and f_n. The PoFs of amplifiers that fulfill the transformation conditions obtained in Chapter 4 ($G_{Lf} \geq G_{Li}$ and $C_{Lf} \leq C_{Li}$) are transformed from the no-load space to those new conditions and the individuals that are dominated or do not fulfill design constraints in the final space are identified.

2. If the selected amplifier, whose coordinates are defined by the new values of the set of indexing variables, is valid in the final space (i.e., is non-dominated and fulfills the design constraints), the mutation process stops here. Otherwise, it continues with steps 3 and 4.

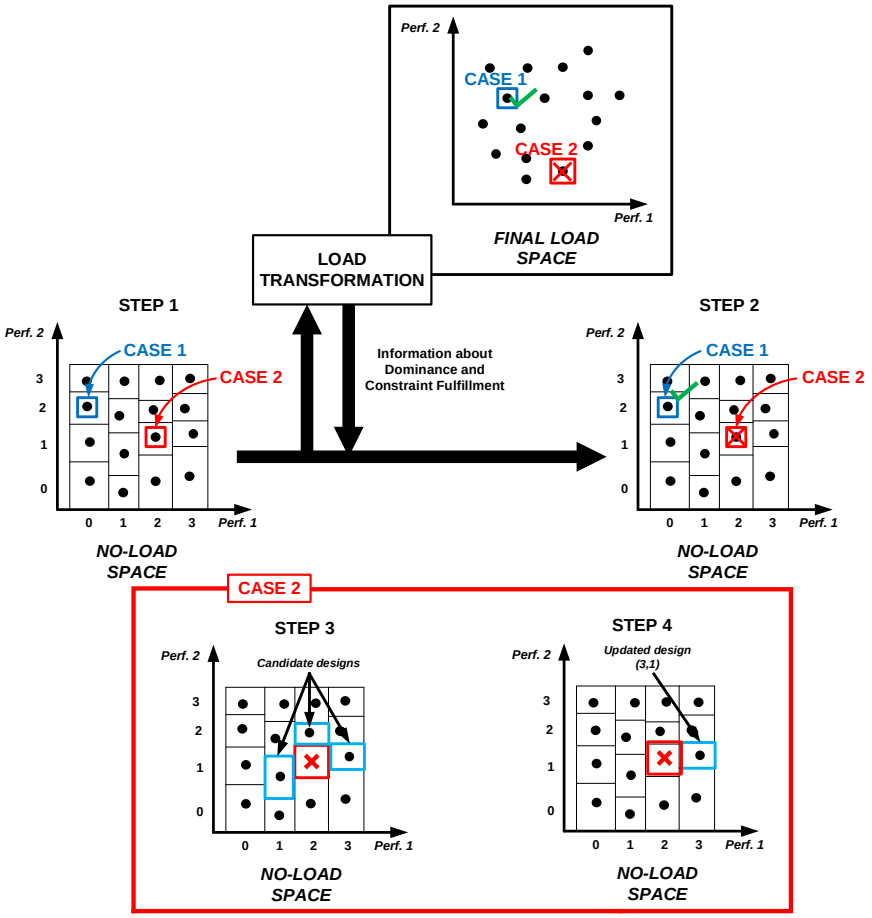


Figure 5.6: Selection of amplifiers from low-level PoFs by mutation of the set of coordinates that are assigned using the Index-mapping method.

3. In this third step, if necessary, the individuals of the PoFs of amplifiers that are non-dominated in the new loading conditions and have minimum distance, in the coordinates space, to the selected amplifier are identified.

4. In this final step, one of the designs identified in the previous step is chosen randomly and the indexing variables are updated with its coordinates.

In the example shown in the figure, individuals of a low-level PoF of 3 design objectives are indexed using two coordinates in the no-load space. As it can be seen, two different cases are illustrated, where the transformation technique is used to identify the individuals that are not valid in the final space. In case 1, the selected individuals is valid and, thus, the mutation of the indexing variables ends here. In case 2, on the other hand, the selected design is not valid in the final space and steps 3 and 4 are necessary. At step 3, the individuals with minimum distance

to the selected individual are identified. Finally, at step 4, one of the individuals identified at step 3 is chosen randomly, and the values of the indexing variables are updated with the coordinates of the chosen individual.

Pareto-optimal front of the CT-LP filter

The PoF of the CT-LP filter for a GSM standard is generated with a population of 100 individuals and after 100 generations of the evolutionary process. The filter performances are evaluated using HSPICE® and the amplifiers are evaluated using device-level models. The obtained result is shown in Fig.5.7.

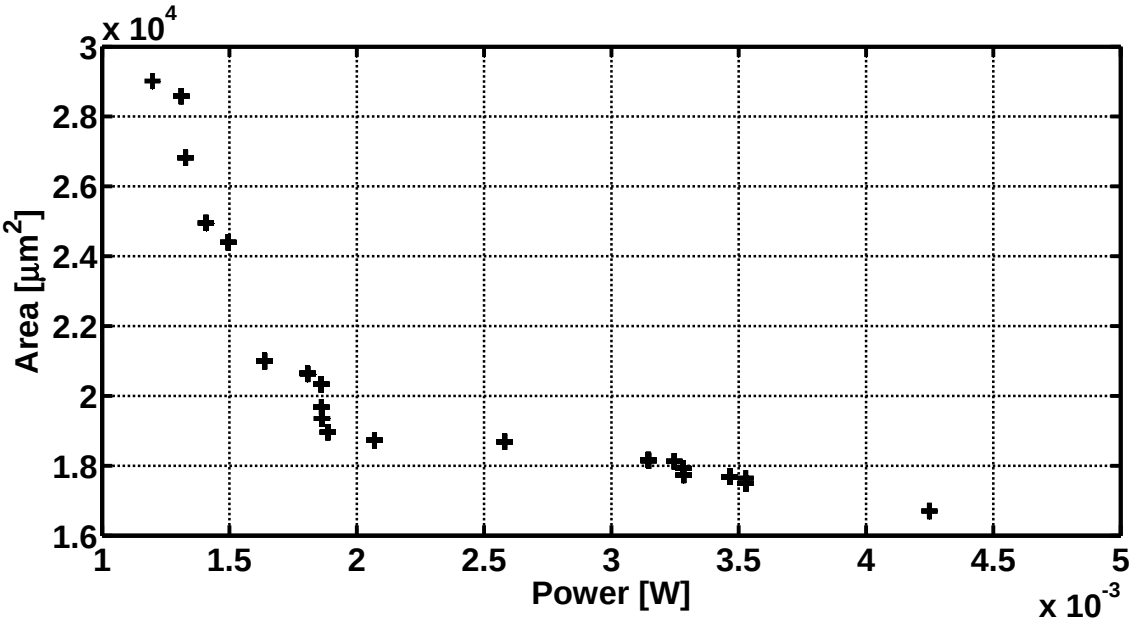


Figure 5.7: PoF of the filter for GSM standard.

As it can be seen, it is formed by around 20 different designs. It is interesting to discuss the characteristics of the amplifiers of the low-level PoFs that are used in the designs of the PoF of the filter. For this, let us focus on the projection of the PoFs of amplifiers onto the area and power consumption plane, which are shown in Figures 5.8 and 5.9.

The amplifiers that are used in the final PoF of the filter, which are shown in red circles in the same figures, are near the region of lowest area and power consumption values. This means that the optimization process has been able to explore the low-level PoFs efficiently, selecting at the end those amplifiers that, while allow to fulfill the filter design constraints, present a good trade-off between the area and the power consumption. By efficiently, we refer here to the fact that,

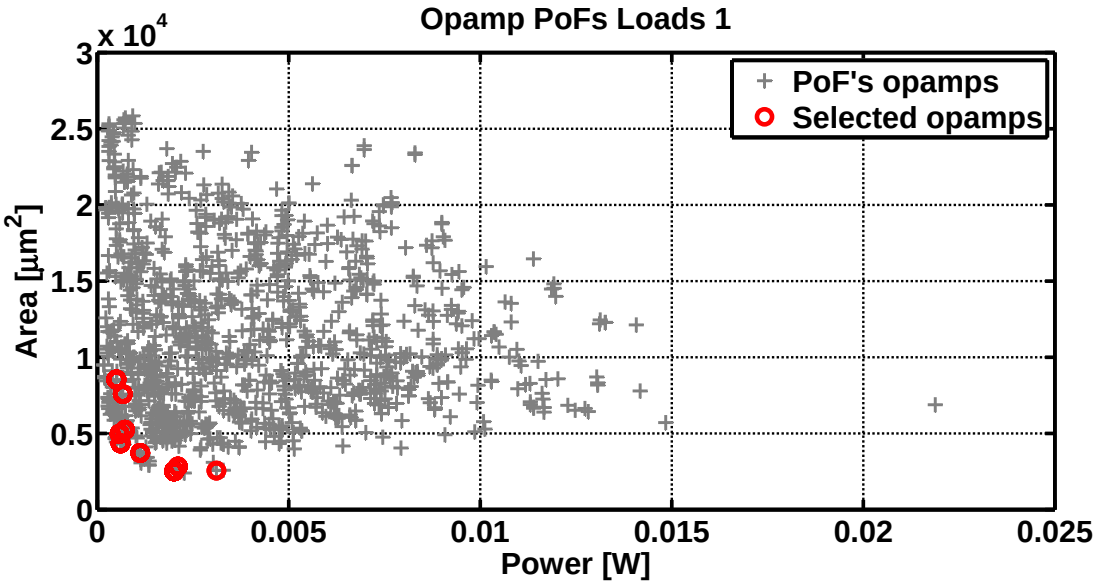


Figure 5.8: Projection onto the are-power consumption plane of the PoFs of amplifiers used to implement OPAMP A of the filter. The amplifiers used in the final front of the filter are enclosed in red circles.

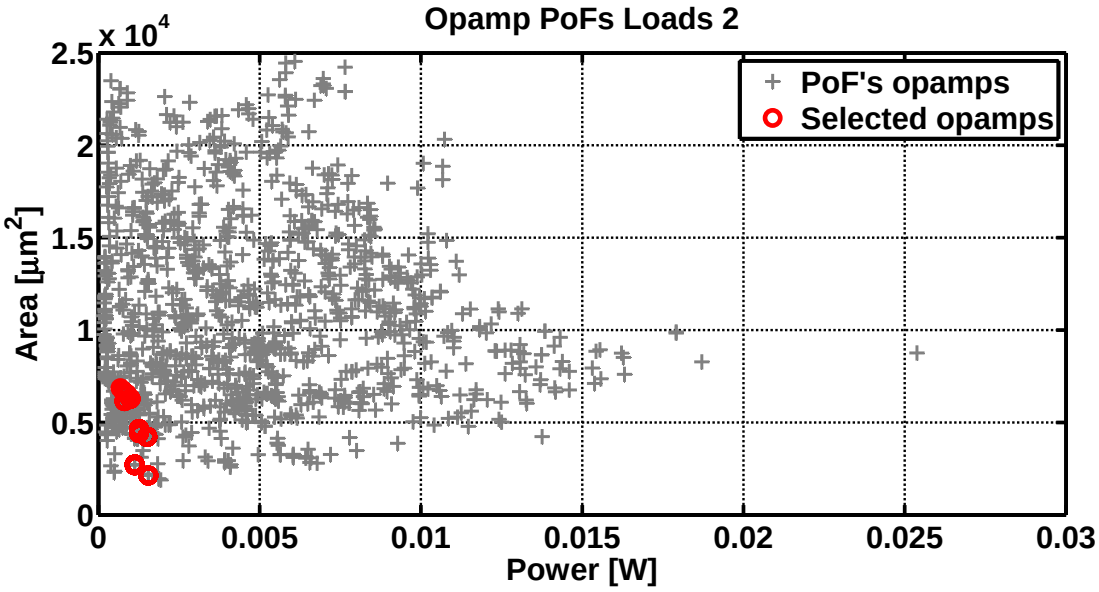


Figure 5.9: Projection onto the are-power consumption plane of the PoFs of amplifiers used to implement OPAMP B of the filter. The amplifiers used in the final front of the filter are enclosed in red circles.

in order to get to the selected amplifiers, the optimization process has not had to explore all possible combinations of designs of the low-level PoFs. From a total of more than 1 million combinations ($1.2 \cdot 10^3$ designs from PoFs for opamp A $\times$ $1.2 \cdot 10^3$ opamps from PoFs for opamp B), a maximum of 10^4 have been explored (100 filter designs $\times$ 100 generations), which is less than 1% of the total.

Comparison with Top-down Design Flow

It is of interest to compare these results with those obtained by traditional design methodologies. For this, a set of ten designs are selected from the PoF of the filter generated in the previous section. The selected designs, which are depicted in Fig.5.10, are chosen so that they are uniformly distributed in the PoF.

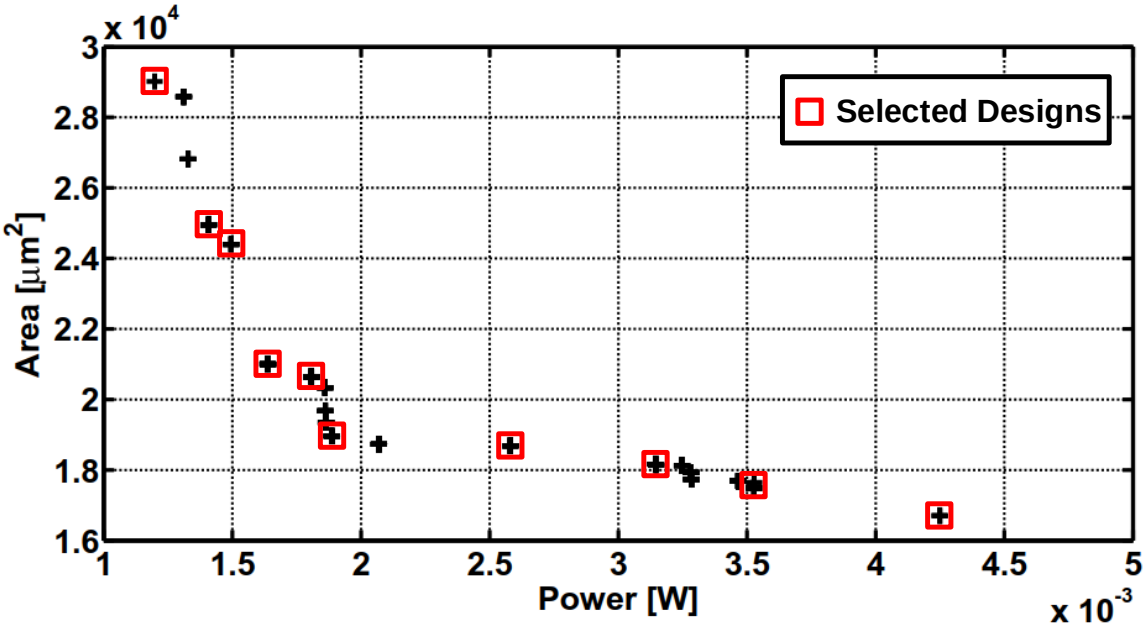


Figure 5.10: Selected designs of the PoF of the filter.

For each one of these designs, the CT-LP filter will be designed for the GSM standard using a top-down flow of design. The main steps of the design flow are described in the following lines.

First the set of selected designs are optimized using the design variables of the filter (the passive network) and macro-models for the amplifiers. A block diagram of the macro-model used for the amplifiers is shown in Fig.5.11. As it can be seen, the macro-model is composed of three stages -input, intermediate and output- each modeling different non-ideal effects. These non-idealities are the input parameters of the opamp macro-model and the optimization process will determine their

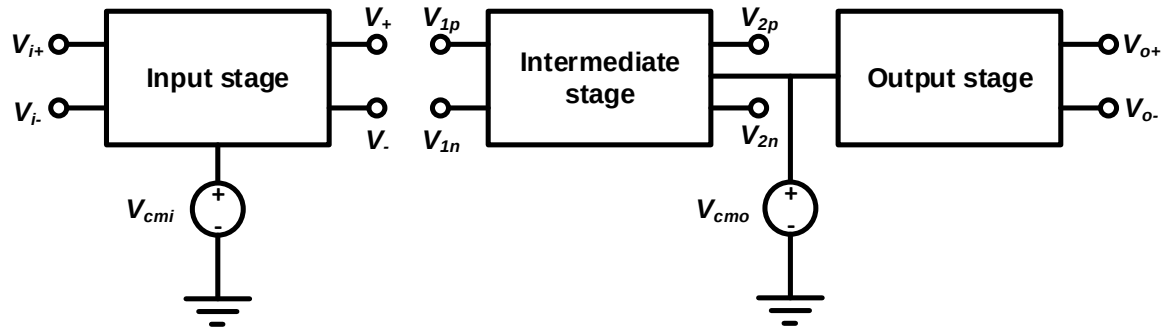


Figure 5.11: Block diagram of the macro-model used for the optimization of the filter at the first step of the top-down process.

required values for the filter to operate correctly. These values will be used as design constraints for the design optimization of the amplifiers.

In this first step of the top-down design process, the power and area of the filter are minimized while the design constraints are met. At this step, the power consumption of the filter and the area are calculated as estimations. The design variables are the non-idealities that are used as input parameters of the opamp macromodel. These non-idealities are shown in Table 5.4. The non-idealities considered not only address frequency response limitations but also, large signal deviations that take into account the finite dynamic range of real opamps and the existence of harmonic distortion mechanisms [67].

Fig.5.12 shows the composition of each stage of the opamp macromodel. The role of each stage in modeling the set of opamp non-idealities is as follows:

- **Input stage**. This stage models the first three input parameters in Table 3.2, i.e., the input offset voltage, the common-mode input capacitances, and the differential input capacitance.

- **Intermediate stage**. The non-idealities modeled here are: the differential-input differential-output low-frequency gain, dynamic effects, slew-rate, nonlinear input transconductance, as well as CMRR, PSRR effects, and the impact of the non-ideal common-mode transfer function (i.e., common-mode input to common-mode output).

- **Output stage**. The output stage models the positive and negative saturation voltages as well as the output resistance.

The rest of design variables of the filter, those that define the passive network, are fixed and their value is that of the corresponding bottom-up design of the PoF

Table 5.4: Macromodel Input Parameters

Parameter	Default	Unit	Description
V_{OS}	0.0	V	Input offset voltage
C_{ic}	0.50e−12	F	Capacitance from input terminal to AC ground
C_{id}	0.20e−12	F	Differential input capacitance
add_db	70.0	dB	Differential-input differential-output low-frequency voltage gain
fp_1	1e3	Hz	1st pole position
fp_2	1e6	Hz	2nd pole position
sr	35.0	$V/\mu s$	Slew-rate
acc_db	−40	dB	Common-mode input to common-mode output voltage gain
CMRR[a]	60	dB	Low-frequency common-mode rejection ratio
$PSRR^+$	80	dB	Low-frequency positive power supply rejection ratio
$PSRR^-$	80	dB	Low-frequency negative power supply rejection ratio
fz_{dd}	2.0e+04	Hz	First zero of the positive power supply transfer characteristic
fz_{ss}	2.0e+04	Hz	First zero of the negative power supply transfer characteristic
fz_{cc}	2.e+050	Hz	First zero of the common-mode transfer characteristic
r_{out}	1.00e+03	W	Resistance from output terminal to common-mode output voltage
os_{pos}	1.0	V	Positive output swing from common-mode output voltage
os_{neg}	1.0	V	Negative output swing from common-mode output voltage

of the filter. The result of this high-level optimization is the set of specifications for the amplifiers (DC-Gain, fu and phase-margin).

At the next step of the top-down design process, the amplifiers are synthesized to attain the specifications that have been determined at the first step. At this step, the power and the area of the amplifiers are minimized while the design constraints are met. These design constraints are the DC-Gain, fu and phase-margin values obtained in the previous step, plus the constraints used in section 3.1.2 of chapter 3 that ensure the correct operation of the amplifier.

Finally, the complete filter design is simulated at transistor-level to get the final and more accurate values of area and power consumption, as well as the values of the design constraints. An illustrative diagram of the design flow is depicted in Fig.5.13. At both levels of the optimization, a single-objective stochastic optimization tool [34, 66] has been used in combination with HSPICE®.

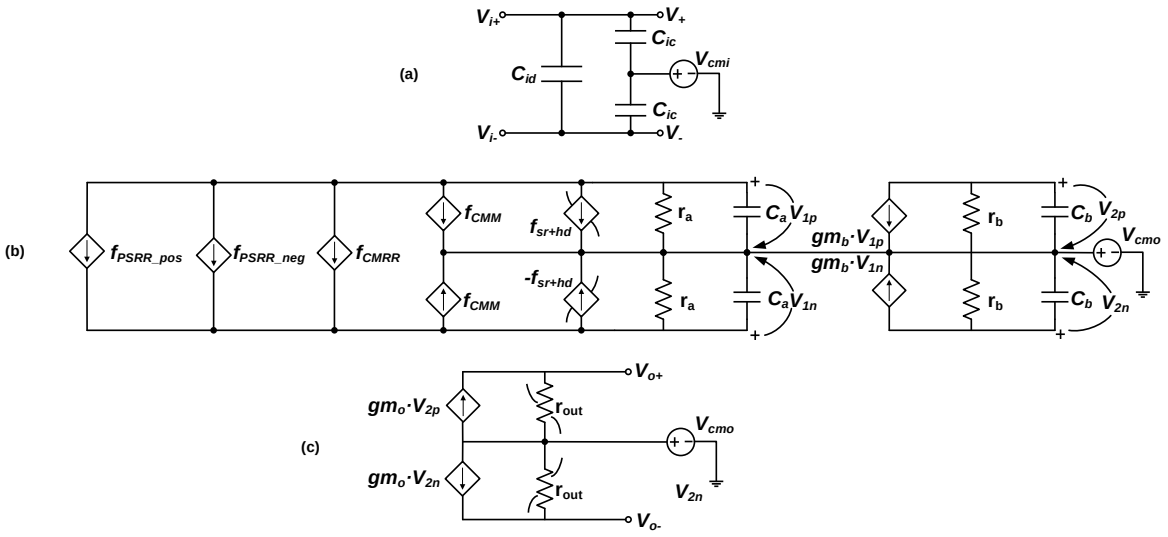


Figure 5.12: (a) Input, (b) intermediate, and (c) output stages of the opamp macromodel.

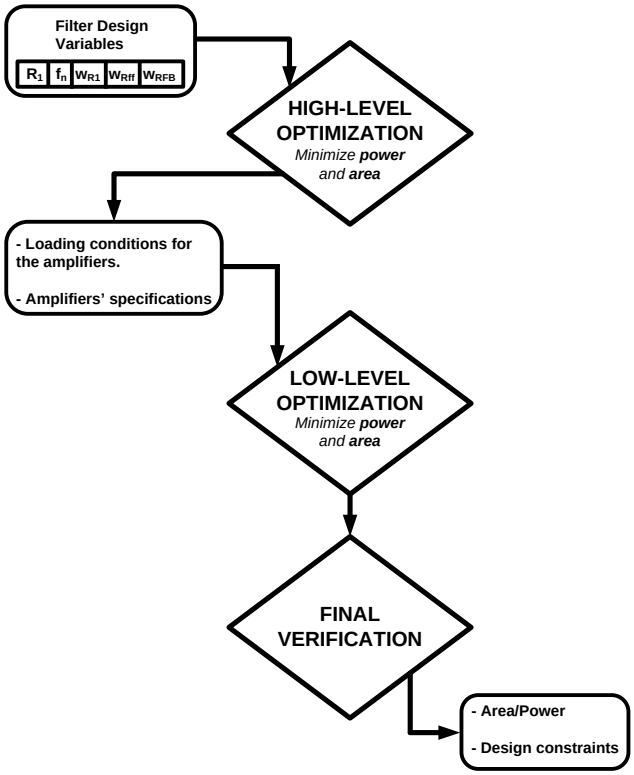


Figure 5.13: Main steps of the Top-down design flow.

The area and power consumption of the selected designs from the previously generated PoF (B-U designs), as well as those of the designs obtained with the top-down design flow described above (T-D designs), are shown in Fig.5.14. As it can be seen, none of the selected designs obtained with the top-down design approach is better than the solutions obtained using the bottom-up methodology proposed in this Thesis. The better results obtained with the bottom-up approach are a direct consequence of using previously generated low-level PoFs, which ensures that the amplifiers that will be used are optimal and near the best trade-off regions of the performances of interest.

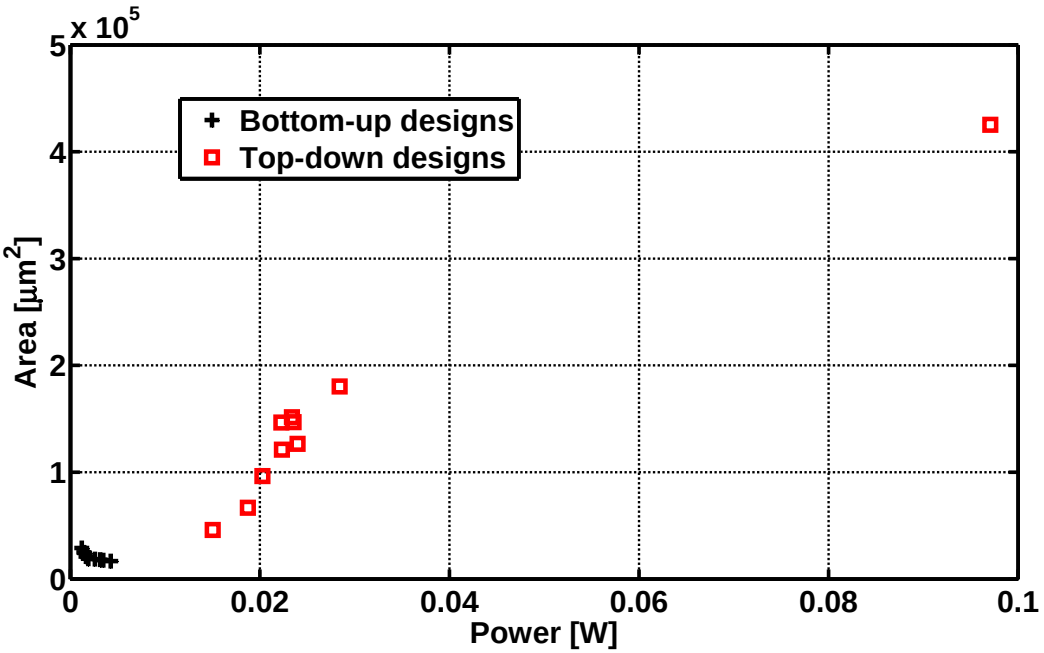


Figure 5.14: Area and power consumption of the selected designs and those obtained with the top-down flow of design.

Table 5.5 summarizes the performances of the amplifiers that are used in one the ten designs selected in Fig.5.10 and obtained using the methodology proposed in this Thesis. The same values are also shown for comparison for the same filter design obtained using the top-down approach. Note that these designs have the same values of the variables that define the passive network of the filter. In Table 5.6, the values of the design variables of those amplifiers are shown. In the top-down approach, the amplifiers are optimized for the loading conditions imposed by the passive network and to provide a set of performance specifications that are estimated in an intermediate step. This estimation is performed relaxing the performance specification as much as possible while meeting the filter specs, but

Table 5.5: Performances of the amplifiers used in the filter designs.

Performance [units]		**OPAMP A**		**OPAMP B**	
		B-U design	**T-D design**	**B-U design**	**T-D design**
DC-Gain	[dB]	108.9	114.3	120.1	110.5
fu	[MHz]	25.3	18.9	51.7	15.6
PM	[°]	44	29	51	30
power	[mW]	1.29	43.4	8.33	53.7
area	[μm^2]	$8.46 \cdot 10^3$	$1.44 \cdot 10^5$	$1.36 \cdot 10^4$	$2.67 \cdot 10^5$
Z_{OUT}	[$k\Omega$]	100	2.60	6.32	1.64

with no controlled relationship with power and area minimization of the amplifiers. As a result, the amplifiers designed using this approach can not compete, in terms of power consumption and area, with designs of the PoF and, thus, the filter obtained is not optimal in terms of area and power consumption.

5.3 GENERATION OF THE MULTI-MODE PARETO-OPTIMAL FRONT OF THE CT-LP FILTER

The hierarchical composition of PoFs has been illustrated with the optimization of the CT-LP filter for the GSM standard. The next experiment illustrates the generation of a mm-PoF of the filter by hierarchical composition of the low-level PoFs of the amplifiers. The demonstration vehicle for this will be the same CT-LP filter. However, in this case the filter will be optimized to fulfill specifications of two standards: GSM and DECT. For this, the new evolutionary algorithm described in section 3.2.1 is used. Besides, in order to cope with the different requirements of both standards, the low-level PoFs of amplifiers will be also multi-mode. This adds a whole new casuistry that must be considered for the correct optimization of the reconfigurable filter. This is explained in detail in the following sections.

5.3.1 *Different specifications for different standards*

As said above, the reconfigurable filter must fulfill specifications for the GSM and DECT standards. These standards, as depicted in Fig.5.15, are in different regions of the frequency spectrum and thus the requirements for the filter will also be different.

These requirements, which will be treated as constraints for the optimization process, are shown in Table 5.7. As it can be seen, the attenuations and cut-off

Table 5.6: Design variables of the amplifiers used in the filter designs.

Variable [units]		OPAMP A		OPAMP B	
		B-U design	T-D design	B-U design	T-D design
w_1	$[\mu m]$	235.4	629.0	197.5	601.3
w_3	$[\mu m]$	39.9	782.3	279.4	459.4
w_5	$[\mu m]$	146.4	89.7	80.2	29.3
w_{10}	$[\mu m]$	61.5	478.5	444.6	210.1
w_{12}	$[\mu m]$	462.5	786.4	733.3	673.9
w_{1c}	$[\mu m]$	147.5	162.9	74.0	175.6
l_{bp}	$[\mu m]$	1.0	1.1	1.2	0.9
l_1	$[\mu m]$	3.0	5.0	1.5	0.5
l_{10}	$[\mu m]$	0.36	3.4	1.6	0.6
l_{14}	$[\mu m]$	0.81	1.6	0.5	2.0
l_{1c}	$[\mu m]$	2.1	2.5	2.0	3.9
l_{3c}	$[\mu m]$	4.2	4.5	3.4	4.4
C_C	[pF]	1.3	1.9	1.8	1.0
R_C	[kΩ]	1.3	2.0	0.9	1.5
α	[-]	158.6	186.7	112.8	192.4
I_{bias}	$[\mu A]$	39.3	6.6	121.2	353.2

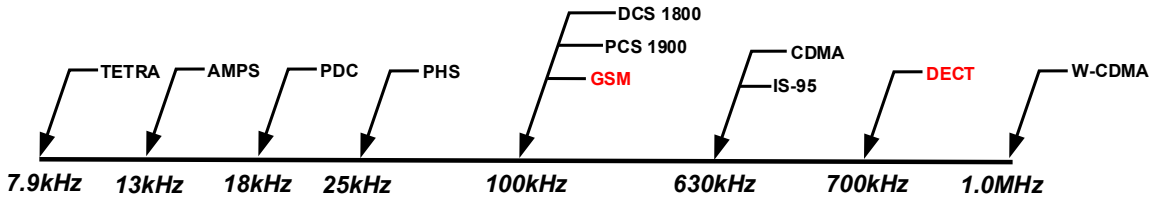


Figure 5.15: Frequency spectrum for different standards.

frequency required for DECT are higher than those of GSM (6.0 MHz as maximum cut-off frequency for GSM and 10.0 MHz for DECT). Thus, amplifiers with higher fu may be necessary to fulfill DECT specifications. For this reason, mm-PoFs of reconfigurable amplifiers will be used in this case. The same amplifier described in section 3.2.2 will be used. However, it will operate in 2 different modes. The reconfiguration strategy and directive will be to change the bias current from I_{bias}

for operation mode 1 to $10 \cdot I_{bias}$ for operation mode 2. This, as explained in section 3.2.2, increases the unity-gain frequency of the amplifier.

Table 5.7: Constraints for the Optimization of the Reconfigurable Filter.

GSM STANDARD		**DECT STANDARD**	
Att.1G	$>$ 30 dB	Att.1D	$>$ 34 dB
Att.2G	$>$ 30 dB	Att.2D	$>$ 34 dB
Att.3G	$>$ 30 dB	Att.3D	$>$ 34 dB
dimar 1G	$<$ 1	dimar 1D	$<$ 1
dimar 2G	$<$ 1	dimar 2D	$<$ 1
DC-Gain G	$>$ 50 dB	DC-Gain D	$>$ 50 dB
fcut G	$<$ 6.0 MHz	fcut D	$<$ 10.0 MHz

The design variables at filter level and their ranges are detailed in Table 5.8. Variables $rr1$ and fn and the width of resistors define the passive network of the filter. The ranges of these variables have been chosen taking into accounts the technology that is used as well as design issues for the proper operation of the filter. The rest of variables are used for the exploration of the low-level mm-PoFs of amplifiers. The configuration variables are binary variables whose value can be 0 or 1. Their mutation is simple bit-flip mutation: they change to 0 if their value is 1 and vice-versa.

All the design variables are depicted in Fig.5.16. As it can be seen, there are different sets of indexing variables to explore the low-level mm-PoFs. For operation mode 1, intended for GSM standard, coordinates of opamps A1 and B1 are used. For operation mode 2, intended for DECT standard, coordinates of opamps A2 and B2 are used. The *configuration variables*, on the other hand, are used to allow the optimizer to explore different reconfiguration directives: using a different operation mode of the same amplifier for each mode of the filter or using a different amplifier for each mode. Variables m_A1 and m_B1 indicate the operation mode of opamps A1 and B1; op_A indicates whether if opamps A1 and A2 are the same or not and, in case they are, variable m_A indicates if they use the same operation mode or not. Variables op_B and m_B indicate the same relationships for opamps B1 and B2. The *indexing variables* are the sets of coordinates that are used to explore the low-level PoFs of amplifiers. In some cases, the values of the *indexing variables* depend on the *configuration variables*. For example, if opamps A1 and A2 are the same, the coordinates of opamps A1 and A2 will be the same.

Table 5.8: Design Variables of the Reconfigurable Filter.

	Name	Min. value	Max. value
Independent variables	$rr1$	$20 \cdot 10^3\ \Omega$	$200 \cdot 10^3\ \Omega$
	fn	$70 \cdot 10^4$ Hz	$120 \cdot 10^4$ Hz
	w_{R_1}	$0.75\mu m^2$	$1.25\mu m^2$
	$w_{R_{FF}}$	$0.75\mu m^2$	$1.25\mu m^2$
	$w_{R_{FB}}$	$0.75\mu m^2$	$1.25\mu m^2$
Configuration variables	m_{A1}	0	1
	m_{B1}	0	1
	op_A	0	1
	m_A	0	1
	op_B	0	1
	m_B	0	1
Indexing variables	Coord. 1 A.1	1	16
	Coord. 2 - 3 A.1	1	15
	Coord. 1 A.2	1	16
	Coord. 2 - 3 A.2	1	15
	Coord. 1 B.1	1	16
	Coord. 2 - 3 B.1	1	15
	Coord. 1 B.2	1	16
	Coord. 2 - 3 B.2	1	15

The mutation of each set of coordinates is carried out as explained in section5.2. However, as the low-level PoFs of amplifiers are multi-mode fronts, it is convenient to give a more detailed description of how the exploration of these low-level mm-PoFs is performed. In this case, the mm-PoFs are split in the different operation modes, that is, all modes 1 of the mm-PoFs are merged in one set and all modes 2 are merged in another set. Afterwards, each one of these sets is indexed in the no-load space. Thus, depending on the operation mode of the amplifiers that is used, which is determined by design variables m_A1 and m_B1 (or m_A2 and m_B2), the process described in section5.2 is performed on the corresponding set of low-level PoFs. An example of this process is depicted in Fig.5.17 for the case of low-level mm-PoFs of 3 design objectives that are indexed using only 2 coordinates.

In order to change the operation mode of the filter, the components of the passive network are also switched. For this, design variables $rr1$ and fn change their values

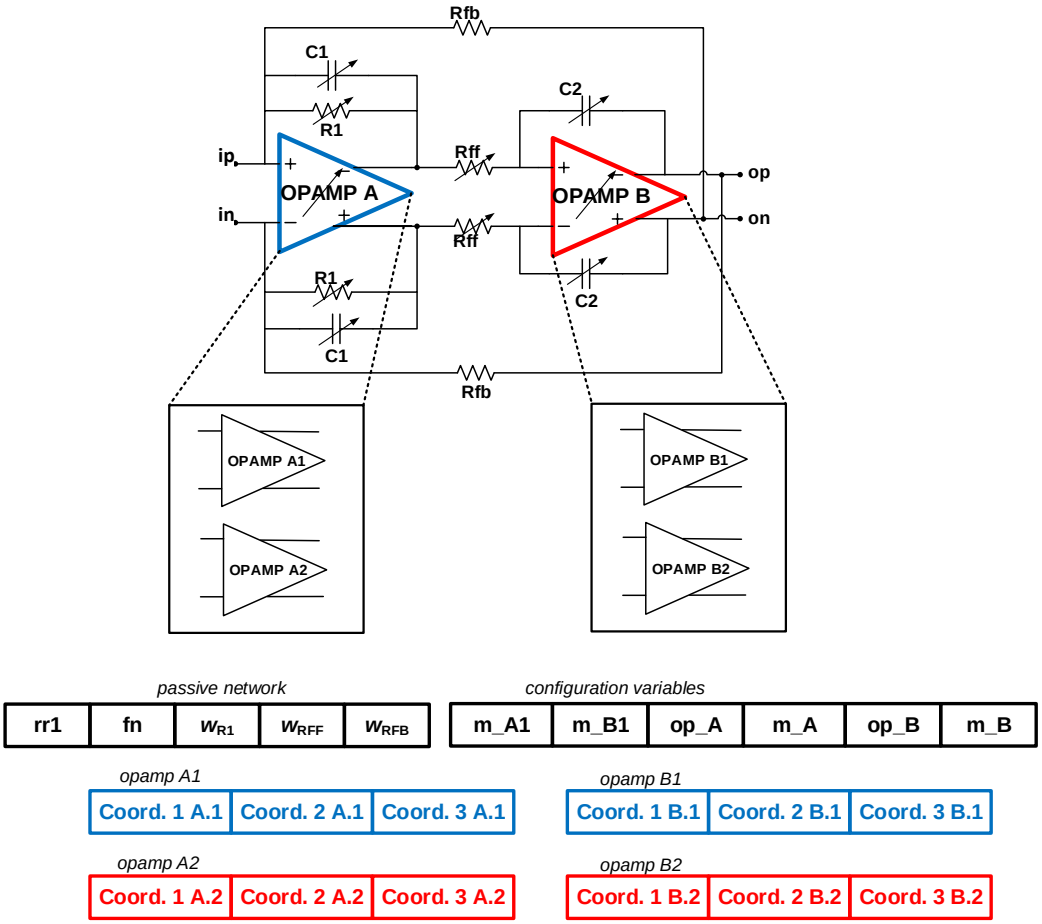


Figure 5.16: Design variables used in the generation of the mm-PoF of the CT-LP filter.

as shown in Table 5.9. The values used in this reconfiguration directive are chosen so that the operation of the filter can be switched between the frequency bands of both GSM and DECT standards [67].

Table 5.9: Reconfigurable Design Variables of the Reconfigurable Filter.

Design variable	**Value Mode** 1	**Value Mode** 2
Resistor R_1	$rr1$	$rr1/3$
Natural frequency	fn	$10 \cdot fn$

The design objectives at the filter level will be the area, the power consumption and a third design objective, which has been called **complexity**, will be also minimized. Complexity accounts for the cost of each filter design in terms of the

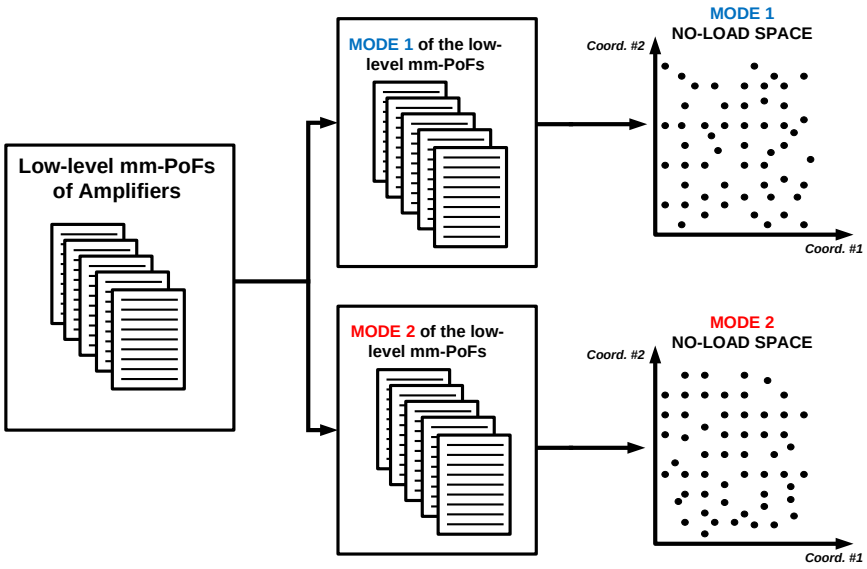


Figure 5.17: The low-level mm-PoFs are separated in two sets, one for each operation mode of the amplifiers. Depending of the operation mode of the amplifiers that is used in the high-level design, the mutation of the indexing variables is performed on the corresponding set.

number of reconfigurable amplifiers that are used and in terms of the different layouts that are used:

$$complexity = layout + reconf \tag{5.5}$$

This is based on two assumptions: the design of a reconfigurable circuit entails more complexity, and, in terms of layout, design cost increases for each different amplifier that is used. For example, let us consider two different filter designs, A and B. Design A uses two reconfigurable amplifiers while design B uses one reconfigurable amplifier for OPAMP A and one single-mode amplifier for OPAMP B. Although two layouts have to be done for both designs, reconfigurable amplifiers are more complex, and thus the complexity in terms of reconfigurability is higher in design A. Using this idea, complexity is defined as the sum of two quantities: $layout$, which accounts for the number of different layouts that have to be designed, and $reconf$, which accounts for the number of reconfigurable amplifiers that are used. In the example described above, complexity of design A is 4 while that of design B is 3.

5.3.2 *Generation of the mm-PoFs of reconfigurable amplifiers*

As in the example in section 5.2, and since no library of mm-PoFs has been previously generated, the first step is the generation of the mm-PoFs of the amplifiers and, for which the load that they will see in the filter must be estimated. In this case, as the passive network of the filter is changing, the load seen by the amplifiers will be also different depending on the operation mode of the filter. The ranges of the loads seen by each amplifier in each operation mode of the filter are depicted in Fig.5.18. It can be seen that, although the load seen by OPAMP B2 is covered by that seen by OPAMP B1 (because R_{FB} and the load of the filter do not change) the load ranges seen by OPAMP A2 are not covered by those seen by OPAMP A1. Therefore, besides the fronts that will be generated for the loading conditions estimated in section 5.2, 4 additional fronts of amplifiers will be generated for the loading conditions detailed in Table 5.10. In total, 12 mm-PoFs of amplifiers will be generated.

Table 5.10: Loading conditions for the generation of the PoFs of amplifiers for Mode 2 of the filter.

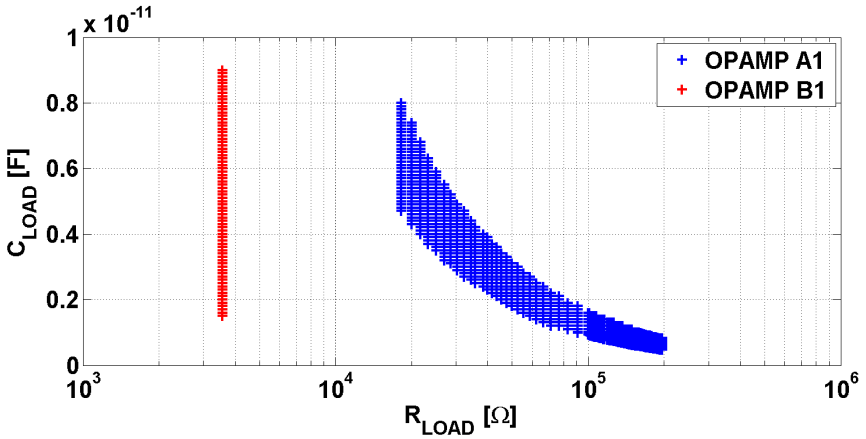
Amplifier PoF	R_{LOAD}	C_{LOAD}
9	$5 \cdot 10^3\ \Omega$	3.0 pF
10	$10 \cdot 10^3\ \Omega$	2.0 pF
11	$30 \cdot 10^3\ \Omega$	0.5 pF
12	$60 \cdot 10^3\ \Omega$	0.1 pF

The design objectives and constraints of each operation mode of the amplifiers are detailed in Table 5.11. As explained in section 5.3.1, the reconfiguration strategy and directive will be to change the bias current from I_{bias} for operation mode 1 to $10 \cdot I_{bias}$ for operation mode 2.

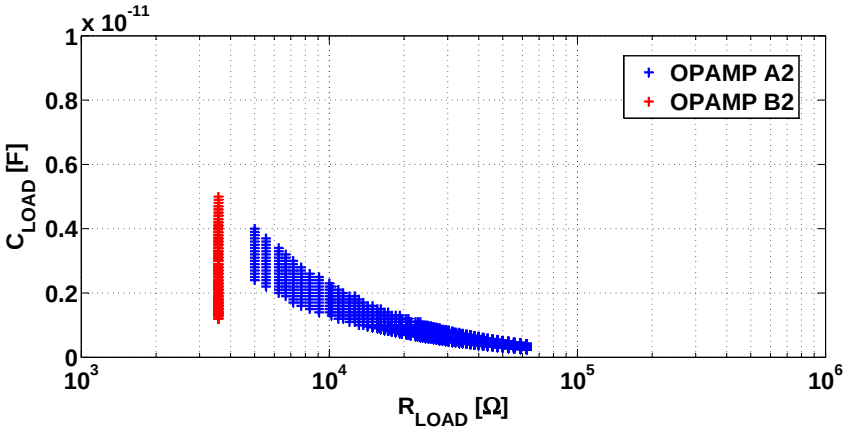
5.3.3 *Generation of the mm-PoF of the filter*

The mm-PoF of the filter, generated with a population size of 100 individuals and after 100 generations of the evolutionary process, is shown in Fig.5.19. As it can be seen, there is a trade-off between the complexity of design and the other two design objectives: power consumption and area.

Solutions with complexity 1 (black crosses) show a worse trade-off between power and area. However, they use the same amplifier operating in the same mode for both OPAMP A and OPAMP B in GSM and DECT standards and, thus, their



(a) Load ranges for operation mode 1 of the filter.



(b) Load ranges for operation mode 2 of the filter.

Figure 5.18: Load ranges for OPAMP A and OPAMP B in the 2 operation modes of the filter.

design is less complex. On the other hand, solutions with complexity 2 (green circles) use a different amplifier to implement OPAMP A and OPAMP B, but both amplifiers use the same operation mode for both modes of the filter and, thus, no reconfiguration of the amplifiers is required. Although two different amplifiers are required, and their design is therefore more complex, they have better values of power and area than those of the designs with complexity 1. Finally, solutions with complexity 3 (blue and red squares) use a reconfigurable amplifier to implement opamps A1 and A2 and a single-mode amplifier to implement opamps B1 and B2. Although these are the most complex designs, their *powerconsumption* in GSM mode is better than that of any design with complexity 1 or 2. These results also demonstrate the ability of the optimizer to explore different reconfiguration

Table 5.11: Design objectives and constraints for the generation of the mm-PoFs of the reconfigurable amplifiers.

Design Objectives	**Mode** 1	**Mode** 2
DC-Gain	maximize	maximize
fu	maximize	maximize
power	minimize	minimize
area	minimize	minimize
Constraints	**Mode** 1	**Mode** 2
Phase Margin (PM)	$60° \leq PM \leq 90°$	$60° \leq PM \leq 90°$
Output Swing (OS)	≥ 3.6 V	≥ 3.6 V
dm (for each transistor)	≥ 1.1	≥ 1.1

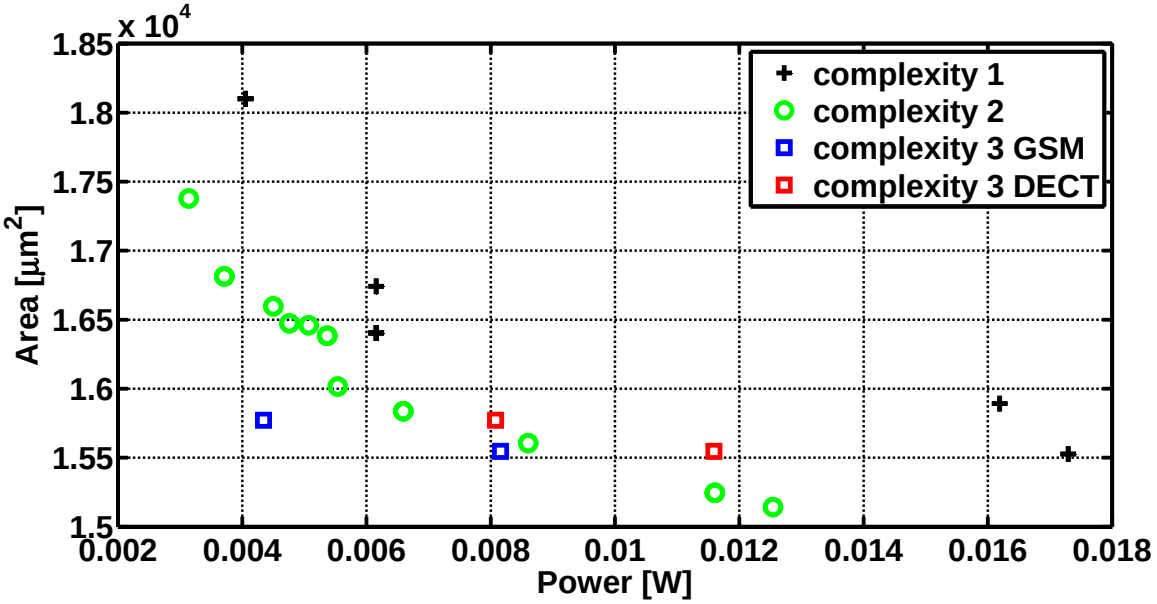


Figure 5.19: Mm-PoF of the filter for GSM and DECT standards.

strategies for the filter, finding optimal solutions in terms of complexity of design and area-power consumption trade-off. This is something that, until now, was only possible with the experience of expert designers or by trial and error methods.

5.4 SUMMARY

In this Chapter, the methodology described in the previous chapters has been applied to the design of an active, reconfigurable low-pass filter. For this, previously generated mm-PoFs of reconfigurable operational amplifiers have been used. The exploration and hierarchical composition of the fronts of amplifiers has been carried out using the load transformation technique along with the Index-mapping method, both described in chapter 4. Besides, it has been demonstrated that the methodology presented in this work can easily improve what can be obtained by traditional approaches. In the next chapter, the methodology is tested in the design of a reconfigurable $\Sigma\Delta$ modulator that must be fulfill specifications for three different communication standards.

6

DESIGN EXAMPLE II: MULTI-STANDARD ΣΔ MODULATOR

In this Chapter, the methodology presented in this Thesis is applied to the design of a 130-nm CMOS multi-standard ΣΔ Modulator. Starting with a set of high-level specifications, a set of candidates solutions of an expandable cascade topology are considered for each standard. For each one of them, a mm-PoF will be generated, optimizing the power consumption of each operation mode and the area occupation. For this, a set of previously generated lower-level mm-PoFs of operational amplifiers are used. This allows much more accurate estimations of power consumption and the area than in traditional design flows. The modulator performances are evaluated using MATLAB Simulink®, for which the performances of the amplifiers from the low-level mm-PoFs are used in the high-level model of the modulator. Before going into detail about the application of the methodology proposed in this work in the design of the modulator, it is necessary to give a brief introduction about the basic concepts regarding the operation of Analog-to-digital converters and ΣΔ modulators.

6.1 BASIC CONCEPTS AND FUNDAMENTALS

Analog-to-digital converters (ADCs) are electronics systems that perform the transformation of analog signals, which are continuous in time and in amplitude, into digital signals, which are discrete in both time and amplitude. Fig.6.1 illustrates the general block diagram of an ADC intended for the conversion of low-pass signals, which essentially consists of an antialiasing filter (AAF), a sampler and a quantizer [68].

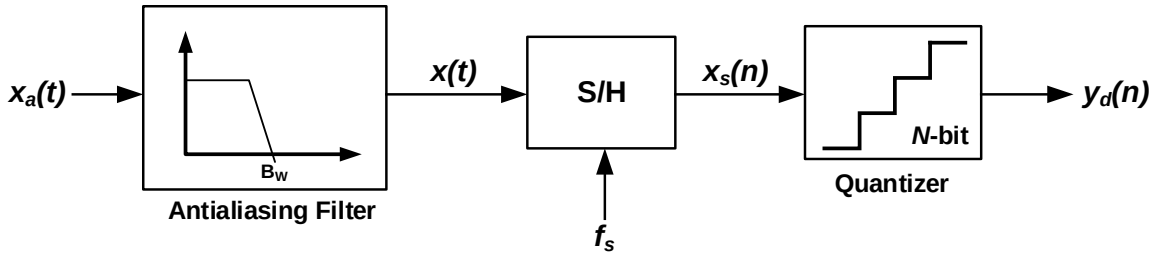


Figure 6.1: General block diagram of an A/D converter.

The AAF prevents out-of-band components from holding over the signal bandwidth, B_w, during the subsequent sampling. The sampling process performs the continuous-to-discrete transformation of the input-signal in time and imposes a limit on the bandwidth of the analog input signal. According to the *Nyquist* theorem, to prevent information loss, the input signal, $x(t)$, must be sampled at a minimum rate of $f_N = 2B_w$, often referred to as the *Nyquist* frequency. On the basis of this criterion, ADCs in which analog input signal is sampled at the minimum rate ($f_s = f_N$) are called *Nyquist*-rate ADCs. Conversely, ADCs in which $f_s > f_N$ are called *oversampling* ADCs. How much faster than required the input signal is sampled is expressed in terms of the oversampling ratio (OSR), defined as:

$$OSR = \frac{f_s}{2B_w} \tag{6.1}$$

The quantization process introduces another limitation on the performance of an ideal ADC, since an error is generated while performing the continuous-to-discrete transformation of the input signal in amplitude, commonly referred to as quantization error [68]. An approach to further increase the accuracy of an oversampling ADC is shaping the quantization noise in the frequency domain -i.e., filtering it- in such a way that most of its power lies outside the signal band. This is illustrated in Fig.6.2, where the quantization noise is conceptually obtained by subtracting the quantizer input signal $q(n)$ from its output $y(n)$ and then passes through a filter transfer function, usually called noise transfer function (NTF). For quantizers working on low-pass signals, NTF is of high-pass type and can be easily obtained from a differentiator filter, with a Z-domain transfer function given by:

$$NTF(z) = \left(1 - z^{-1}\right)^L \tag{6.2}$$

where L stands for the filter order.

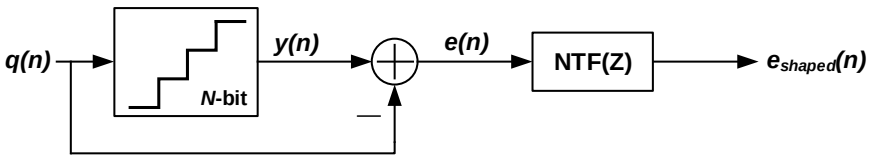


Figure 6.2: Conceptual block diagram of quantization noise shaping.

Sigma-Delta (ΣΔ) ADCs rely on a feedback path to achieve a closed-loop control of the quantization error. Fig.6.3 illustrates the basic block diagram of a ΣΔ ADC intended for the conversion of low-pass signals, which consists of:

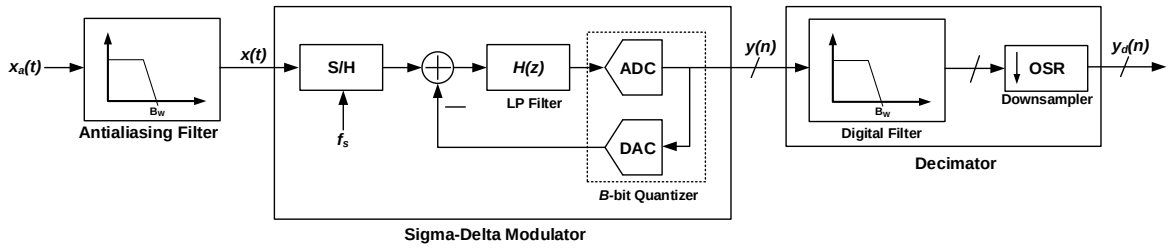


Figure 6.3: General block diagram of a ΣΔ ADC. A low-pass discrete-time ΣΔM is assumed.

- **Antialiasing filter (AAF)**, which band limits the analog input signal to avoid aliasing during its subsequent sampling.
- ΣΔ **modulator (ΣΔM)**, in which the oversampling and quantization of the band-limited analog-to-signal take place. The quantization noise of the embedded B-bit quantizer is shaped in the frequency domain by placing an appropriate loop filter $H(z)$ before it and closing a negative feedback loop around them.
- **Decimator filter**, in which a high-selectivity digital filter sharply removes the out-of-band spectral content of the ΣΔM output and thus most of the shaped quantization noise.

Contrary to Nyquist-rate ADCs, whose performance is mainly characterized by static performance metrics -i.e., monotonicity, gain and offset errors, differential nonlinearity (DNL), and integral nonlinearity (INL) [69]-, ΣΔ ADCs characteristics are typically measured using dynamic performance metrics, which are obtained from the frequency-domain representation of the time-domain digital output sequence. Noise and power metrics are usually the most important measures and comprise:

- **Signal-to-noise ratio (SNR)**, which is the ratio of the output power at the frequency of an input sinusoid to the uncorrelated in-band noise power:

$$SNR(dB) = 10log_{10}\left(\frac{P_{sig,out}}{IBN}\right) \tag{6.3}$$

- **Signal-to-noise-plus-distortion ratio (SNDR)**, which is defined as the ratio of the output power at the frequency of an input sinusoid to the total IBN power, also accounting for possible harmonics at the ΣΔM output.

- **Dynamic Range (DR)**, which can be defined as the ratio of the output power at the frequency of an input sinusoid with maximum amplitude to the output power for a small input amplitude for which $SNR = 0dB$; i.e., so it cannot be distinguished from the error:
- **Effective number of bits (ENOB)**, which can be defined as the number of bits needed for an ideal Nyquist-rate ADC to achieve the same DR as the ΣΔ ADC:

$$ENOB(bit) = \frac{DR(dB) - 1.76}{6.02} \tag{6.4}$$

- **Overload level (OL)**, which is considered to define the maximum input amplitude for which the ΣΔM still operates correctly and can almost be arbitrarily defined, but it is typically chosen as the amplitude for which the SNR drops 6 dB below the peak SNR [70].

Since the ΣΔ modulator is the responsible of the sampling and quantization processes that ultimately limit the accuracy of the A/D conversion, it is the block that has most influence on the performance of the ADC. We will focus on this block from now on.

PERFORMANCE ENHANCEMENT OF ΣΔ MODULATORS

The output of an ideal low-pass *Lth*-order ΣΔ modulator in the *Z*-domain can be considered to be [68]:

$$Y(z) = STF(z)X(z) + NTF(z)E(z) = z^{-L}X(z) + \left(1 + z^{-1}\right)^{L} E(z) \tag{6.5}$$

, where $|STF(f) = 1$ and the NTF builds up an *Lth*-order high-pass shaping of the quantization noise of the embedded quantizer. If a *B*-bit quantizer is employed, the dynamic range of the ΣΔM can be obtained as:

$$DR(dB) = 10log_{10}\left(\frac{P_{sig,out,max}}{IBN}\right) \approx 10log_{10}\left[\frac{3}{2}\left(2^{B} - 1\right)\frac{(2L+1)\,OSR^{(2L+1)}}{\pi^{2L}}\right] \tag{6.6}$$

Note from last equation that the dynamic range of a ΣΔ modulator is ideally determined by the values of L, OSR and B, which can thus be considered as

the three key parameters that define the ΣΔM at the high level. The DR of a ΣΔ modulator can be improved by increasing each of these parameters:

- **Increasing the order of the ΣΔ modulators.** The accuracy of the A/D conversion can be considerably improved by increasing the noise-shaping order, since a larger fraction of the total quantization noise power will be pushed out of the signal band. The DR enhancement if L is increased in one for a given OSR can be expressed as:

$$\Delta DR(sB) \approx 10log_{10}\left[\frac{2L+3}{2L+1}\left(\frac{OSR}{\pi}\right)^2\right] \tag{6.7}$$

  This means that, for instance, the DR of a 4th-order ΣΔM with $OSR = 32$ is ideally 21.3 dB (3.5 bit) larger than that of a third-order ΣΔM.

- **Increasing the OSR ΣΔ modulator.** The DR of an ideal L-order ΣΔ modulator increases with OSR in $3(2L+1)$dB/octave. However, for a given conversion bandwidth B_w, the oversampling ratio cannot be arbitrarily increased, since it leads to a higher sampling frequency f_s for the operation of the ΣΔ circuitry. The latter, if achievable in practice for a given technological process, leads to a larger power consumption.

- **Increasing the number of bits of the ΣΔ modulator quantizer.** An increase in B leads to a decrease of the quantization step Δ and thus to a reduction of the quantization noise power. Each additional bit in the embedded quantizer of a ΣΔM is considered to typically yield a 6-dB (1-bit) improvement on the DR [71]. However, a multibit embedded quantizer requires a multilevel DAC to close the negative feedback loop in the ΣΔM. Contrary to a two-level feedback DAC ($B = 1$), which is inherently linear, a multilevel DAC will in practice be nonlinear to some extent. The DAC nonlinearity will be directly added to the ΣΔM input and will thus appear at the output since $|STF(f)| \approx 1$ within the signal band. Therefore, the linearity required in a multibit DAC equals in practice that wanted for the ΣΔ modulator.

These strategies can be combined in different ways, which has given rise to a huge number of ΣΔM topologies reported in the literature. Attending to the number of quantizers that are employed, we can classify the topologies in Single-loop ΣΔMs, which use only one quantizer, and Cascade ΣΔMs, which employ several quantizers. These topological alternatives are discussed in the following lines.

Single-Loop ΣΔ Modulators

ΣΔ modulators that make use of only one embedded quantizer are usually referred to as single-loop topologies. Fig.6.4 shows a second-order ΣΔ modulator built up by cascading two discrete-time integrators, with each integrator receiving a weighted feedback path from the DAC. Coefficients a_i are usually called integrator scaling or weights.

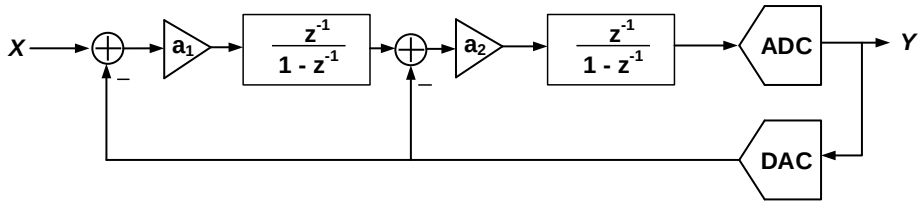


Figure 6.4: Block diagram of second-order ΣΔM.

For the sake of illustration, Fig.6.5 shows a possible implementation of the second-order ΣΔM using fully-differential SC circuitry and assuming single-bit quantization. Note from the first SC integrator that both the modulator input signal and the DAC feedback signal are processed through the sampling capacitor C_S. For the second integrator, the output of the first integrator is processed through both C_{S1} and C_{S2}, whereas the DAC feedback signal is processed only through C_{S2}. The modulator weights are thus implemented as the following capacitor ratios:

$$\begin{aligned} g_1 &= g_1^{'} = \frac{C_S}{C_{I1}} \\ g_2 &= \frac{C_{S1} + C_{S2}}{C_{I2}}, g_2^{'} = \frac{C_{S2}}{C_{I2}} \end{aligned} \tag{6.8}$$

Cascade ΣΔ Modulators

The simplest way to extend a ΣΔM to an arbitrary Lth-order shaping consists of including L integrators before the quantizer. Extending the second-order ΣΔM in Fig.6.4, the topology in Fig.6.6 is obtained, which is known as an Lth-order single-loop ΣΔM with distributed feedback [72].

However, implementing a high-order NTF with a single-loop ΣΔM leads to instability problems $L > 2$, exhibiting unbounded states and poor SNR compared to that predicted by linear analysis. In general, instability appears at the modulator output as a large-amplitude low-frequency oscillation, leading to long bitstreams

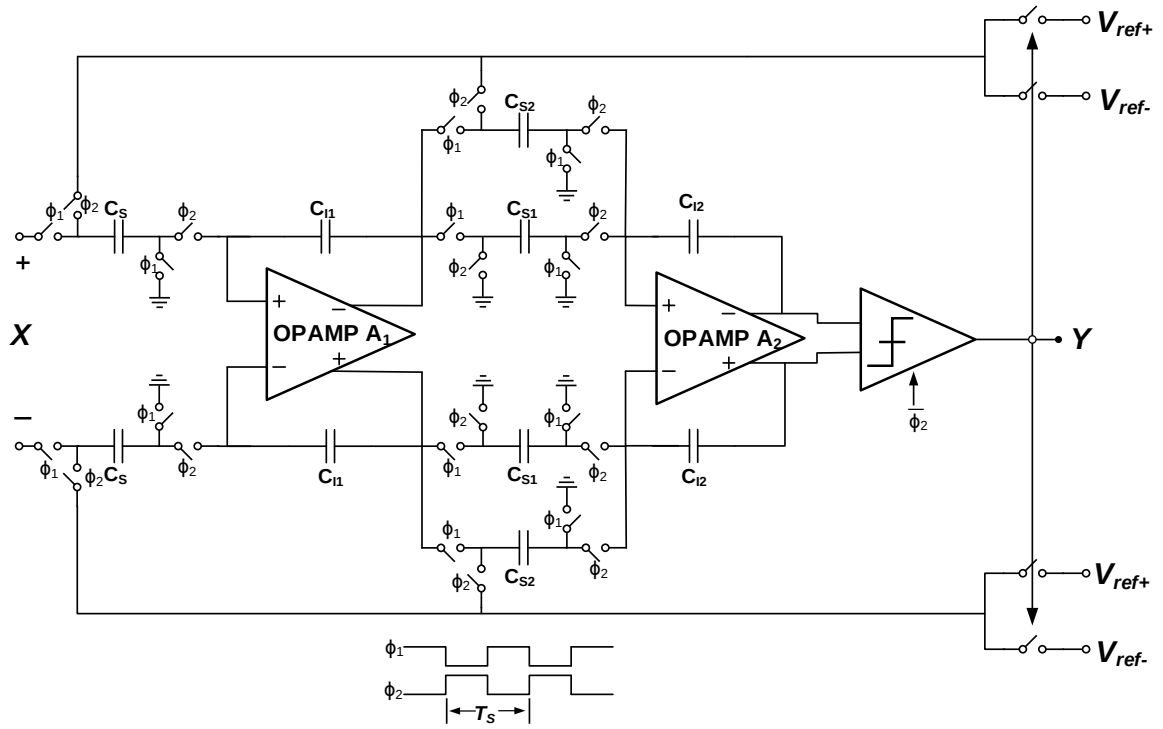


Figure 6.5: Fully-differential SC implementation of a second-order ΣΔ modulator.

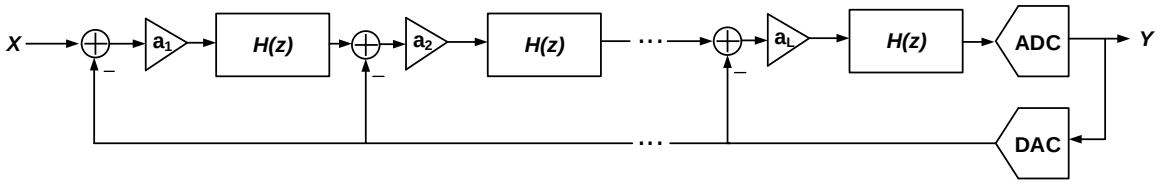


Figure 6.6: High-order single loop ΣΔ modulator with distributed feedback.

of alternating $+1'$s and $-1'$s [68]. Although these problems can be circumvented with adequate scaling coefficients, they result in a significant decrease of the DR compared with an ideal ΣΔM. An alternative approach to obtain a high-order noise-shaping while avoiding instabilities is found in the so-called cascade ΣΔM, also known as multiloop ΣΔM or multistage noise-shaping (MASH) ΣΔM [73–76]. Their architecture is illustrated in Fig.6.7 and consists of N stages of ΣΔ modulators, in which each stage remodulates a scaled version of the quantization error generated in the preceding one. This topology is chosen for the design processes described in this Chapter.

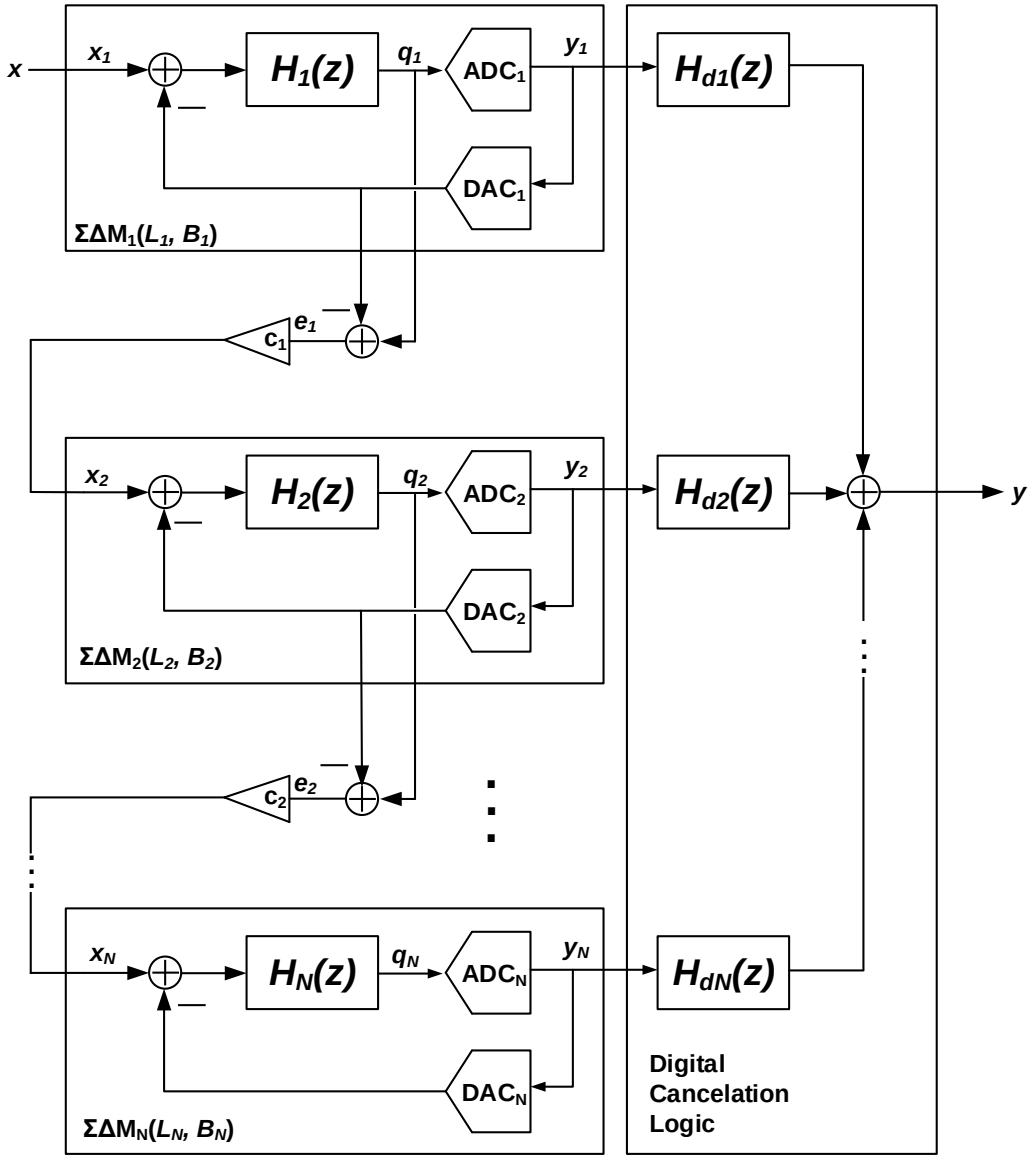


Figure 6.7: General topology of a N-stage cascade ΣΔ modulator.

Now that the fundamentals of ΣΔ modulators have been presented, the design process where the methodology presented in this thesis is applied is described. From a set of high-level specifications of resolution and bandwidth for 3 communication standards, several cascade configurations (for different L, B and OSR values) are considered for each standard. After a high-level analysis of the candidates, only a fraction of them is considered for further analysis.

6.2 FROM SYSTEM-LEVEL SPECIFICATIONS TO BLOCK REQUIREMENTS

The high-level specifications for the GSM, Bluetooth and UMTS standards, which can be seen in Table 6.1, will be our starting point for the design of the reconfigurable ΣΔ modulator.

Table 6.1: ΣΔ Modulator Multi-standard Specifications.

Standard	Resolution	Bandwidth
GSM	13 bits	200 kHz
Bluetooth	11 bits	1 MHz
UMTS	9 bits	4 MHz

To cope with these multi-standard specifications, the expandable cascade topology shown in Fig.6.8 [77] will be used. It is composed of a second-order stage followed by first-order stages, and can be extended to any order, L, by simply adjusting the number of first-order stages. The noise cancellation logic eliminates the quantization errors of all stages but the last one, which is shaped by a noise transfer function (NTF) of order equal to the sum of the orders of all stages. This architecture combines the good performances of a high-order modulator as well as a high stability since only first and second-order modulators are used.

As it has been explained in previous section, any modulator can be characterized by the set of parameters $\{L, B, OSR\}$, where L denotes the order of the modulator, B the number of bits of the last-stage quantizer and OSR the oversampling ratio. The next step in the design of the multi-standard modulator is to select a set of $\{L, B, OSR\}$ candidates that meet the specifications in each standard with minimum power consumption. This exploration is done under the following assumptions:

- Voltage reference of the modulator (V_{ref}) is 1.2 V and the input signal level is placed at -5.6 dBFs in order to maximize the SNDR.
- Given the targeted resolutions, the considered values of L are 2, 3 and 4.
- In order to ease the frequency division of a master clock frequency from one standard to another, the sampling frequency (f_s) is restricted to values $\div 1$, $\div 2$, $\div 4$, etc., from a maximum of 160 MHz. This limits the OSR values to explore and force to expand the bandwidth in UMTS from 3.84 to 4 MHz.
- The smallest unit capacitor is fixed to 0.25 pF for mismatching issues.
- The sampling capacitor at the modulator front-end can only take values that are multiple of the unit capacitor.

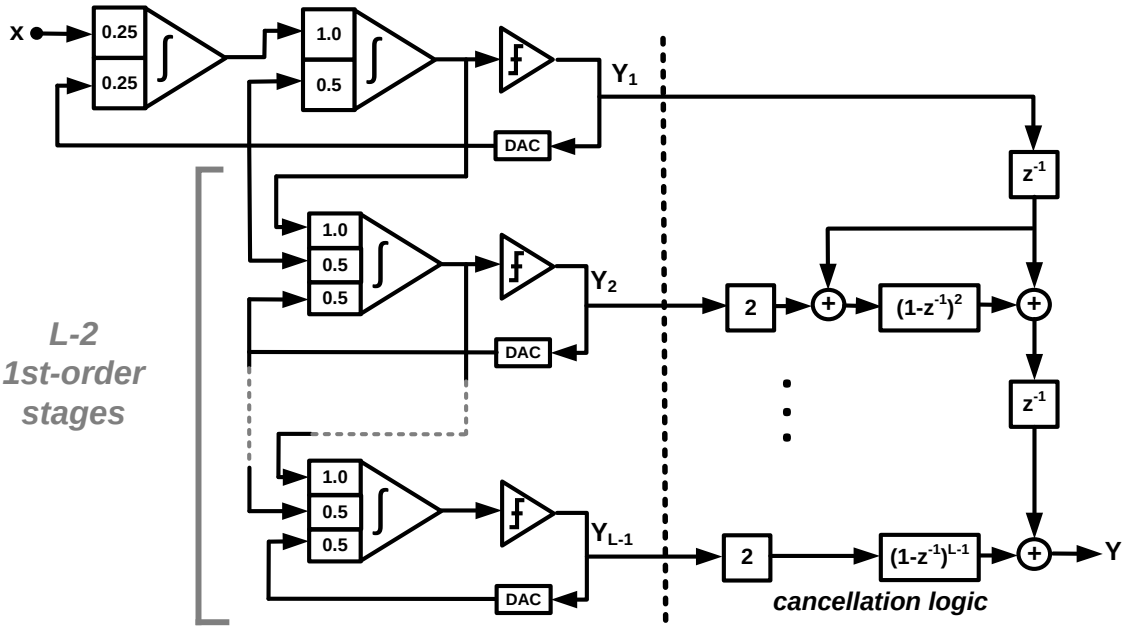


Figure 6.8: Expandable cascade ΣΔ modulator.

During this first exploration, the power consumption is estimated using the analytical procedure described in [78]. The procedure, based on compact expressions that contemplate both architectural and technological features, schematically consists of the following steps:

- The in-band quantization error power (P_Q) is calculated for given values of $\{L, B, OSR\}$ and V_{ref}. Noise leakages due to capacitor mismatch, finite amplifier DC-Gain, and errors in the multi-bit quantizer (if $B > 1$) are also contemplated.

- The in-band error power due to circuit noise (P_{CN}) is considered. The value of the sampling capacitor at the modulator front-end (C_S) is selected so that $P_Q + P_{CN}$ is smaller than the maximum allowed total in-band error. P_{CN} will be mainly contributed by kT/C noise, but some room is left at this step for the contribution of the front-end amplifier noise.

- The amplifier gain-bandwidth product (GB) is estimated so that the in-band error power due to the integrator defective settling (P_{st}) is non-limiting ($P_{st} << P_Q + P_{CN}$). A linear settling model is used, considering that it takes a number $\ln\left(2^{ENOB}\right)$ of time constants to settle within $ENOB$ resolution.

- The amplifier GB is related to its power consumption, for which the amplifier topology must be known a priori. Suitable candidates are closely related to the process technology and its supply voltage, minimal device length, etc. Typical choice is folded-cascode for supplies above $3V$ or two-stage amplifiers below 2.5 V. In this case, thus, the folded-cascode topology will be considered.

- Once the power dissipation of the front-end integrator has been estimated, that of the remaining ones (with less demanding specifications) is considered to be a fraction of it. The overall modulator power is then obtained by adding up all contributions, together with the dynamic power in the SC stages.

The candidates considered for each standard, sorted in increasing power consumption, are shown in Table 6.2. The required values of the sampling frequency (f_s) and the sampling capacitors (C_s), as well as the obtained values of the Dynamic Range (DRs) and Signal-to-Noise ratio ($SNDRs$), are also shown. Highlighted rows are those candidates selected for further consideration. Note that the rest of candidates can be obtained by simply increasing the L or B values of the selected candidates.

Once a set of candidates is considered for each standard, the next step of the design methodology is the selection of the best combination of these candidates. For this, a mm-PoF will be generated for each of the selected combination. The next section focuses on this, beginning with the selection of the best amplifier topology for this application.

6.3 GENERATION OF THE MM-POF FOR EACH COMBINATION OF CANDIDATES

The required amplifiers for the generation of the mm-PoF of each combination of $\{L, B, OSR\}$ candidates are obtained from lower-level mm-PoFs of reconfigurable amplifiers. Although in practical cases it is assumed that a library of PoFs of the most basic building blocks is available, each for a different load, this is not the case in this illustrative example. For this reason, a set of mm-PoFs of amplifiers will be generated for a different loading conditions, since each $\{L, B, OSR\}$ candidate imposes a different load to the integrators.

During the generation of the mm-PoF at the modulator level, the performances of the reconfigurable amplifiers of the low-level mm-PoFs are transformed to the conditions estimated at the modulator level. This transformation is done using the technique described in section 4.1.1 of Chapter 4. Before moving on to the details about the generation of mm-PoFs of the modulator, let us explain the generation of the mm-PoFs of amplifiers.

Table 6.2: {L,B,OSR} candidates for each standard sorted in increasing power consumption

Std	L	B	OSR	f_s[MHz]	C_s[pF]	DR [bits]	$SNDR_{peak}$[bit]	Power [mW]
GSM	4	1	50	20	0.50	14.42	13.59	10.9
	3	2	50	20	0.50	14.39	13.56	11.7
	3	3	50	20	0.50	14.41	13.58	12.5
	4	2	50	20	0.50	14.42	13.59	13.4
	3	4	50	20	0.50	14.41	13.58	14.1
	4	3	50	20	0.50	14.42	13.59	14.2
	4	4	50	20	0.50	14.42	13.59	15.8
	3	1	100	40	0.25	14.42	13.59	17.0
	4	1	100	40	0.25	14.42	13.59	20.0
BT	4	1	20	40	0.25	12.82	11.99	18.1
	3	3	20	40	0.25	12.76	11.93	20.6
	3	4	20	40	0.25	13.05	12.22	22.5
	4	2	20	40	0.25	13.16	12.33	23.0
	4	3	20	40	0.25	13.21	12.38	23.9
	4	4	20	40	0.25	13.22	12.39	25.5
	3	1	40	80	0.25	13.40	12.57	32.1
UMTS	3	4	10	80	0.25	10.81	9.98	37.3
	4	2	10	80	0.25	10.45	9.62	38.6
	4	3	10	80	0.25	11.46	10.63	42.0

6.3.1 *Generation of the mm-PoFs of Reconfigurable Amplifiers*

The mm-PoFs of amplifiers will be generated for 4 operation modes. The topology selected for the synthesis of the amplifiers used in the ΣΔ modulator is the folded-cascode shown in Fig.6.9. Although the DC-gains achievable with this topology are not too high, it offers enough bandwidths for the high speed specifications required for the UMTS standard.

Also shown in Fig.6.9, the chromosome of the amplifier indicates the design variables that will be used for the generation of the mm-PoF. These are the widths and lengths of some transistors and the bias current, which will be changed for each operation mode as detailed in the figure. The rest of parameters of the circuit that are not specified in the chromosome are defined as functions of the design variables. This is detailed in Table 6.3, where expression 1 ensures that transistors M_{10} and M_{11} still operate in saturation region for unbalanced operation of the input differential pair:

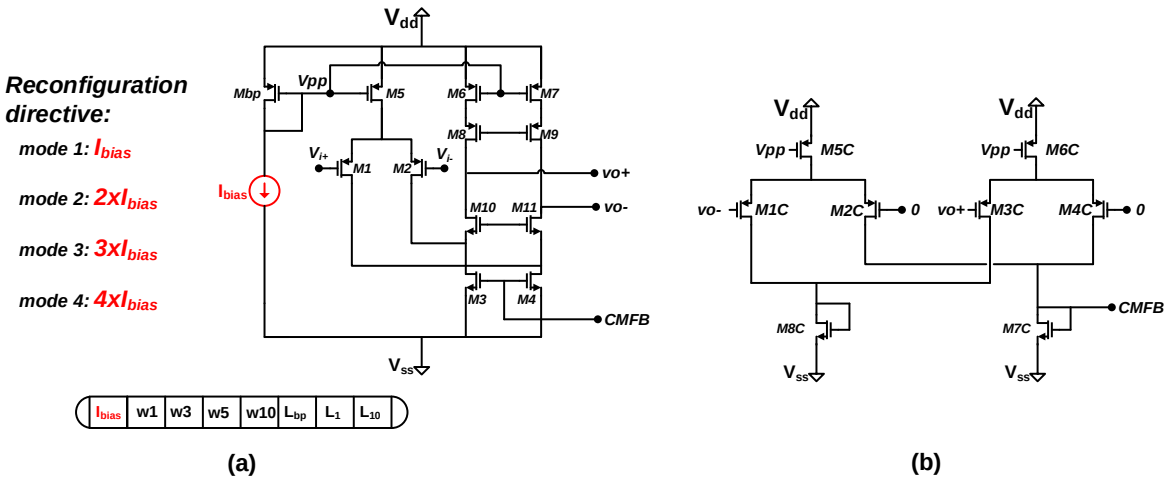


Figure 6.9: Folded-cascode amplifier. (a) Core. (b) Common-mode feedback circuit.

$$I_6 > I_{bias}/2 \rightarrow I_6 = (0.5 + \kappa) \cdot I_{bias} \tag{6.9}$$

where $\kappa \cdot I_{bias}$ is the minimum current flowing through M_{10} and M_{11} to ensure saturation operation. Typically $\kappa = 0.1$, so that $I_6 = 0.6 \cdot I_{bias}$. This relationship between currents translates directly into a relationship between the width of the transistors:

$$\frac{I_{bias}}{w_5} = \frac{I_6}{w_6} \implies w_6 = \frac{I_6}{I_{bias}} \cdot w_5 = 0.6 \cdot w_5 \tag{6.10}$$

Design objectives and constraints that must be fulfilled by the amplifiers for the four operation modes are detailed in Table 6.4. As it can be seen, they are the same used in the experiments described in the previous chapters

As explained above, several mm-PoFs of amplifiers will be generated, each one for different loading conditions. 7 different loads are considered: 1, 3.5, 5, 7.5, 10, 12.5 and 15 pF. Only capacitive loads are considered, since no resistive load is seen by the integrators. These values have been chosen taking into account the range covered by the different loads the amplifiers will see in the modulator in each operation mode. Once again, as in Chapter 5, it is important to note that in practical cases this will not be necessary, since the presented methodology assumes the existence of a library of PoFs of the most basic basic building blocks, generated for a varied range of loading conditions, actually quite similar to those proposed above.

Table 6.3: Relationships between design variables.

Variable	Range	Dependent variable	Relation	Why?
w_1	1 - 800 μm	w_2, w_{1c}, w_{2c}, w_{3c}, w_{4c}	=	symmetry
w_3	1 - 800 μm	w_4, w_{7c}, w_{8c}	=	symmetry
w_5	1 - 800 μm	w_6, w_7, w_8, w_9	$0.6 \cdot w_5$	Expression 1
		w_{5c}, w_{6c}	=	symmetry
w_{10}	1 - 800 μm	w_{11}	=	symmetry
l_{bp}	130 - 400 nm	l_3, l_4, l_5, l_6, l_{5c} l_7, l_8, l_9, l_{6c}, l_{7c}, l_{8c}	=	symmetry
l_1	130 - 400 nm	l_2, l_{1c}, l_{2c}, l_{3c}, l_{4c}	=	symmetry
l_{10}	130 - 400 nm	l_{11}	=	symmetry
I_{bias}	1 - 1000 μA	-	-	- height

Table 6.4: Design Objectives and Constraints.

Design Objectives	Treatment
DC-Gain	maximize
unity-gain frequency (fu)	maximize
power	minimize
area	minimize
Constraint	**Values**
Phase Margin (PM)	$60^\circ \leq PM \leq 90^\circ$
Output Swing (OS)	$\geq$ 3.6 V
Slew-rate	$\geq 50\ V/\mu s$
dm (for each transistor)	≥ 1.1

6.3.2 *System-level Optimization*

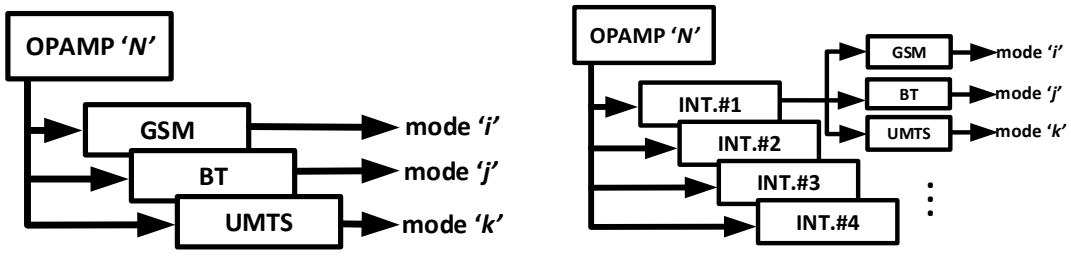
For the generation of the mm-PoF of each combination of $\{L, B, OSR\}$ candidates, a directive must be defined to select the amplifiers from the low-level mm-PoFs that will be used to implement the integrators of the modulator. In [79] the used strategy consists in using the same amplifier for all integrators with the only difference being a larger differential input pair for the second and third amplifiers. Besides, the bias current of each amplifier is adapted from one standard to another, varying from 16 to 80 μA. In this work, several cases are considered. They are depicted in Figures 6.10 and 6.11 and are detailed in the following lines.

1. **Directive 1**, Fig.6.10a, uses the same amplifier for all integrators. For each mode of the modulator, all amplifiers will use the same operation mode, but this mode can vary from one standard to another. The modes can take any of the 4 possible values for which the mm-PoF of amplifiers has been generated, for instance, operation mode 1 of the amplifier for GSM, operation mode 2 for BT and operation mode 4 for UMTS.

2. **Directive 2**, Fig.6.10b, uses the same amplifier for all integrators. The operation modes of the amplifiers for each mode of the modulator are chosen independently. For instance, modes 1, 3 and 4 of the amplifier for GSM, BT and UMTS, respectively, in the first integrator; modes 2, 3 and 4 of the amplifier for GSM, BT and UMTS, respectively, in the second integrator and so on.

3. **Directive 3**, Fig.6.11, uses a different amplifier for each integrator. The operation mode of each amplifier and of each integrator for each mode of the modulator are chosen independently. For example, integrator 1 using amplifier N in modes 2, 2 and 4 for GSM, BT and UMTS, respectively.

Each reconfiguration directive requires a different number of design variables to explore the low-level mm-PoFs of amplifiers. Reconfiguration directive 1 requires 6 design variables: 3 to select the amplifier from the low-level mm-PoF (because the mm-PoFs have been generated for 4 design objectives) and 3 more to select the operation mode of the amplifier that is used in each mode of the modulator. Reconfiguration directive 2 requires 11 design variables: 3 to select the amplifier; 3 for integrators 1, 2 and 3, that decide which mode of the amplifier is used in each integrator for each mode of the modulator; and 2 for integrator 4 since this is used only for BT and UMTS standards. Finally, reconfiguration directive 3 requires 23 design variables: 12 to select the amplifier used for each integrator and 11 more to choose the modes of the amplifiers used for each mode of the modulator.



(a) (b)

Figure 6.10: Reconfiguration directives (a) 1 and (b) 2.

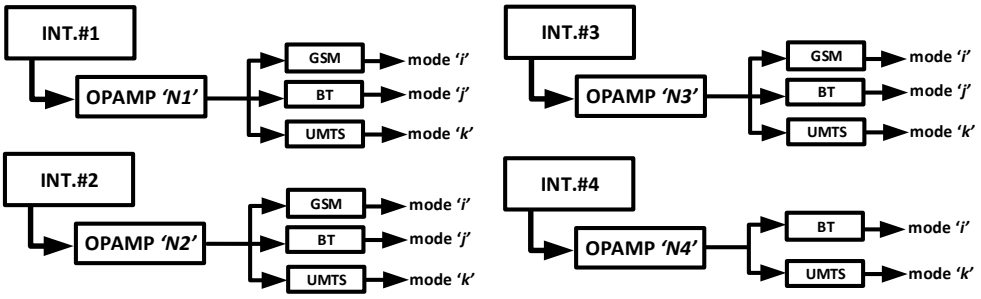


Figure 6.11: Reconfiguration directive 3.

The optimization method used for these experiments is based on the use of the new Multi-mode Multi-objective Evolutionary Algorithm (the optimizer) coupled to a MATLAB Simulink®-based simulator (the evaluator). More specifically, the evaluator that has been used is SIMSIDES [80], a high-level Simulink-based synthesis tool for ΣΔ modulators. The procedure is depicted in Fig.6.12. The optimizer evolves a population of multi-mode modulator designs using SIMSIDES to evaluate the performance characteristics of each design. For this, the parameters that characterize each design are used in the Simulink® model of the modulator. These parameters, which constitute the chromosome of each design, are the performances of the amplifiers that are used to implement the modulator integrators.

An example of a Simulink® model used to evaluate the performances of the modulator is depicted in Fig.6.13. The figure corresponds to a fourth-order modulator with multi-bit quantizer in the last stage. The chromosome, formed by 6 design variables for each integrator, is also shown in the figure. Three of these variables are used to select the amplifier that will be used to implement that integrator. The method to explore the low-level mm-PoFs of amplifiers will be

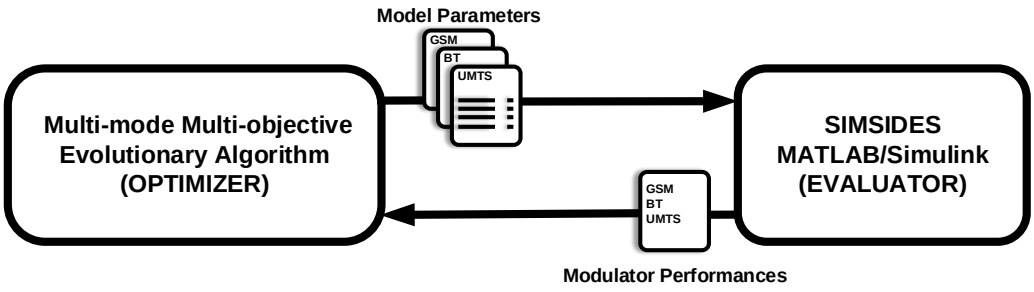


Figure 6.12: Optimization procedure for the generation of the mm-PoF of the ΣΔ modulator.

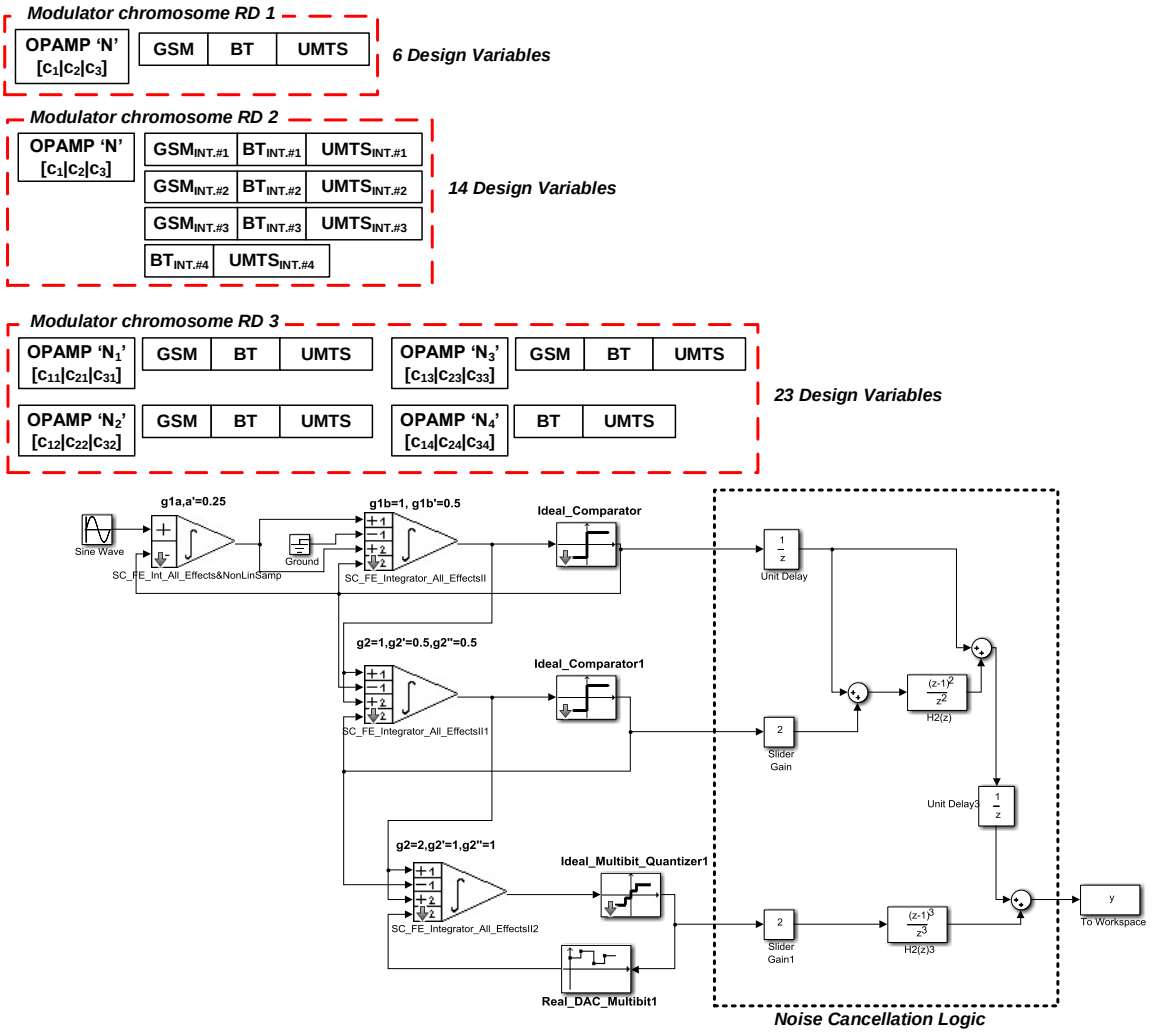


Figure 6.13: Simulink® model of the ΣΔ modulator.

the Index-mapping method described in 4.2.2. As the mm-PoFs of amplifiers are generated for 4 design objectives, only 3 coordinates are necessary to explore those fronts. The last three variables of the modulator chromosome are used to select the operation mode of that amplifier that will be used for each operation mode of the modulator. These are simple integer variables that can take any value between 1 and 4. In the case of modulator order 3, only three integrators are used and thus the number of design variables is also reduced.

As explained above, the parameters used for the implementation of the modulator integrators in the Simulink® model are obtained from the low-level mm-PoFs of amplifiers. The process where the necessary information for the

evaluation of each design is obtained is shown in Fig.6.14. This process is detailed in the following lines.

1. First, the chromosome of the individual determines the amplifier that will be used for each integrator of the modulator, as well as the operation mode.
2. The performances of the selected amplifier are transformed to the loading conditions of the integrator.
3. The new performances are written in the data file that will contain all the information necessary for the simulation of the model.
4. The model is simulated using SIMSIDES and the performances of the modulator (power consumption of each mode, area occupation, standards requirements, etc.) are included in the chromosome of the individual.

The design objectives of the optimization will be the area and the power consumption of each operation mode. As constraints, it will be imposed that the modulator provides a valid resolution when operating under each of the standard specifications. Table 6.5 summarizes the characteristics of the optimization.

Table 6.5: Design Objectives and Constraints for the Optimization of the ΣΔ Modulator.

	Name	**Treatment**
Design Objectives	area	minimize
	power	minimize
Constraints	Resolution GSM	$\geq$ 13 bits
	Resolution BT	$\geq$ 11 bits
	Resolution UMTS	$\geq$ 9 bits

The area of the modulator will be estimated as the sum of the area of all integrators, that is, the area of the amplifiers, which is directly obtained from the low-level mm-PoFs, the area of the capacitor arrays used to implement the integrators weights and an estimation of the area of the rest of the blocks (comparators and multi-bit quantizers). The power consumption will be estimated as the sum of the power of the amplifiers, which is also obtained from the low-level mm-PoFs, and the power dissipated in the comparators, in the last stage multi-bit DAC and in the SC stages. More details about the estimation of the area and the power consumption are given in the next section. The resolution of the modulator, on the other hand, is obtained by evaluating the Simulink® model of the modulator, using for this the real performances of the amplifiers from the low-level mm-PoF of amplifiers. As explained above , the performances of the amplifiers must be

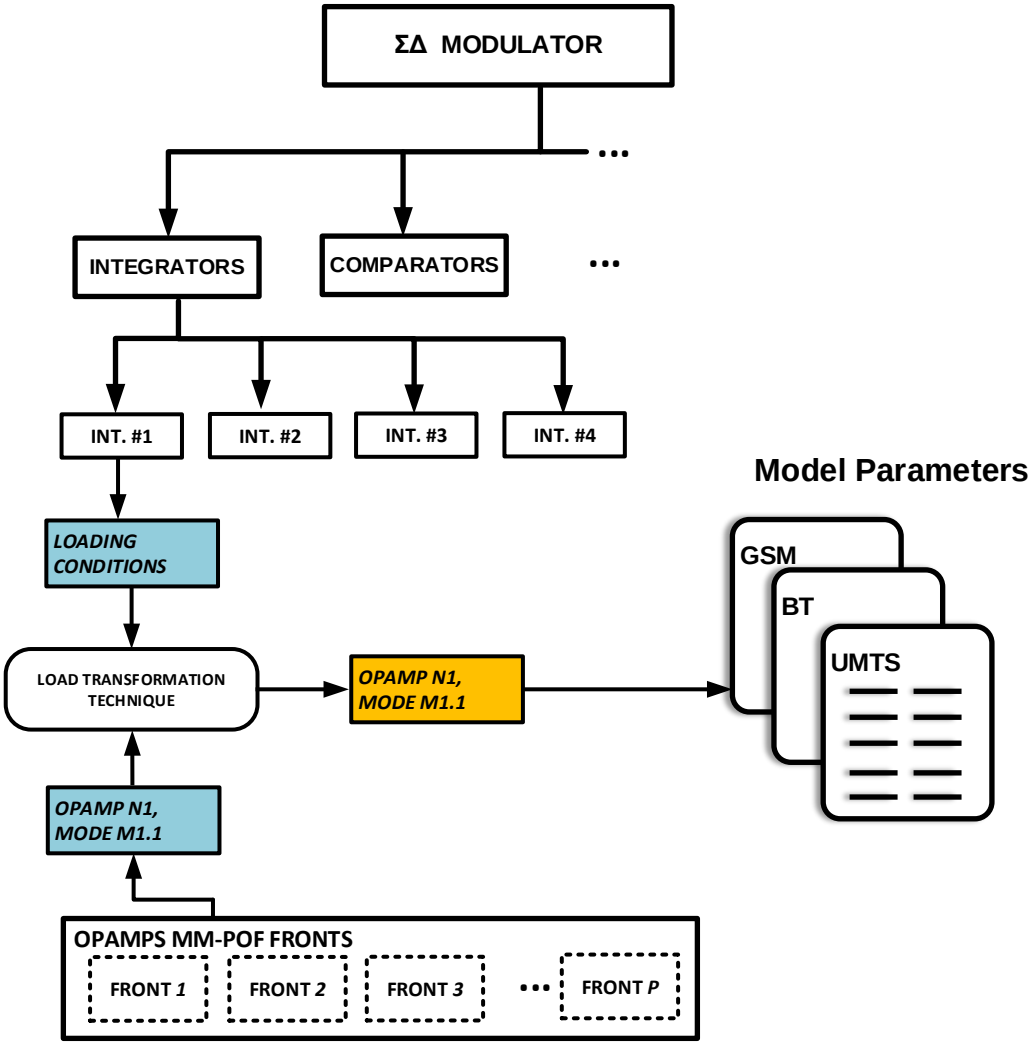


Figure 6.14: Generation of the information required for the simulation of each individual.

transformed to the equivalent load of the integrators. The estimation of this equivalent load is also detailed in the next section.

6.4 AREA, POWER CONSUMPTION AND LOAD ESTIMATIONS

6.4.1 *Area Estimation*

The area occupation will be estimated as the sum of the area of the integrators, including the area of the amplifiers and that of the capacitor arrays, plus the area of the switches, the area of the comparators and the multi-bit quantizers of the last

stages. The area of the amplifiers does not need to be estimated as it is obtained directly from the low-level mm-PoFs.

Capacitors

The area of the capacitors used in the switched-capacitor integrators of the ΣΔ modulator are estimated taking into account the structures depicted in Fig.6.15, which are used to implement the integrator weights. Note that only the first integrator uses a commonly centroid design because the matching of the remaining weights is based only on closely-placed unit capacitors. The integrator weights are implemented by means of capacitor ratios. If a weight, g_i, is implemented as:

$$g_i = \frac{m_i C_u}{n_i C_u} \tag{6.11}$$

, where C_u is the unit capacitor, , this means that, for instance, the weight of the first integrator of the modulator, which is 0.25, must be implemented using $m_1 = 1$ and $n_1 = 4$. Taking this into account and adding the necessary dummy capacitors, it can be concluded that 2×57 unit capacitors are necessary to implement the integrator weights when the order of the modulator is 3, or 2×73 when the order of the modulator is 4. The smallest value of the unit capacitor is fixed to $0.25 - pF$ for mismatching issues. Its area is approximately of $21.5\mu m \times 17.5\mu m$. This value has been estimated considering a metal-insulator-metal (MiM) implementation, which exhibits a good matching and very small bottom-plate parasitics.

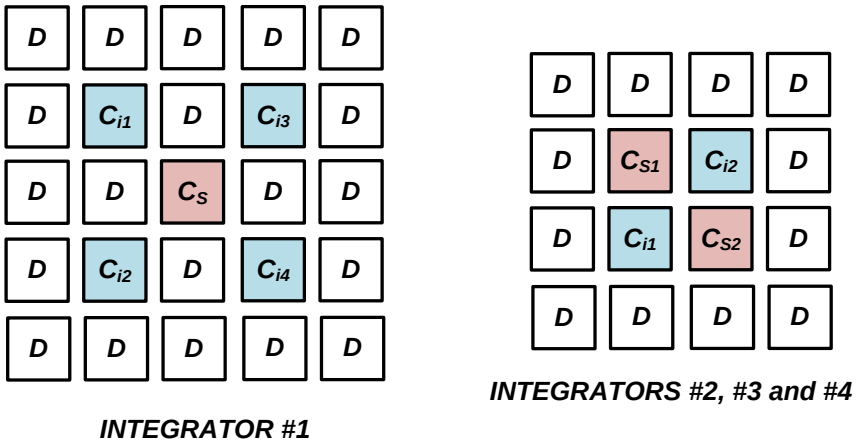


Figure 6.15: Capacitor arrays used to implement the integrator weights in the ΣΔ modulator.

Comparators

The area of the comparators in the single-bit modulator stages will be estimated considering the latched topology shown in Fig.6.16. It includes a pre-amplifying stage to attenuate the impact of common-mode interferences on the comparator and of kick-back noise on the integrator. Considering this topology in 130-nm CMOS technology and the results reported in [81], where the same topology is used, a value of $3.5 \cdot 10^3 \mu m^2$ is a good estimation.

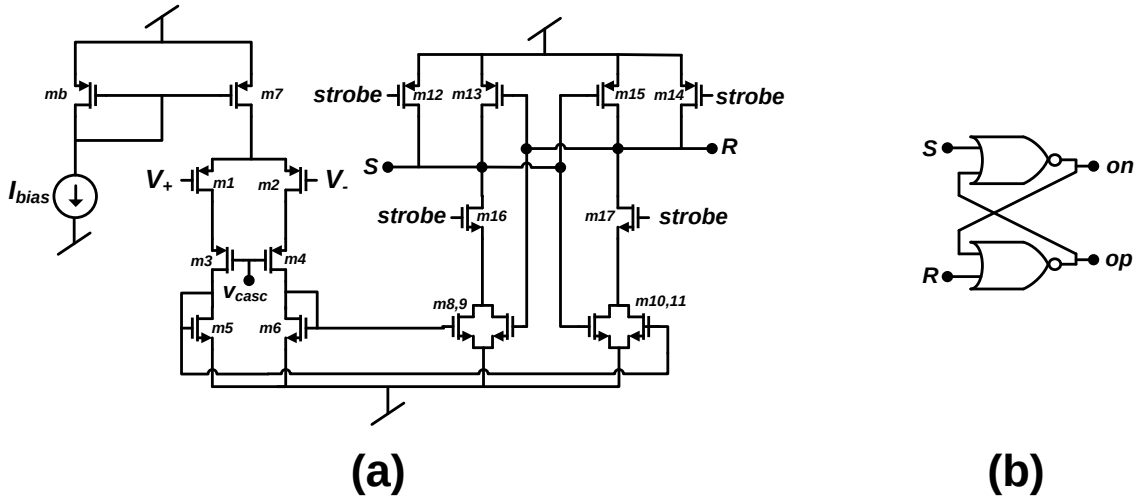


Figure 6.16: Comparator: (a) Pre-amplifying stage and regenerative latch, (b) SR latch.

Multi-bit Quantizer

The area of the multi-bit quantizer will be estimated considering an implementation with a flash quantizer and a resistor-ladder DAC. The used topology is depicted in Fig.6.17 for the case of a 2-bit quantizer. The comparators in the quantizer are similar to those described above but with an extra differential pair at the pre-amplifying stage in order to operate with fully-differential inputs. Therefore, the total area of the comparators and the last-stage quantizer can be estimated in terms of the order of the modulator and the number of bits of the last-stage quantizer as:

$$A_{total} = A_{comparator} \times \left[(L-1) + \left(2^B - 1 \right) \right] \tag{6.12}$$

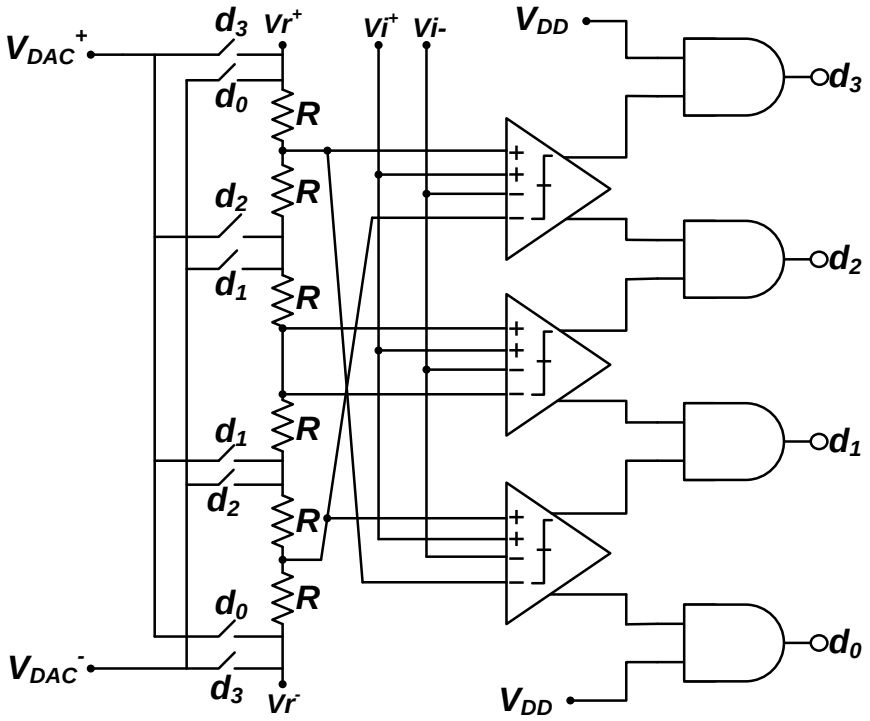


Figure 6.17: 2-bit quantizer used in the last stage of the modulator.

Switches

The area of the switches is estimated assuming a CMOS implementation. The area of the transistors can be estimated as:

$$A_{switch} = N_{switches} \times L_{min} \left(\omega_n + \omega_p\right) \tag{6.13}$$

where

$$\omega_n = \frac{L_{min}}{2R_{on}K_n\left(\frac{V_{DD}}{2} - V_{TN}\right)}, \omega_p = \frac{L_{min}}{2R_{on}K_p\left(\frac{V_{DD}}{2} - |V_{TP}|\right)}$$

The maximum acceptable value of the on resistance is estimated imposing that the pole it originates is at least at one decade higher than the pole of the amplifier of the integrator [82]:

$$R_{on,MAX} = \frac{1}{10 \cdot 2C_s \cdot GB} \tag{6.14}$$

6.4.2 *Power Estimation*

The power consumption of the cascade ΣΔ modulator can be estimated as:

$$Power \cong P_{op,sta} + P_{DAC} + \left[(L-1) + \left(2^B - 1\right)\right] P_{comp} + P_{SC} \tag{6.15}$$

where $P_{op,sta}$ is the power dissipated in the amplifiers; P_{DAC} is the power dissipated in the last-stage multi-bit DAC (in case $B > 1$); P_{comp} denotes the power dissipated in the comparators; and P_{SC} is the dynamic power dissipated in SC stages. The power dissipated in the amplifiers ($P_{op,sta}$) does not need to be estimated as we can use the real values stored in the low-level mm-PoFs of amplifiers. As in the case of the loads estimation, this allows a much more accurate estimation of the overall power consumption of the modulator. The estimation of the rest of contributions is detailed in the following lines.

Multi-bit DAC

Due to its relaxed requirements, the last-stage multi-bit DAC will be implemented with a resistor ladder. Its main design consideration, besides resistor matching and linearity, is the settling error. Assuming a tolerance of 1/2 LSB, according to [83] we can write:

$$P_{DAC} \cong \frac{V_{ref}}{2} \pi \left(2^B - 1\right) \cdot f_s \cdot C_{par} \tag{6.16}$$

where C_{par} is the input parasitic capacitance of the comparator and, in a 130-nm CMOS technology, a good estimation is 0.056 pF.

Comparators

The power dissipated in the comparators enclose the power dissipated in the $L-1$ latched comparators used as single-bit quantizers and those in the last-stage multi-bit quantizer, that is, $\left(2^B - 1\right)$ more latches. Thus, according to [84], the total power dissipated in the comparators can be estimated as:

$$P_{comp_total} \cong \left[(L-1) + \left(2^B - 1\right)\right] \cdot K_{comp} \cdot I_{max,comp} \cdot V_{ref} \tag{6.17}$$

where K_{comp} depends on the topology of the pre-amplifier of the comparator and which can be approximated as 1; and $I_{max,comp}$ is the maximum output current driven by the comparator, which can be approximated to $10mA$ for the technology considered here.

Switches

The power dissipated in the SC stages can be estimated as a multiple of the power dissipated by switching a capacitance C_u between the reference voltages at a frequency f_s:

$$P_{SC}^{u} = C_u f_s V_{ref}^2. \tag{6.18}$$

The final value depends on the integrator weights and in our case a good estimation is provided by the following expression:

$$P_{SC} = 2\left[5C_{u1} + 4\left(L-1\right)C_{u2}\right] f_s V_{ref}^2 \tag{6.19}$$

where the factor 2 comes from the differential implementation; C_{u1} is the unit capacitor used in the first integrator and C_{u2} is the one used in the rest of integrators, usually smaller than C_{u1}.

6.4.3 *Load Estimation*

In order to evaluate the performances of the amplifiers, their characteristics must be transformed to the new loading conditions. The equivalent loads for the amplifiers in the integrators can be estimated considering the generic scheme in Fig.6.18, which shows the configuration of the integrator at the begining of the integration phase. By applying basic circuit theory, the equivalent capacitive load at the amplifier output node during the integration phase can be obtained as [82]:

$$C_{eq} \cong C_S + C_P + C_L\left(1 + \frac{C_S + C_P}{C_I}\right) \tag{6.20}$$

In equation 6.20, C_I is the integrator feedback capacitance and it is related to C_S through the integrator weight ($C_I = C_S/g_i$); and C_P and C_L are the integrator summing node and output node parasitics, respectively. Estimating the latter two capacitances is a difficult task because of their extreme dependence on the actual amplifier design. However, since in this case real amplifiers that have been already designed are used in the optimization of the modulator, we can use the real values of these capacitances which allows much more accurate estimations.

6.5 EXPERIMENTAL RESULTS

The combinations that have been selected are shown in Table 6.6. For each one of them, the mm-PoF have been generated using the 3 reconfiguration directives that have been described previously.

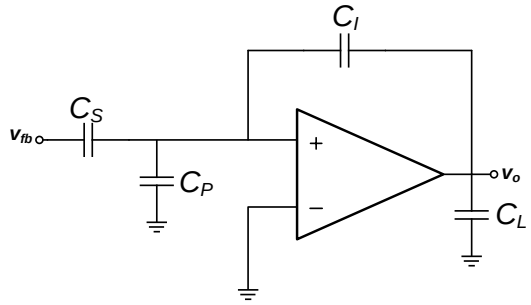


Figure 6.18: SC integrator at integration phase.

Table 6.6: Selected Combinations.

COMBINATION	GSM Candidate	Bluetooth Candidate	UMTS Candidate
1	$\{4,1,50\}$	$\{4,1,20\}$	$\{3,4,10\}$
2	$\{4,1,50\}$	$\{4,1,20\}$	$\{4,2,10\}$
3	$\{4,1,50\}$	$\{3,3,20\}$	$\{3,4,10\}$
4	$\{4,1,50\}$	$\{3,3,20\}$	$\{4,2,10\}$
5	$\{3,2,50\}$	$\{4,1,20\}$	$\{3,4,10\}$
6	$\{3,2,50\}$	$\{4,1,20\}$	$\{4,2,10\}$
7	$\{3,2,50\}$	$\{3,3,20\}$	$\{3,4,10\}$
8	$\{3,2,50\}$	$\{3,3,20\}$	$\{4,2,10\}$
9	$\{3,1,100\}$	$\{4,1,20\}$	$\{3,4,10\}$
10	$\{3,1,100\}$	$\{4,1,20\}$	$\{4,2,10\}$
11	$\{3,1,100\}$	$\{3,3,20\}$	$\{3,4,10\}$
12	$\{3,1,100\}$	$\{3,3,20\}$	$\{4,2,10\}$

The mm-PoFs obtained for each combination and for each reconfiguration directive are shown in Figures 6.19, 6.20 and 6.21. Note that, in the three figures, each point represents a reconfigurable modulator, but instead of displaying the power consumption of each operation mode, only the average power consumption among the modes is shown. Since the area is the same for all operation modes, each reconfigurable modulator is represented by a single point. This is done to improve the visualization of the results. As it can be seen, in all three reconfiguration directives, combinations 2 and 10 get the best results in terms of the trade-off between area and power consumption. This is due, in part, to the higher area

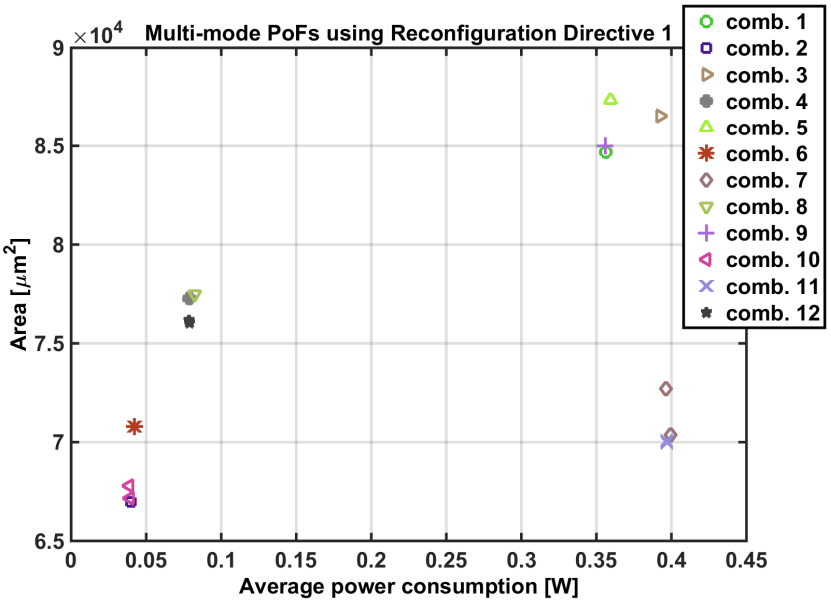


Figure 6.19: Average power consumption and area of the combinations of $\{L, B, OSR\}$ selected candidates obtained using reconfiguration directive 1.

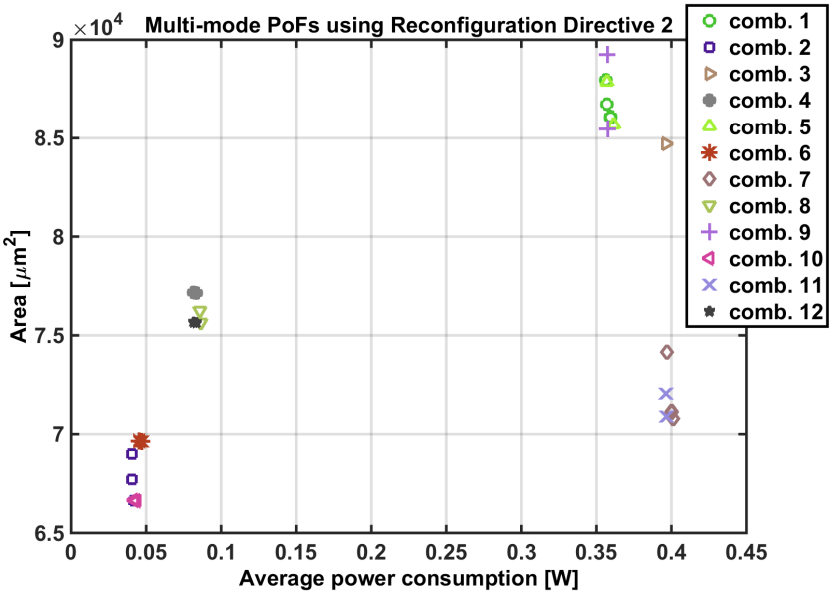


Figure 6.20: Average power consumption and area of the combinations of $\{L, B, OSR\}$ selected candidates using reconfiguration directive 2.

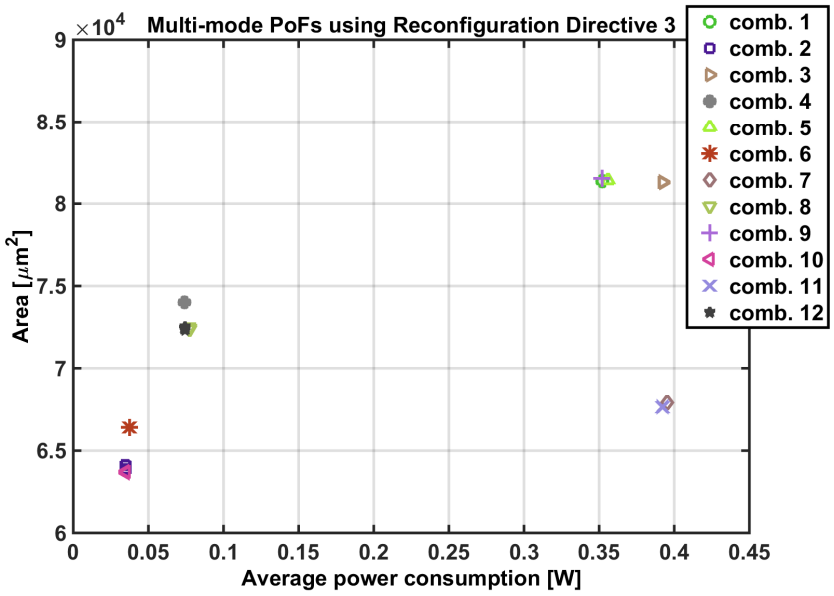


Figure 6.21: Average power consumption and area of the combinations of $\{L, B, OSR\}$ selected candidates using reconfiguration directive 3.

that is required when using multi-bit quantizers of more than 2 bits. Combination 2 corresponds to $\{4, 1, 50\}$ for GSM, $\{4, 1, 20\}$ for Bluetooth and $\{4, 2, 10\}$ for UMTS, while combination 10 corresponds to $\{3, 1, 100\}$ for GSM, $\{4, 1, 20\}$ for Bluetooth and $\{4, 2, 10\}$ for UMTS. These solutions comprise third and fourth order modulators and single or 2-bit quantizers at the last stage.

Combinations 2 and 10 are shown alone for the different reconfiguration directives in Fig.6.22. As it can be seen, the optimizations that make use of reconfiguration directive 3 get the best results by far in terms of the area and power consumption trade-off. This directive lets the optimizer to use different amplifiers for each integrator, and using a different operation mode of the amplifier for each operation mode of the modulator. In other words, this directive allows the optimizer to choose over a much more diverse number of combinations of amplifiers and operation modes and, therefore, is able to find more and much better solutions than the other more restrictive directives.

Let us consider two different designs from the mm-PoFs corresponding to reconfiguration directive 3, one from combination 2 (design 1) and another from combination 10 (design 2). These mm-PoFs are shown in Fig.6.23, where the two selected designs are enclosed in circles. The performances of these designs are shown in Table 6.7. As it can be seen, both designs fulfill the resolution specification for each standard. Their power consumption can be switched between around 10

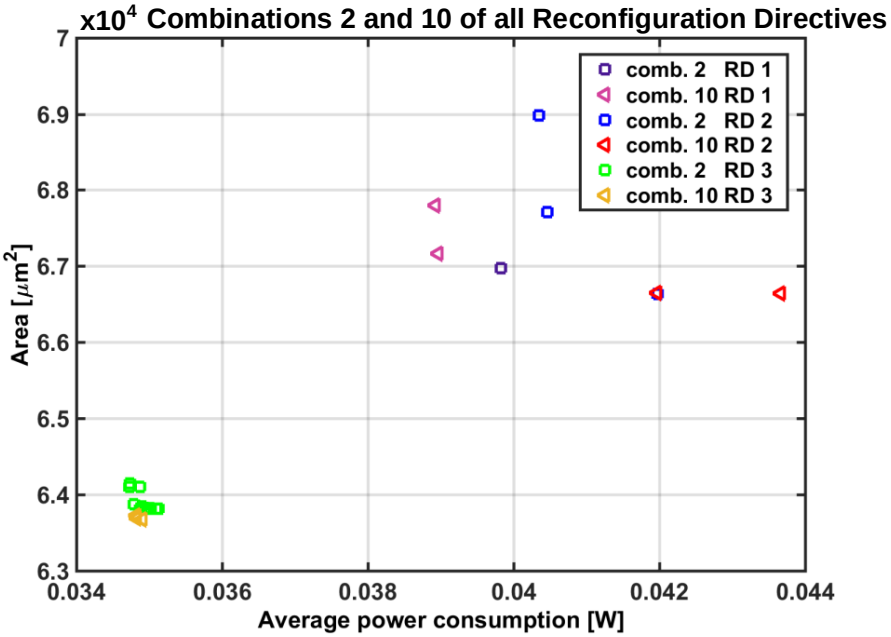


Figure 6.22: Average power consumption and area of combinations 2 and 10.

mW for GSM mode and more than 80 mW for UMTS. Although the area of the two solutions is similar, their power consumption is slightly different in some operation modes. Design 1 has a lower power consumption in GSM and UMTS modes, but for Bluetooth mode design 2 gets a better value.

Table 6.7: Final Design Performances.

	Design 1			**Design** 2		
	GSM	**BT**	**UMTS**	**GSM**	**BT**	**UMTS**
Architecture	2-1-1	2-1-1	2-1-1(2bits)	2-1	2-1-1	2-1-1(2bits)
Oversampling Ratio	50	20	10	100	20	10
f_s**[MHz]**	20	40	80	40	40	80
$SNDR_{peak}$**[dB]**	83.43	79.71	61.21	89.24	74.50	57.08
power [mW]	9.90	14.20	80.30	10.30	13.20	81.00
area $[10^3 \mu m^2]$	63.88			63.70		

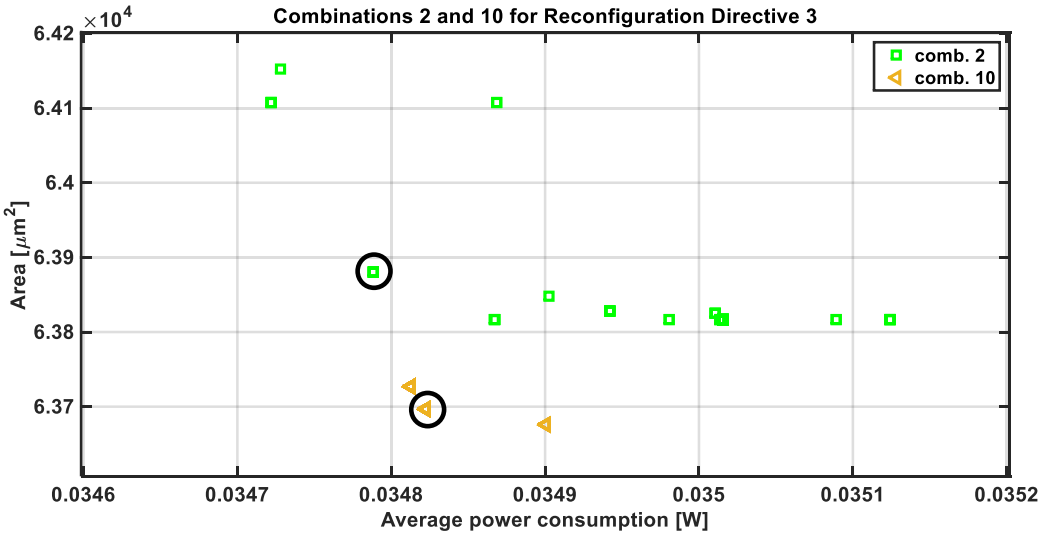
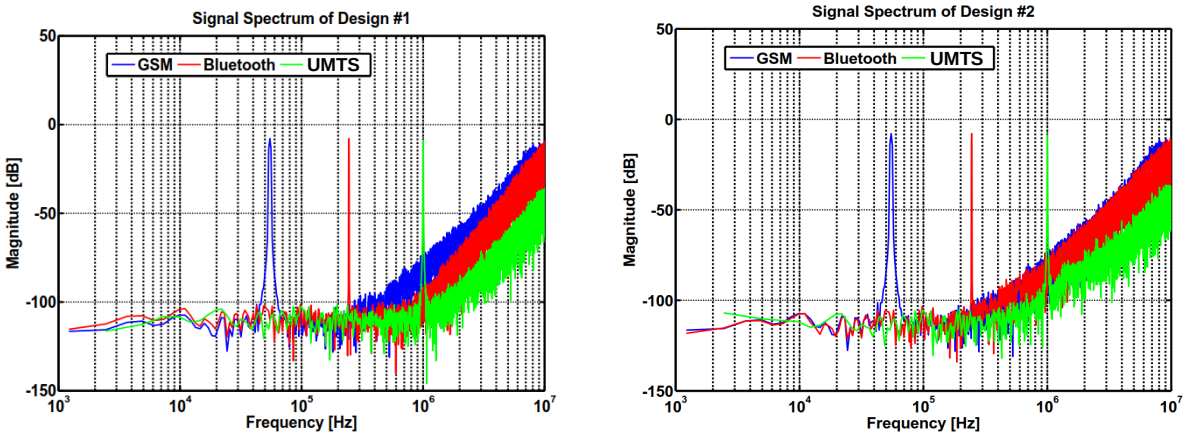


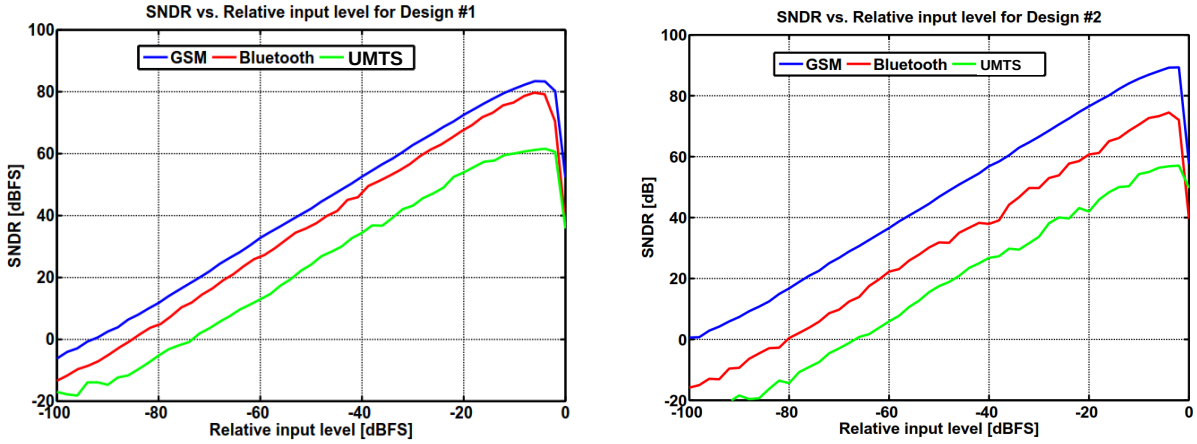
Figure 6.23: Average power consumption and area of combination 2 obtained with reconfiguration directive 3.

The output spectra and the SNDR curves of both designs for each standard are shown in Figures 6.24 and 6.25. As it can be seen, both solutions show a good performance in the bands of interest.



(a) (b)

Figure 6.24: Output spectrum of (a) design 1 and (b) design 2.



(a) (b)

Figure 6.25: SNDR curve of (a) design 1 and (b) design 2.

Although it has already been explained, it is important to note here that the amplifiers used to implement the integrators of the two selected modulators are fully-sized designs. Their performance characteristics are shown in Tables 6.8 and 6.9. Each integrator is implemented using the same amplifier, which can use a different operation mode for each mode of the modulator. For example, integrator 1 of design 1 uses one operation mode of the amplifier for GSM and Bluetooth standards, and another mode for UMTS standard. Note that design 2 uses a 2-1 architecture in GSM mode and, thus, the fourth integrator is used only for the Bluetooth and UMTS standards.

Table 6.8: Performances of the Amplifiers used for Design 1.

	INT. 1		**INT. 2**		**INT. 3**		**INT. 4**	
	GSM/BT	**UMTS**	**GSM**	**BT/UMTS**	**GSM/UMTS**	**BT**	**GSM/UMTS**	**BT**
DC-Gain [dB]	70.98	69.77	53.42	51.61	65.91	65.91	68.87	68.16
GBW [MHz]	57.04	163.66	218.81	230.86	96.06	70.79	108.48	122.90
Phase margin [º]	78.85	76.43	79.54	80.92	73.53	77.85	78.66	80.55
Slew-rate [V/μs]	45.51	159.30	229.93	255.48	87.88	55.98	89.72	99.03
Eq. Load [pF]	0.33	0.34	0.25	0.25	0.57	0.57	0.17	0.17
OSW [V]	1.84	1.57	1.45	1.34	1.82	1.82	1.70	1.58
Eq. input noise [nV/$Hz^{1/2}$]	18.27	14.44	14.57	12.05	15.27	6.82	20.16	15.78
Bias current [μA]	60.53	181.60	183.94	245.26	175.77	703.07	104.97	157.46
Power [mW]	0.32	0.93	0.78	0.98	0.92	0.92	0.55	0.81

Table 6.9: Performances of the Amplifiers used for Design 2.

	INT. 1		**INT.** 2		**INT.** 3			**INT.** 4	
	GSM/BT	**UMTS**	**GSM**	**BT/UMTS**	**GSM**	**BT**	**UMTS**	**BT**	**UMTS**
DC-Gain [dB]	66.68	66.35	55.55	52.28	68.19	67.28	66.09	68.63	68.62
GBW [MHz]	104.83	192.97	121.14	209.78	50.24	132.50	166.86	51.68	95.52
Phase margin [º]	73.24	72.15	82.42	82.25	79.14	78.02	77.78	79.80	79.14
Slew-rate [V/μs]	98.76	193.47	105.92	214.09	36.34	105.77	140.18	37.67	73.54
Eq. Load [pF]	0.55	0.56	0.27	0.28	0.17	0.17	0.17	0.17	0.17
OSW [V]	1.84	1.69	1.55	1.28	1.85	1.58	1.49	1.87	1.73
Eq. input noise [nV/$Hz^{1/2}$]	14.80	9.98	18.53	11.56	25.35	13.88	11.68	25.98	17.94
Bias current [μA]	188.63	377.26	100.62	201.24	58.17	174.52	232.70	61.41	122.82
Power [mW]	0.99	1.95	0.46	0.82	0.31	0.90	1.16	0.33	0.64

6.6 SUMMARY

The results that have been presented in this Chapter show how the design methodology proposed in this Thesis can be applied in the design process of complex analog and mixed-signal systems that must fulfill different sets of specifications. Different cascade architectures of a reconfigurable ΣΔ modulator have been considered and, for each one, the mm-PoF has been generated. At modulator level, the mm-PoFs have been generated using mm-PoFs of amplifiers of 4 operation modes, which are used to implement the reconfigurable integrators of the modulator. Several reconfiguration directives are considered regarding the reconfigurability of the amplifiers that implement the integrators for the different operation modes of the modulator. At modulator level, the candidate solutions are evaluated using Simulink® models and SIMSIDES, where the integrators are instantiated using macro-models that take into account the real performances of the amplifiers of the low-level mm-PoFs.

CONCLUSIONS

This work presents a contribution in the field of systematic design methodologies of reconfigurable analog and mixed-signal circuits and systems. Reconfigurable analog circuits are essential in the current multi-standard paradigm as they provide indisputable advantages: reduced area occupation and power adaptability. However, in order to be able to design such systems according to the tight constraints imposed by the market demands, it is crucial to develop efficient design methodologies that reduce the design gap between the digital and the analog domains. Although analog circuits might represent a small fraction of a complete mixed-signal system, most of the design time is spent there because the available analog CAD tools are far from the level of automation of the digital counterpart.

The work presented in this thesis arises motivated by these problems, providing a new bottom-up design methodology based on the use of the Pareto-optimal fronts (PoFs) of analog circuits. These fronts capture the best achievable trade-offs between conflicting circuit performances. The first contribution of this work is a new method that allows to obtain the PoFs of reconfigurable circuits, what we have called multi-mode PoFs. For this, a new evolutionary algorithm has been constructed, which allows optimizing simultaneously the multiple sets of performances that reconfigurable circuits provide. The algorithm is validated using the generation of the mm-PoF of a reconfigurable folded-cascode, Miller-compensated operational amplifier.

Secondly, two key implementation issues regarding the hierarchical composition of PoFs and mm-PoFs have been addressed for the first time. The first one is related to the context dependence of the performances of analog circuits. A solution for this problem has been presented for the case of operational amplifiers, which are one of the most common circuits used in almost any electronic system and whose performances rely greatly on the load impedance. The provided solution is a new technique that allows re-evaluating the performances of amplifiers under different loading conditions. The technique is based on the use of the poles and zeroes of the gain and output impedance of the amplifiers and it does not require device-level simulation. This characteristic allows using it dynamically during the generation of mm-PoFs of complex systems without significantly impacting in the CPU time.

The second issue regarding the composition of PoFs is related to the exploration of the PoFs of lower-level blocks during the generation of the PoFs of higher-level blocks. Specifically, it refers to how the optimizer -the new evolutionary algorithm- has to explore the performances of PoFs (or mm-PoFs) of lower-level blocks, which are part of the search space during the optimization of higher-level blocks. The

solution proposed in this work assigns a set of unique coordinates to each design of a lower-level PoF, so that the algorithm can explore efficiently and meaningfully the lower-level PoFs using those coordinates as design variables.

The capabilities of the methodology presented in this thesis, along with all the solutions proposed to solve the implementation issues of the hierarchical composition of PoFs and mm-PoFs, have been demonstrated in two design problems:

- The mm-PoF of a 0.35-μm continuous-time low-pass active filter that fulfills specifications for GSM and DECT standards has been generated. For this, mm-PoFs of operational amplifiers have been hierarchically composed. The amplifiers are implemented using a folded-cascode, Miller-compensated topology. The mm-PoF of the reconfigurable filter, as well as those of the reconfigurable amplifiers, are generated for two operation modes and using HSPICE as circuit evaluator.

- The mm-PoF of a 130-nm CMOS reconfigurable ΣΔ modulator requied to fulfill specifications for GSM, Bluetooth and UMTS standards has been generated. This second application example entails more complexity than the previous one as the number of operation modes that must be optimized is higher. In this case, mm-PoFs of reconfigurable amplifiers of four operation modes, which are used to implement the integrators of the modulator, have been hierarchically composed. Besides, several reconfiguration directives are considered in this experiment, which gives the optimizer total freedom to explore them and decide which is the best suited for the required specifications. The mm-PoF of the reconfigurable modulator has been generated using MATLAB/Simsides as circuit evaluator. In the case of the generation of the mm-PoFs of the reconfigurable amplifiers, the evaluator has been HSPICE.

In the first desing problem, the methodology presented in this Thesis is applied in a pure bottom-up design process. In the second scenario, on the other hand, the methodology is used to complement a high-level exploration process of different architectures for the reconfigurable modulator. Here, instead of using estimations of low-level blocks specifications, the methodology presented in this Thesis allows using accurate values of performances, as well as the reconfiguration capabilities, of the low-level blocks at early stages of the design process. This represent an important advantage over traditional top-down approaches, where bad estimations for low-level blocks specifications lead to undesired repetitions of the whole design process.

7

APPENDIX I

PSEUDOCODE OF THE NEW MULTI-MODE MOEA FUNCTIONS

Algorithm 1: Intra-individual dominance check.

```
Intra individual Dominance(mode A, mode B):

    //First the constraint violation is compared:
    if constraint violation (mode A) < constraint violation (mode B) then
        mode A is intra-dominated by mode B

    else if constraint violation (mode A) > constraint violation (mode B) then
        mode B is intra-dominated by mode A

    //In case the constraint violation is equal then the design objectives are compared:
    else if constraint violation (mode A) > constraint violation (mode B) then
        set dom1 = 0
        set dom2 = 0
        for each design objective
            if  design objective(mode A) < design objective(mode B) then
                set dom1 = 1

            else if design objective(mode A) > design objective(mode B) then
                set dom2 = 1

        if dom1 = 1 and dom2 = 0 then
            mode B is intra-dominated by mode A

        else if dom1 = 0 and dom2 = 1 then
            mode A is intra-dominated by mode B
```

Algorithm 2: Multi-mode assignment of the crowding distance.

```
Assignment of the Multi-mode Crowding Distance (population)

    //1st: Create the auxiliary population where each mode is treated as an individual:
    for each individual of the population
        for each mode of each individual:
            add mode of the individual to the auxiliary population

    //2nd: Crowding distance assignment for the auxiliary population.
    crowddist_assignment (auxiliary population);

    //3rd: Assignment of the crowding distance to the multi-mode individuals:
    for each individual of the population:
        set crowding distance(individual) to 0
        for each mode of each individual:
            crowding distance(individual) = crowding distance(individual) + crowding distance(mode)

        //Average the value of the crowding distance among the number of modes:
        crowding distance(individual) = crowding distance(individual)/nmod
```

Algorithm 3: Inter-individual dominance check.

```
inter-individual dominance check (ind. A, ind. B)

    //1st: mark the dominated modes of the individuals:*/
    for each mode of each individual
        if the mode violates constraints or if it is intra-dominated then:
            set mode as dominated
            increase the number of dominated modes of the individual in 1

    //2nd: Cross-wise inter-dominance check between the non-dominated modes of the individuals.
    for mode A = each mode of ind. A:
        for mode B = each mode of ind. B:
            if mode A is not dominated and mode B is not dominated then:
                set dom1 = 0
                set dom2 = 0
                for each design objective:
                    if design objective (mode A) < design objective (mode B) then:
                        set dom1 = 1
                    else if design objective (mode A) > design objective (mode B) then:
                        set dom2 = 1

                if dom1 = 1 and dom2 = 0 then:
                    increase number of dominated modes of ind. B in 1
                else if dom1 = 0 and dom2 = 1 then:
                    increase number of dominated modes of ind. A in 1

    //Case 1:
    if all modes of both individuals violate constraints then:
        if constraint violation (ind. A) < constraint violation(ind. B) then:
            ind. A is dominated by ind. B
        else if constraint violation (ind. A) > constraint violation(ind. B) then:
            ind. B is dominated by ind. A
        else if constraint violation (ind. A) > constraint violation(ind. B) then:
            both individuals are not dominated between them

    //Case 2:
    else if ind. B violates constraints in all modes and ind. A fulfills constraints in some mode then:
        ind. B is dominated by ind. A
    else if ind. A violates constraints in all modes and ind. B fulfills constraints in some mode then:
        ind. A is dominated by ind. B

    //Case 3:
    else if both individuals fulfill constraints in some mode then:
        if constraint violation (ind. A) < constraint violation (ind. B) then:
            ind. A is dominated by ind. B
        else if constraint violation (ind. A) > constraint violation (ind. B) then:
            ind. B is dominated by ind. A
        else if constraint violation (ind. A) = constraint violation (ind. B) then:
            if ind. A has less dominated modes than ind. B then:
                ind. B is dominated by ind. A
            else if ind. A has more dominated modes than ind. B then:
                ind. A is dominated by ind. B
            else both individuals have the same number of dominated modes then:
                both individuals are not dominated between them
```

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APPENDIX II

PSEUDOCODE OF THE LOAD TRANSFORMATION TECHNIQUE

Algorithm 4: Load transformation of performances of operational amplifiers.

```
load transformation:
    //Parameters:
    GLo = transconductance of the initial loading conditions
    CLo = capacitance of the initial loading conditions

    GLf = transconductance of the final loading conditions
    CLf = capacitance of the final loading conditions

    Ao   = gain at initial loading conditions
    Zout = output impedance

    Fuf = unity-gain frequency at final loading conditions
    PMf = phase-margin at final loading conditions
    Af  = gain at the final loading conditions

    /*First: Calculation of the productories of poles and zeroes*/
    /*Productory of the poles of the output impedance (prodpi)*/
    prodpi = 1
    for pole = each pole of the output impedance:
            prodpi = prodpi * (-pole)

    /*Productory of the zeroes of the output impedance (prodri)*/
    prodri = 1
    for zero = each zero of the output impedance:
            prodri = prodri * (-zero)

    /*Productory of the poles of the gain (prodpli)*/
    prodpli = 1
    for pole = each pole of the gain:
            prodpli = prodpli * (-pole)

    /*Productory of the zeroes of the gain (prodzi)*/
    prodzi = 1
    for zero = each zero of the gain:
            prodzi = prodzi * (-zero)

    /*Third: Calculation of the denominator and numerator of the new transffer function*/
    ppi = polynomial of the poles of the output impedance
    pri = polynomial of the zeros of the output impedance
    ppli = polynomial of the poles of the gain at the initial loading conditions
    pzli = polynomial of the zeros of the gain at the initial loading conditions

    /*Calculation of numerator and denominator of the gain at the final loading conditions:*/
    numerator = [(GLo + sCLo) * Zout * prodpi) * pri + (ppi * prodri) ] * pri * ((Ao * prodpli)/prodzi)
    denominator = [((GLf + sCLf) * Zout * prodpi) * pri + (ppi * prodri) ] * prodpli
```

```
/*Calculation of the Unity-gain Frequency in the new loading conditions:*/
nfpoints = 50
wlow = 1e-4
whigh = 1e11

do while (whigh-wlow)/whigh > 1e-7:
    logfreqival = log10(whigh/wlow)/nfpoints
    wfreq = wlow/10^(logfreqival)
    magnitude = 0
    for j=0:nfpoints:
        wfreq = wfreq*10^(logfreqival);
        magnitude[j] = evaluate(numerator at wfreq) / eval(denominator at wfreq)

        //If magnitude has changed sign:
        if magnitude[j] < 1 and magnitude[j-1] > 1 then:
            Fuf = (wfreq*fscale)/(2*pi)
            whigh = wfreq
            wlow = wfreq/10^(logfreqival)
            break for loop

/*Calculation of the Phase-margin in the new loading conditions:*/
/*Contribution of the poles:*/
PMf = 0
wu = Fuf*2*pi

for pole = each pole of the output impedance:
    if the pole has no imaginary part then:
        PMf = PMf + ((-atan(wu))/abs(real part(pole)))*360 / (2*pi)

    else if the pole has imaginary part then:
        ALFA = real part of the pole
        BETA = imaginary part of the pole
        PMf = PMf + (-atan((2*wu*abs(ALFA))/(ALFA^2+BETA^2-wu^2)))*360 / (2*pi);


/*Contribution of the zeros:*/
wu = Fuf*2*pi

for zero = each zero of the gain:
    if the zero has no imaginary part and is negative then:
        PMf = PMf + ((atan(wu))/abs(real part(zero)))*360 / (2*pi)

    else if the zero has no imaginary part and is positive then:
        PMf = PMf + ((-atan(wu))/real part(zero))*360 / (2*pi)

    else if the zero has imaginary part and the real part is negative:
        ALFA = real part of the zero
        BETA = imaginary part of the zero
        PMf = PMf + (atan((2*wu*abs(ALFA))/(ALFA^2+BETA^2-wu^2)))*360 / (2*pi);

    else if the zero has imaginary part and the real part is positive:
        ALFA = real part of the zero
        BETA = imaginary part of the zero
        PMf = PMf + (-atan((2*wu*ALFA)/(ALFA^2+BETA^2-wu^2)))*360 / (2*pi);

PMf = PMf + 180


/*Calculation of the DC-Gain in the new loading conditions:*/
Af = evaluate numerator at(0) / evaluate denominator at(0)
```

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