A BIST Solution for Frequency Domain Characterization of Analog Circuits

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Abstract: *This work presents an efficient implementation of a BIST solution for frequency characterization of analog systems. It allows a complete characterization in terms of magnitude and phase, including also harmonic distortion and offset measurements. Signal generation is performed using a modified filter, while response evaluation is based on 1st-order ΣΔ modulation and very simple digital processing. The signal generator and the response analyzer have been implemented using the Switched-Capacitor (SC) technique in a standard 0.35μm-3.3V CMOS technology. Both circuits have been separately validated, and an on-board prototype of the complete test system for frequency characterization has been implemented. Experimental results verify the functionality of the proposed approach, and a dynamic range of 70dB@62.5kHz (1MHz clock) has been demonstrated.*

Keywords: Analog BIST, Signal Generator, Frequency Response Characterization, On-Chip Spectrum Analyzer, On-Chip Network Analyzer.

I. Introduction

Nowadays, complex mixed-signal electronic systems are extensively developed. Consequently, the increasing cost associated with testing these complex systems have motivated research efforts to explore more efficient testing methodologies. This issue is identified in the SIA Roadmap for Semiconductors [1] as one of the key problems for the development of current and future mixed-signal Systems-on-Chip (SoCs).

Usually, the test of the analog parts represents the main bottleneck in this line. Traditional test methods for analog circuits rely in functional tests, demanding high quality input stimuli, and high data volume acquisition and processing capability. Moreover, the sensitivity of analog cores to test conditions and process variations make their test a difficult task that requires expensive ATE (Automatic Test Equipment). BIST (Built-in Self-Test) schemes are a well-accepted technique to overcome some of these problems. These schemes consist of

moving part of the required test resources from the ATE to the chip [2].

Most of the analog subsystems composing complex SoCs are tested and/or characterized using frequency-related specifications, such as gain, phase-shift or delay, distortion, etc. These specifications are usually measured using dedicated test equipment that applies a periodic input stimulus to the Circuit Under Test (CUT), and performs complex spectral processing algorithms to the test response. Moving test signal generation and response evaluation to the CUT is a key issue to extend these frequency related tests to a full BIST scheme. In this line, some interesting work on generation and evaluation of periodic signals for BIST applications has been published for the last years [3]-[15]. Among them, preferred solutions are those with the following attributes: a) low-speed digital interface, b) programming capability to accommodate the test to the target parameter, c) robustness against environmental noise and process variations and, d) low design efforts and reduced area overhead.

Many of the reported BIST solutions adopt digital techniques. These approaches make use of a DAC interface for stimuli generation, and an ADC for digitizing the response [3], [5], [6], [8], [12], [15]. In particular, the use of ΣΔ modulators for generating and acquiring test signals have been successfully exploited [4]-[5], [11]-[14]. Concerning signal generation, ΣΔ encoded bit-streams are proposed in [4]-[5] to generate high quality sinewaves. This is a very attractive solution if the quantization noise does not need to be removed. Otherwise, a highly selective post-filtering is required, which may mean a large area and/or power overhead. On the other hand, the work in [12] demonstrates that ΣΔ modulators can be also used as efficient A/D interfaces for functional analog test applications. However, the approach in [12] makes use of a complex FFT algorithm to extract the test parameters from the digitized response. The complexity of the evaluation algorithm makes it unsuitable for its on-chip implementation, unless the required resources are available in the system and they can be reused.

A complete BIST scheme for frequency-domain characterization, including on-chip stimuli generation and functional evaluation of the response, can be found in [6]-[8]. Signal generation in [8] is based on a SC variable gain amplifier, while response evaluation is carried out using a programmable bandpass filter followed by an amplitude detector. On the other hand, reference [6] proposes a frequency synthesizer for stimulus generation, and analog multipliers together with amplitude/phase detectors for extracting gain and phase-shift parameters. Both solutions, although simple and compact, perform all the operations in the

analog domain, and are limited to applications demanding a low dynamic range.

Authors reported in [10] a technique for sinusoidal test stimulus generation where the required resources are mainly reduced to a modified analog filtering stage. On the other hand, authors exploit in [13] the noise shaping properties of 1st-order ΣΔ modulators to propose a robust signal evaluator that extracts, digitally encoded, the main characteristics of an analog periodic signal without the need of complex processing. Both approaches were validated through electrical and behavioral simulations.

This paper extends the previous work [10], [13] in several ways. Firstly, it presents a set of prototypes in a standard 0.35μm CMOS technology of the previously proposed signal generator and evaluator. Secondly, they are validated and characterized in the laboratory as stand-alone circuits. A wide set of experimental results are shown to validate their functionality. Finally, a complete BIST solution for frequency domain characterization of analog circuits is built using the developed test blocks. An on-board demonstrator for the proposed system is described and characterized in the laboratory.

This paper is organized as follows. Section II introduces the proposed BIST scheme and the solutions for signal generation and evaluation. Section III presents the design of the test system main building blocks in a 0.35μm CMOS technology. Section IV shows some experimental results and compares them to other reported approaches. Finally, Section V summarizes the main contributions of this work.

II. System description

The block diagram of the proposed system is shown in Figure 1. It is composed of three main blocks, apart from the CUT:

- A compact sinewave generator whith digital control for signal amplitude and frequency. It is based on a modified filter able to perform two operations at the same time: signal generation from a DC input, and filtering of any unwanted spectral components.
- A signature extractor composed by two matched 1st-order ΣΔ modulators and digital counters. It provides two digital words that encode the main characteristics of the test response signal. Target CUT performance parameters such as offset, gain, phase shift, and harmonic distortion can be easily extracted by processing these digital words.
- Some digital logic for control, clock generation and synchronism tasks, as the main interface with the external test equipment.

The basic operation of the system can be briefly explained as follows. After amplitude and frequency selection, the control logic programs the signal generator to deliver the corresponding sinewave signal. This signal is firstly entered to the signature extractor, which produces two digital words encoding the characteristic parameters of the test signal. Signal parameters (DC-level, amplitude, phase, distortion) are then extracted by simple processing and stored as reference values. After that, the generated sinewave signal is passed to the CUT and its response is processed by the signature extractor. The generated signatures are then processed and related to the stored reference values to extract the target measurement.

A. Sinewave Generator

Digital solutions for signal generation usually follow the general scheme in Figure 2 [4]-[5], [8], [9], [12], [15]. The test signal is firstly generated in the digital domain, and then converted to analog by a D/A interface. In general, the generation of sinusoidal test signals requires a smooth analog filter front-end. Its mission is to attenuate the level of undesired harmonics and other frequency components coming from the D/A interface. Assuming that the digital part and the D/A converter are ideal, the spectral quality of the generated signal is finally determined by the characteristics of this front-end filter in terms of its shape and linearity. The solution adopted in this work implements the technique described in [10] to reduce the sinewave generator to mainly the front-end analog filter, together with a simple digital interface for control and synchronization tasks. Hence, this approach implies clear benefits in terms of area savings and complexity reduction.

Figure 3 shows the proposed sinewave generator block diagram, and the corresponding time diagram. It consists of a SC lowpass second-order filtering stage with two non-overlapping clock phases, Φ_1 and Φ_2, and a DC input, V_{ref}. Signal generation is carried out through a digitally programmable capacitor array, $C_J[m]$, and the switching input scheme controlled by signals Φ_{c1} to Φ_{c4} and Φ_{IN}. The capacitor array $C_J[m]$ is composed by a set of four capacitors, C_{Jm}, weighted as,

$$C_{Jm} = C_J \sin(m\pi/8) \qquad m = 1, ..., 4 \tag{1}$$

These capacitors are sequentially switched following the timing scheme illustrated in Figure 3c. Due to the symmetry of a sinewave, these four capacitors are enough to implement the positive part of a 16-step sinewave, while the input switching scheme sets the weight (positive or negative) of each step. This way, the charge $Q_{CJ}(m)$ transferred by $C_J[m]$ to the core filter in the m-th clock cycle can be expressed as,

$$Q_{CJ}(m) = \left\{\Phi_{IN}(m) - \overline{\Phi_{IN}(m)}\right\} C_{Jm} V_{ref} \qquad m = 1,2,3,\ldots,15 \tag{2}$$

which is equivalent to the charge that would be transferred by a capacitor of value C_J and charged with a voltage corresponding to the m-out-of-16 step of a sinewave of amplitude V_{ref}, that is,

$$Q_{CJ}(m) = V_{ref} C_J \sin(m\pi/8) \qquad m = 1,2,3,\ldots,15 \tag{3}$$

In other words, the response of the circuit is equivalent to the response of a linear-time invariant filter to such 16-step sinewave, and thus, the proposed circuitry performs the necessary two operations, signal generation and filtering of unwanted components, at the same time. Moreover, the amplitude of the generated signal can be controlled through the DC input, V_{ref}, and its frequency through the frequency of the external control signals Φ_{c1} to Φ_{c4}.

It is convenient to remark that the quality of the generated signal depends strongly on the matching between capacitors, which is usually very good in CMOS technologies. In particular, typical values of 99.9% matching can be achieved in our selected 0.35μm CMOS technology. In addition, the spectral purity of the output is increased due to the filtering action. For that, the main tone of the output (1/16 of the clock frequency) has been placed in the passband while the unwanted harmonic components have been located in the rejection band.

B. Signal Characterization

The signal characterization solution proposed in this work is able to extract, in the digital domain, the DC-level and the amplitude and phase-shift of the harmonic components of a periodic signal [13]. Figure 4 depicts the block diagram of the system together with an example of the corresponding timing diagram. Its functionality can be briefly described as follows. Let $x(t)$ be a periodic signal of period T. This signal is firstly modulated by two square waves in quadrature, $SQ_k^T(t)$ and $SQ_k^T(t\text{-}T/4k)$, of unit amplitude and period T/k, where k is an integer. The resulting signals $y_{1k}(t)$ and $y_{2k}(t)$ are fed to two matched 1st-order ΣΔ modulators, with an oversampling ratio $N=T/T_s$, where T_s is the sampling period. The generated bit-streams d_{1k} and d_{2k} are then integrated along an integer number M of periods of the signal under evaluation using a set of counters to obtain the digital signatures I_{1k} and I_{2k}. A weighting strategy [13] that cancels the contribution of the offset of the modulators has been used in the counters. It can be shown that, if M is even and $N/2^3k$ is integer, the

amplitude, A_k, and phase, φ_k, of the k-th harmonic of signal $x(t)$, and its DC-level, B, are confined in bounded intervals and related to the signatures I_{1k} and I_{2k} as follows (for $k=0$ it has been set $SQ_0^T(t) = 1$),

$$\left(A_K\right)^2 \in \left(\frac{\pi}{2}\frac{1}{MN}\right)^2 \left[\min\left\{\left(I_{1k}+\varepsilon_{1k}\right)^2+\left(I_{2k}+\varepsilon_{2k}\right)^2\right\},\ \max\left\{\left(I_{1k}+\varepsilon_{1k}\right)^2+\left(I_{2k}+\varepsilon_{2k}\right)^2\right\}\right] \tag{4}$$

$$\tan\varphi_k \in \left[\min\left(\frac{I_{1k}+\varepsilon_{1k}}{I_{2k}+\varepsilon_{2k}}\right), \max\left(\frac{I_{1k}+\varepsilon_{1k}}{I_{2k}+\varepsilon_{2k}}\right)\right] \tag{5}$$

$$B \in \frac{1}{MN}\left[I_{10}-\varepsilon_{10}, I_{10}+\varepsilon_{10}\right] \quad or \quad \frac{1}{MN}\left[I_{20}-\varepsilon_{20}, I_{20}+\varepsilon_{20}\right] \tag{6}$$

where ε_{1k} and ε_{2k} (k= 0, 1, 2,...) are unknown error terms, and magnitudes A_k and B are normalized with respect to the full-scale range of the ΣΔ modulators. The error terms are due to the quantization noise in the ΣΔ modulators, and it can be proved [13] that they are limited to $\varepsilon_{1k}, \varepsilon_{2k} \in \left[-4, 4\right]$. Since I_{1k} and I_{2k} are proportional to the number of evaluation samples (MN), then it should be clear that the relative errors of the measurements can be reduced by increasing the product MN. Furthermore, the required digital processing of the signatures I_{1k} and I_{2k} is very simple, which opens the possibility to realize it on-chip or externally with conventional arithmetic DSP.

C. Control and System Synchronization Considerations

An important feature of the proposed characterization system is the inherent synchronization between the signal generator and the signature extractor when the same master clock is used to generate the necessary clocks and control signals. This is illustrated in Figure 5, where the master clock is used directly to generate the clocks and control signals needed by the signature extractor, while a 1/6 division of the master clock is used in the generation of the clocks and control signals in the generator. Given that the signal generator provides a signal of frequency 1/16 of its clock frequency, then the oversampling ratio in the modulators is set to N=6×16= 96.

III. Building Blocks Design

A. Sinewave Generator

The schematic of the sinewave generator was already shown in Figure 3. Table I shows the normalized capacitor values used in the design. These values have been set to obtain a

peak-gain of 6dB at frequency 1/16 the clock frequency, and a pole quality factor Q=5. The peak-gain frequency has been made coincident by design with the fundamental frequency of the intended sinewave, so the main tone is amplified, while harmonic components are attenuated, thus improving the spectral purity of the output.

Both the amplitude, A_{output}, and frequency, f_{output}, of the output signal are linearly controlled by the input DC voltage, V_{ref}, and the clock frequency, f_{clock}, respectively as given by,

$$\begin{aligned} A_{output} &= V_{ref} \times peak-gain \\ f_{output} &= f_{clk}/16 \end{aligned} \tag{7}$$

The need of an external DC-input V_{ref} for amplitude control can be avoided by generating it either internally or externally through digital techniques. For example, using the well-known technique based on the analog integration of a digital Pulse Width Modulated (PWM) signal [14]. In this way, the interface with the external equipment can be made purely digital as represented in the general scheme in Figure 1.

B. Signature Extractor: ΣΔ modulator with built-in input square-wave modulation

Figure 6 shows the schematic of the implemented fully differential first-order ΣΔ modulator. The ratio C_I/C_F in Figure 6 has been set to 0.4 in order to avoid saturation effects in the amplifier while maintaining a moderate gain in the integrator. The switching input interface has been properly modified in order to perform the required input square-wave modulation; the modulator operates with two non-overlapping clock phases (ψ_1, ψ_2) while the control signal q_k gives the proper weight (positive or negative) to the input *Vin*.

The Opamp, also used in the design of the filter, is a single stage fully-differential folded-cascode structure with SC common-mode feedback. A simple dynamic latch has been used as a comparator.

IV. Experimental results

The sinewave generator and the analog part of the signature extractor, which includes the two first-order ΣΔ modulators with built-in input square-wave modulation, were integrated in a standard 0.35 μm-3.3V CMOS technology. Figure 7 shows microphotographs of both systems. The signal generator occupies an area of 280μm×550μm using a 300fF capacitor as unitary capacitance. Approximately, a 60% of the area is due to the capacitor array, as it has been marked in the figure. However, it is convenient to remark that the presented

implementation can be greatly optimized in terms of area. It can be proved [10] that the proposed design tolerates capacitance variations up to 2% without degrading performance figures, while, according to the selected technology specifications, the employed capacitors will have a mismatch of around 0.2%. Hence, capacitor sizes can be reduced without affecting the performance, and so the total area can be further reduced.

Concerning the signature extractor, the two ΣΔ modulators occupy an area of only 270μm×250μm. The digital part has not been integrated, but its area overhead has been estimated. Figure 8 shows a direct synthesis from a Verilog description of the digital processing circuitry using 16-bit counters. The synthesis was performed using a standard-cell library in the same 0.35μm CMOS technology. It takes an area of 300μm×300μm approximately.

An on-board prototype of the test system shown in Figure 1 was developed to show the feasibility of the proposed approach. The on-board demonstrator, depicted in Figure 9, makes use of the previously integrated sinewave generator and signature extractor. A fully differential active-RC filter has been included as a CUT. External digital equipment provides the required digital control signals and clocks, and processes the digital signatures to extract the test parameters.

The following subsections present some relevant experimental results. Three different classes of experiments have been carried out. Two of them aim to validate the signal generator and the signature extractor separately using external equipment. The third one aims to demonstrate the functionality of the complete frequency characterization test system.

A. Sinewave Generator

A set of experiments have been developed to test the functionality of the sinewave generator, and to mesure the spectral purity of the generated signals. The generated sinewaves in these experiments are directly captured and processed by external test equipment.

Figure 10a shows the generator output signals, captured with a digital oscilloscope, corresponding to three different DC input reference differential levels: 150mV, 250mV and 300mV. The amplitudes of the generated waveforms are 300mV, 500mV and 600mV, respectively. The output frequency is 62.5kHz corresponding to a clock frequency of 1MHz (62.5kHz= 1MHz/16). Figure 10b shows the spectrum measured with an external spectrum analyzer for the generated 1Vpp, 62.5kHz output signal. The SFDR is 70dB and the THD is

67dB.

Figure 11 shows the achieved performance in terms of THD and SFDR when sweeping both the output amplitude, from 300mV to 600mV, and frequency, from 5kHz to 62.5kHz. As it can be deduced, the quality of the generated signal keeps approximately constant over the whole operational range.

B. Signature extractor

Different experiments were performed in order to verify the functionality of the sinewave evauator. Test stimuli, digital control signals, and the sampling clock for these experiments were provided by an external ATE and fed to the evaluator block.

The first set of tests is aimed to prove the functionality and accuracy of the evaluation strategy. It consists of verifying the dependency of the digital signatures with the number of evaluation samples. Figure 12a represents the obtained digital codes corresponding to the amplitude measurements for a 0.6V single tone when sweeping the number of evaluation samples. The sampling frequency in the modulator was 1MHz and the oversampling ratio was N=144. All the codes are confined in a linear band with error bounds limited to ±3, which is in agreement with the maximum expected error of ±4 from (4). Figure 12b shows the evolution of the relative error in these measurements. It decreases drastically, as expected, with the number of samples.

The system capability for harmonic characterization is demonstrated in Figure 13. This figure shows the measurements of a multitone signal composed by three harmonic components: A_1=−11.02dBFS, A_2=−30.9dBFS, and, A_3=−50.8dBFS. Values in dBFS are normalized with respect to the full-scale range of the modulators. The oversampling ratio was set to N=96, while the number of periods M taken for the evaluation has been swept from M=20 to M=1000. Twenty-five runs per M value were carried out to demonstrate that the measurements are repeatable and, in any case, the values are confined in the corresponding intervals. Sensitivities of fractions of dBFS are achieved very quickly, and the bounded intervals are tighter as the number of samples increases. Also, it is clearly shown how the measurements of the second and third harmonics are approximately 20dB and 40dB below the main one.

C. Complete System

A fully-differential active-RC 2nd-order lowpass filter with a cutoff frequency around

1kHz has been selected as the CUT to validate the operation of the complete system as a network analyzer. The experiments addressed the measurement of the filter gain and phase Bode diagrams.

Firstly, the test stimulus is characterized. Due to the amplitude stability of the signal generator and the synchronism with respect the control signals, this characterization is performed only once. For that, the CUT is bypassed and the generated waveform feeds directly the signature extractor. The amplitude and phase with respect the square waves used for modulation are computed and the corresponding digital codes, C_{A_REF} and C_{ϕ_REF}, respectively, are stored to be used as reference codes. Following the protocol depicted in Figure 14, the gain of the CUT at a given frequency can then be computed as the ratio of the obtained amplitude digital code C_{A_OUT} and C_{A_REF}, while the phase shift is the difference between the corresponding code C_{ϕ_OUT} and C_{ϕ_REF}.

Figure 15 shows the obtained bode magnitude and phase diagrams. Measurements were performed taking 200 periods for the evaluation. The blue stars mark each measurement, while the solid line represents the measurements obtained with an external sinewave generator and a digital oscilloscope for comparison purposes. The agreement between both measurements is very good.

The system capability to measure harmonic distortion is illustrated in Figures 16a and 16b. These figures show the estimation of the second and third harmonic components of the filter output for two different inputs: 800mVpp@1.6kHz, and 800mVpp@1.3kHz, respectively. Harmonic distortion measurements were performed taking 400 periods for the evaluation. The solid line is the spectrum measured with a digital oscilloscope. The depicted confidence intervals have been calculated accordingly to (4). The agreement between the commercial system and our proposed test system is good, and, if a better precision is needed, it can be achieved just by increasing the number of evaluation periods.

The offset measurement capabilities are illustrated in Figure 17. The offset of the filter was evaluated as the difference between the digital code of the DC level of the input signal and the digital code of the DC level of the output signal. Figure 17 shows the obtained offset measurement versus the frequency of the input signal used for the evaluation. The frequency of the input signal has been swept up to 20kHz, the same frequency range considered for the evaluation of the Bode diagrams. The solid line represents the offset level measured with the external generator and the digital oscilloscope, which results to be close to zero along the considered frequency range. The stars correspond to the proposed analyzer taking 2 periods

of the signal for evaluation, and the dashed-line band represents the expected measurement range predicted by (6). The agreement between the measurements is very good, and, again, if a better precision is needed, it can be achieved just by increasing the number of periods taken for evaluation.

D. Comparison with state-of-the-art integrated solutions

In order to provide an overview of the current state-of-the-art in analog built-in test systems, Table II summarizes relevant reported approaches with experimental results from integrated prototypes. It is important to notice that these approaches have different application scenarios and capabilities, so a face-to-face comparison is not meaningful. Instead of that, this section is aimed to place the achieved results into perspective.

The integrated test core presented in [3] is mainly digital and very versatile, which make it very attractive. However, due to the required oversampling in the generator, the applications are limited to a small fraction of the clock frequency (20MHz reported), while a large filtering is required to obtain high quality sinewaves. A digitizer captures the test reponse with an effective sampling rate of 4 GHz through subsampling, but all processing, such as FFT for frequency characterization, must be done externally.

The SC spectrum analyzer in [8] is simple, cost-effective in terms of area and power, and contemplates harmonic measurement. However, it is limited to applications requiring low dynamic range (40dB@10kHz demonstrated)

The work in [6] presents a small area, digital interface, and a wider frequency range, up to 130 MHz. It includes magnitude and phase measurements, but the dynamic range is limited to 30dB, an ADC is required at the output, and power consumption is higher.

The work in [15] presents an FPGA-based BIST solution able to perform analog functional measurements, including frequency response characterization, both magnitude and phase, linearity figures such as the input-referred IP3, and Noise Figure measurements, by a simplified spectral digital processing. It is purely digital, so it could be efficiently implemented as standard cells via synthesis tools. However, it relies on the reuse of existing DAC and ADC for providing the test stimuli and acquiring the CUT response, respectively, and hence the test accuracy depends on the availability of high-resolution ADCs and DACs within the system under test. This approach is hence particularly suitable for testing analog blocks embedded in mixed-signal SoCs, where these converters are usually available.

The work presented herein is capable of a complete frequency characterization including

magnitude harmonic composition, phase-shift, and offset. The area has been estimated taking into account the generator (0.15mm^2), the signature extractor (0.065mm^2) and the estimation of the required DSP circuitry (0.09mm^2) for parameter extraction from the digital signatures. The presented solution offers the best dynamic range for similar operation frequencies. However, it is not free of limitations. Thus, the proposed test core has been demonstrated to be particularly good for analog filter characterization, but the developed generator is not suitable for multitone signal generation, so two-tone measurements are not feasible. In addition, the frequency range of the presented implementation is limited by the SC technique and the need of oversampling in the signature extractor. Nevertheless, the proposed generation strategy can be extended to higher frequencies by using appropriate design techniques (for instance, OTA-C, MOSFET-C, or other continuous-time approach) in accordance to the frequency range of interest [10], [16].

V. Conclusions

A practical implementation of a switched-capacitor BIST solution for frequency characterization has been presented. The proposed scheme allows a complete characterization in terms of magnitude and phase, including harmonic components and offset. The communication with the external tester is purely digital, which reduces the cost of the required test equipment. Signal generation is performed using a modified SC filter that, controlled by digital signals, performs the operations of signal generation and filtering of unwanted components. The CUT response evaluation is based on 1st-order ΣΔ modulation and a very simple digital processing, which gives the attributes of robustness and simplicity.

The main building blocks of the scheme have been implemented in a standard 0.35μm-3.3V CMOS technology and characterized separately in the laboratory. Results in this sense agree with the analytically expected behaviour. The complete frequency characterization test scheme has been mounted on a board and its feasibility demonstrated using a second-order continuous-time filter as a CUT. A dynamic range of 70dB@62.5KHz (1MHz sampling rate) has been demonstrated, which improves significantly the results from other reported approaches. The main limitations of the developed prototype are the reduced frequency range due to the need of oversampling, and also its functionality is restricted to single-tone measurements.

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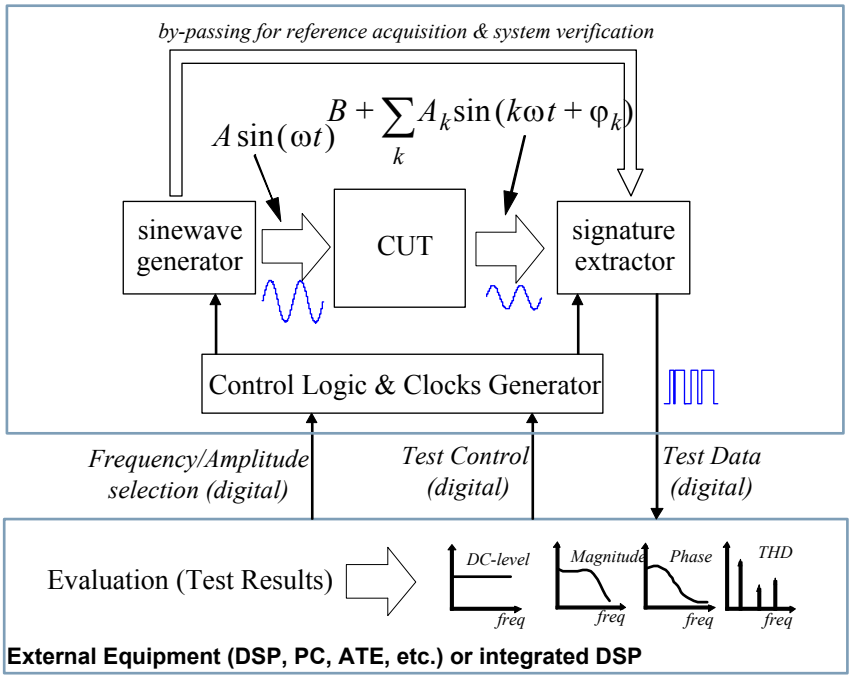

Figure 1: Conceptual block diagram of the proposed characterization system.

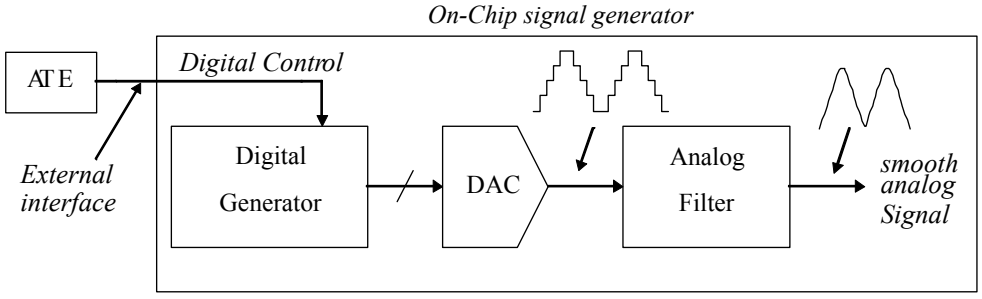

Figure 2: Block diagram of digital-based analog signal generators.

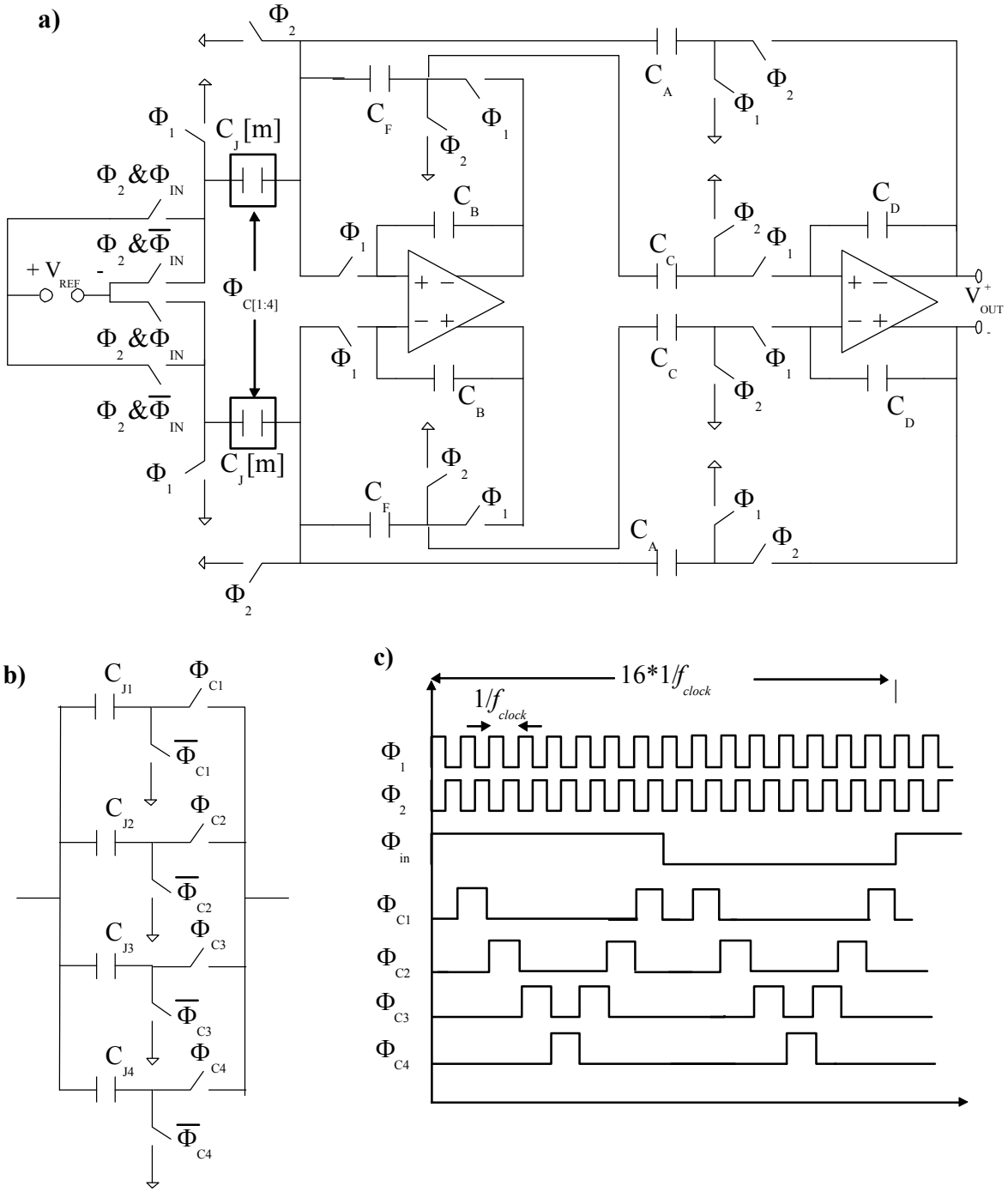

Figure 3: a) Schematic of the designed SC sinewave generator.
b) Input weigthed capacitor array $C_J[m]$.
c)Timing and control scheme

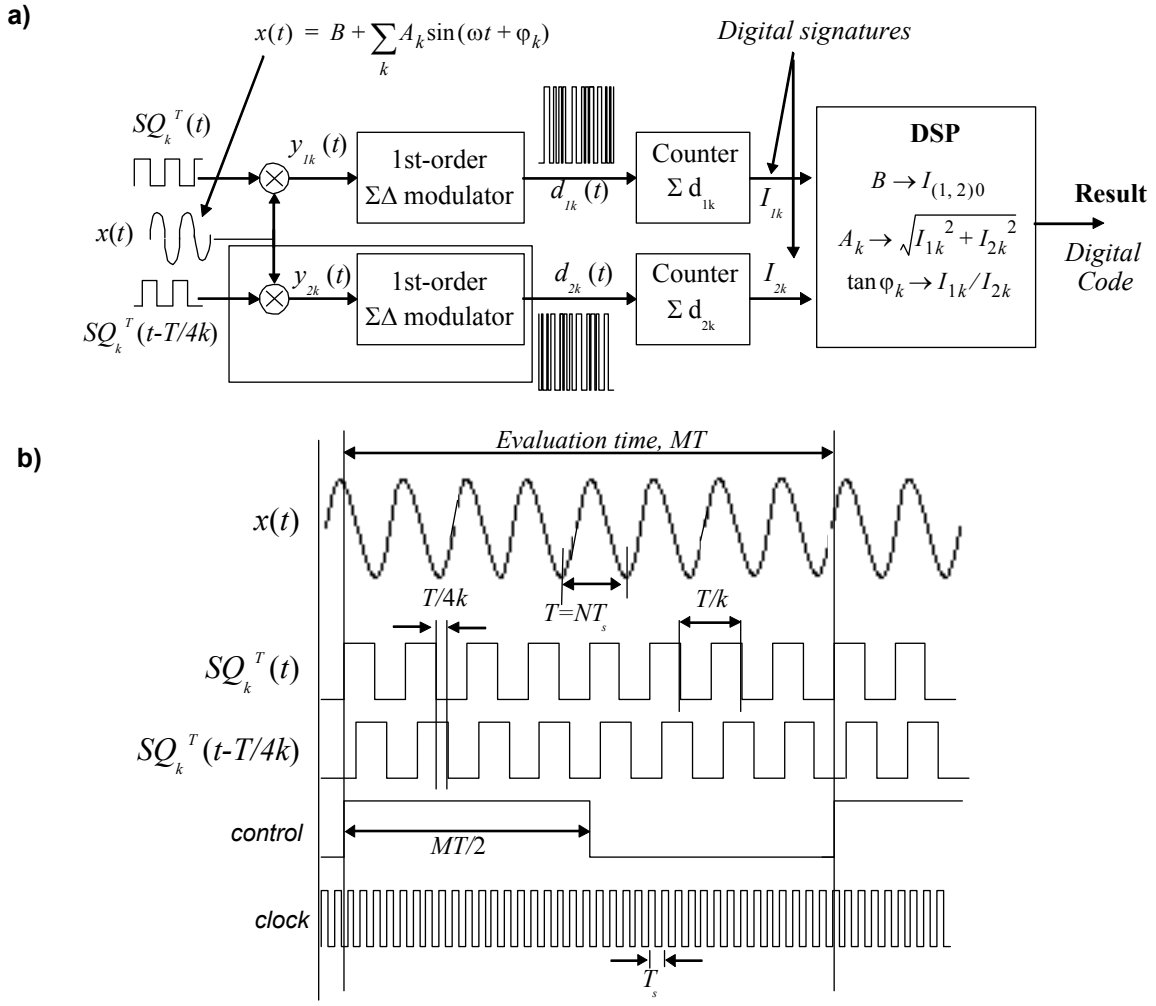

Figure 4: a) Block diagram of the signature extractor and signal processing for parameter extraction.
b)Timing scheme.

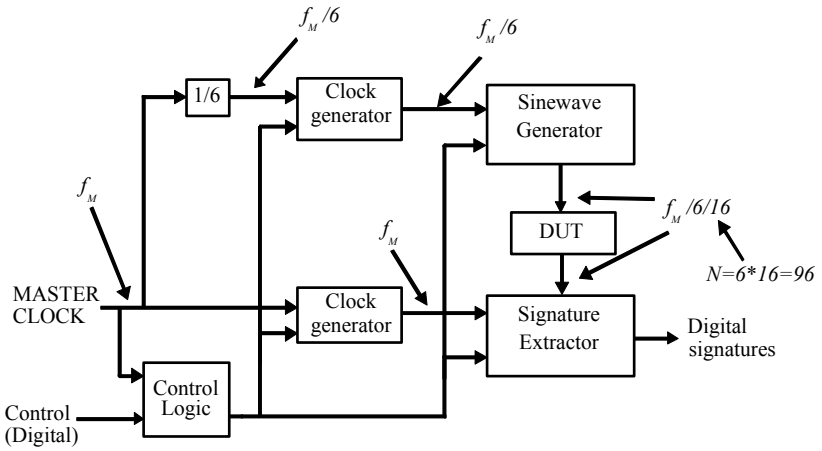

Figure 5: Example of synchronization between signal generation and evaluation in the system (oversampling ratio in the modulators, N=96).

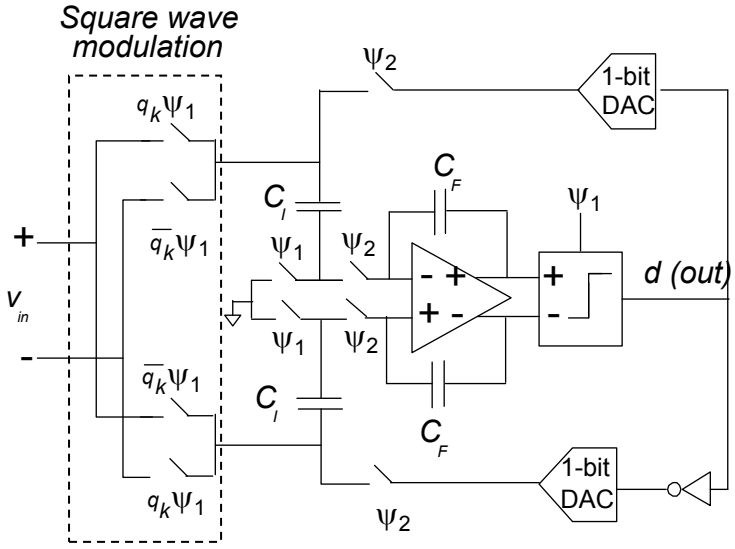

Figure 6: Schematic of the ΣΔ modulator with embedded square modulation in the input switching block

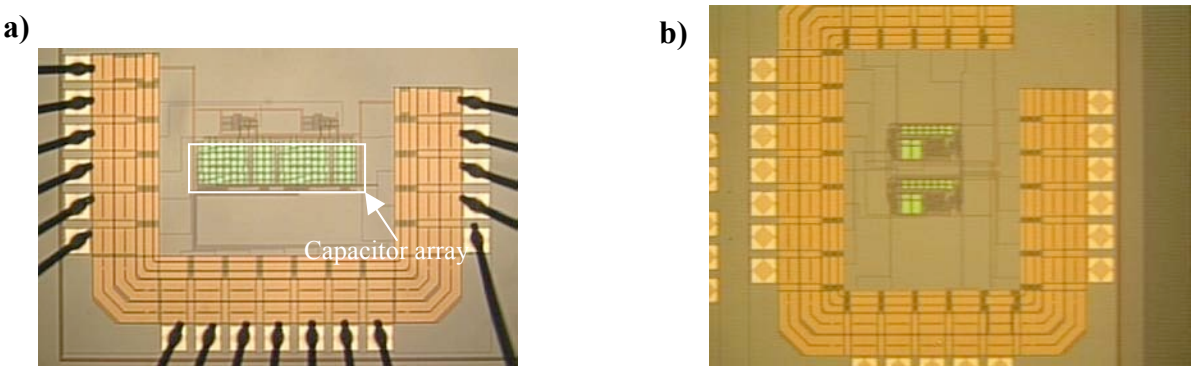

Figure 7: Microphotographs: a) Sinewave generator, b) Signature extractor.

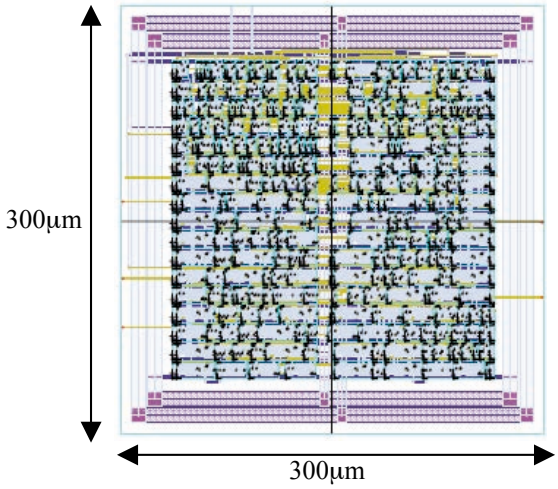

Figure 8: 16-bit word-length DSP circuitry synthesized from a VHDL description using standard cells in a 0.35µm CMOS technology.

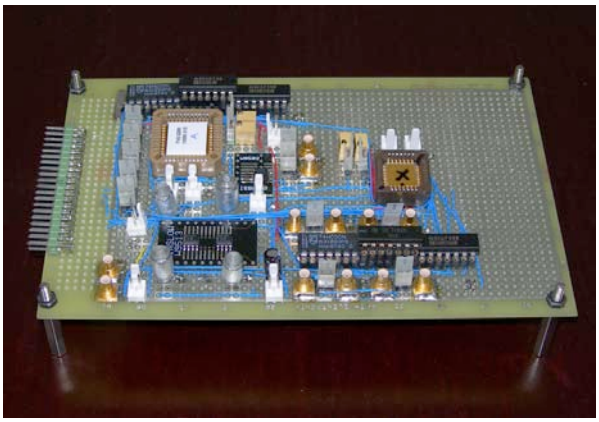

Figure 9: Demonstrator test board for the complete system.

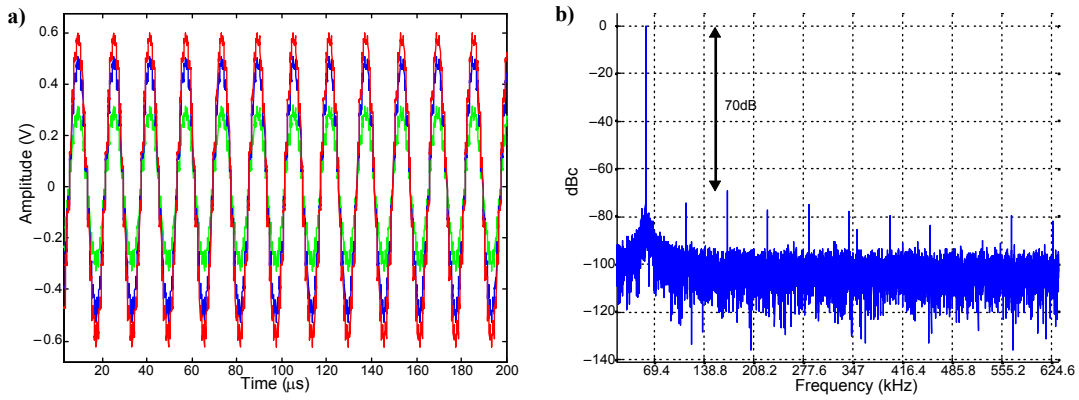

Figure 10: a) Generator output signals at 62.5kHz for V_{REF} = 150mV, 250mV, and 300mV.
b) Output spectrum for a 1Vpp signal at 62.5kHz.

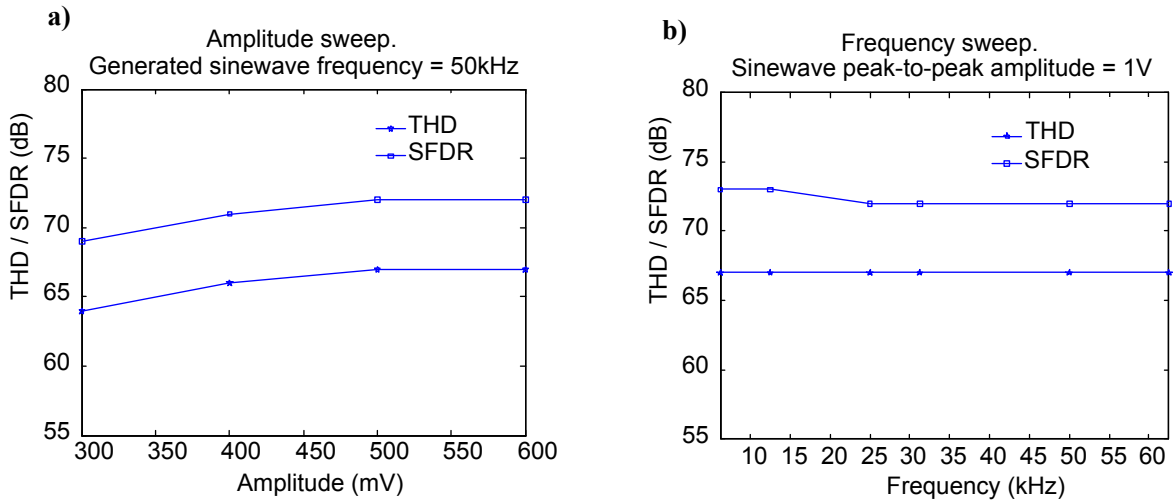

Figure 11: a) Generator output THD and SFDR as a function of the output amplitude.
b) Generator output THD and SFDR as a function of the output frequency.

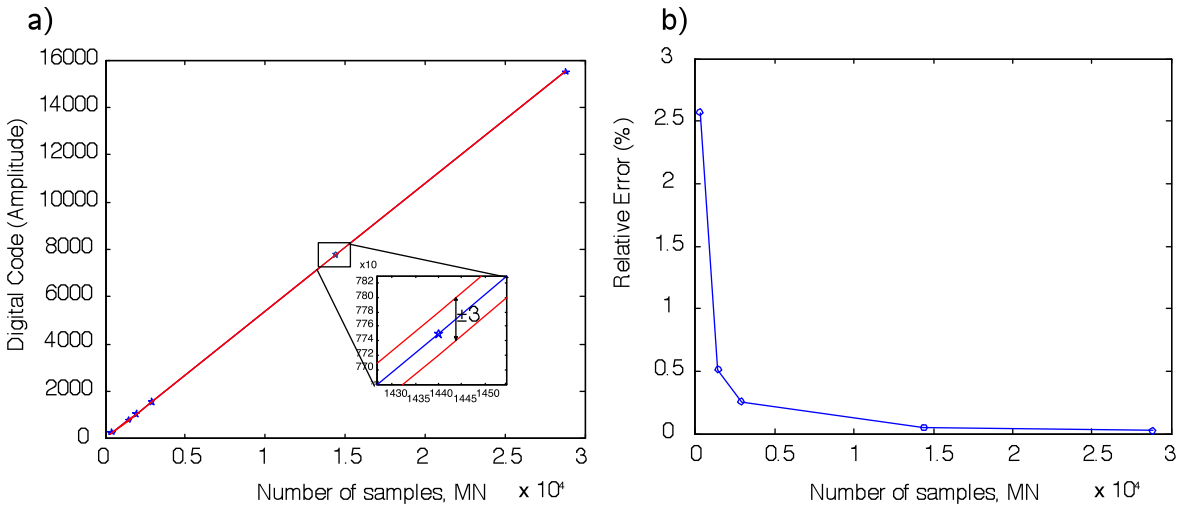

Figure 12: a) Obtained amplitude digital code vs. number of samples.
b) Relative error of the measurements vs. number of samples.

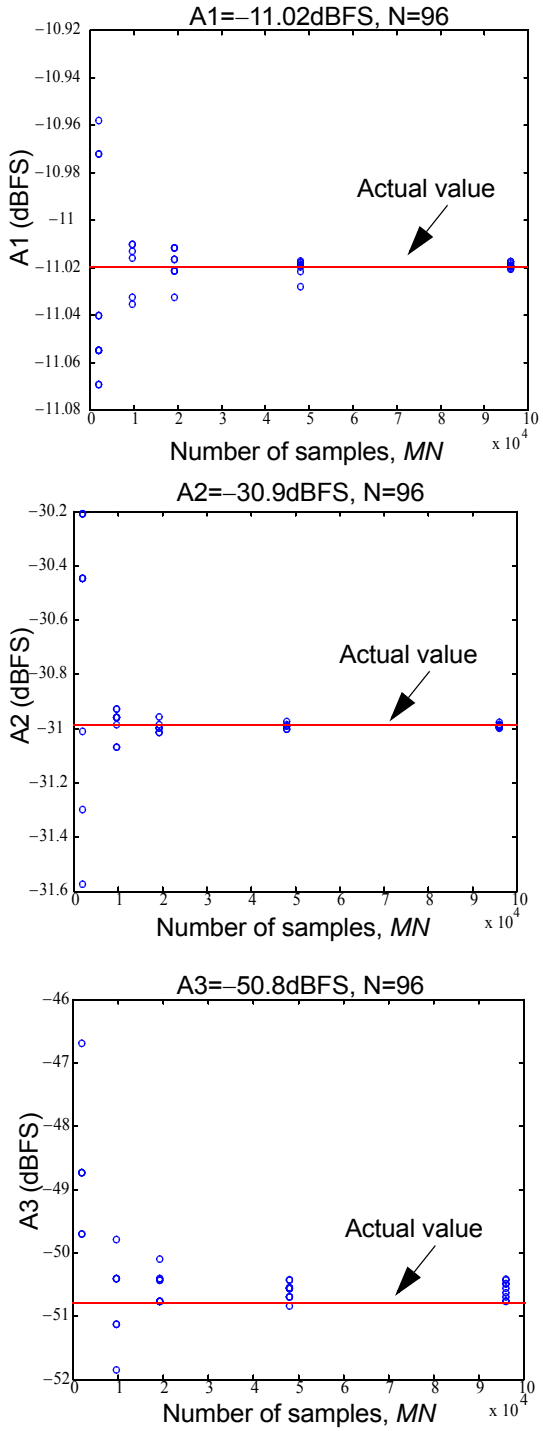

Figure 13: Harmonic component measurement as a function of the number of samples.

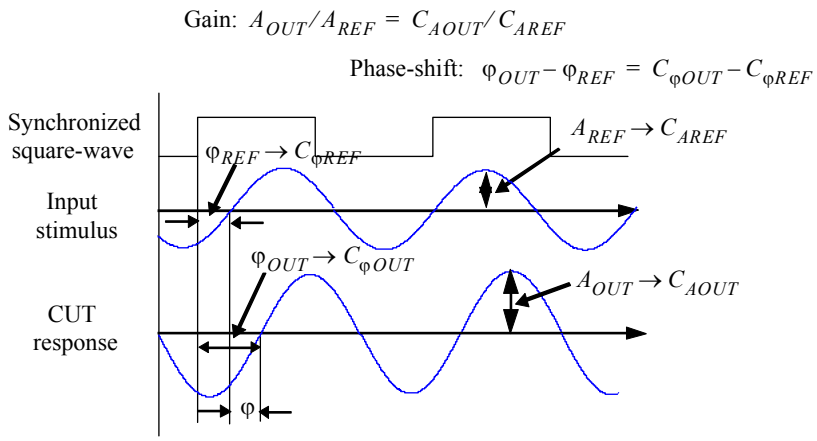

Figure 14: Protocol for frequency response characterization: gain and phase-shift extraction.

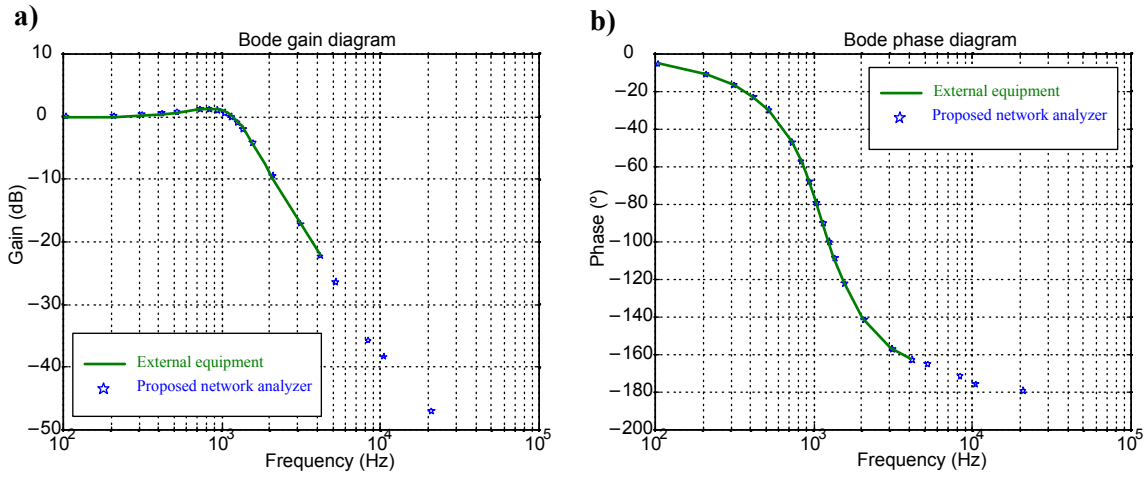

Figure 15: Measured Bode diagram: a) Magnitude response; b) Phase response

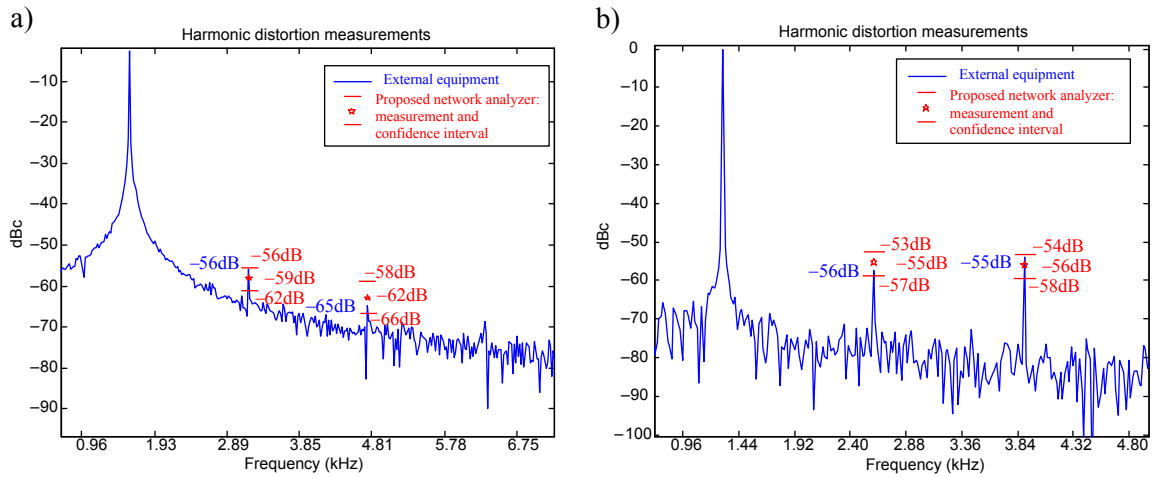

Figure 16: Harmonic distortion measurements: a) Main tone frequency = 1.6kHz; b) Main tone frequency =1.3kHz.

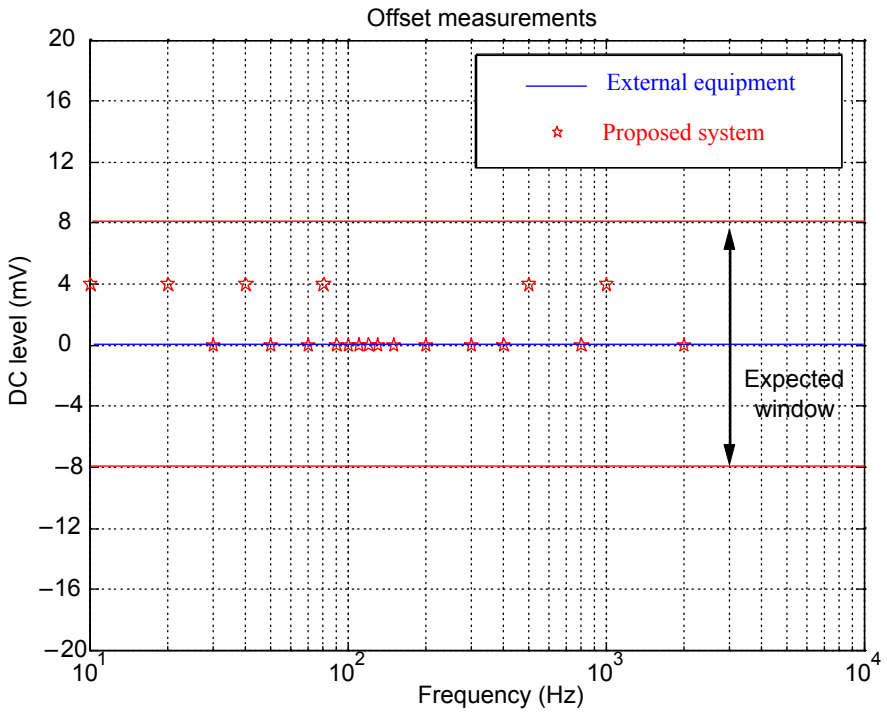

Figure 17: Offset measurements

Table I: Normalized capacitor values in the generator (Figure 3)

C_A	5.194	C_D	2.574
C_B	12.749	C_F	1.014
C_C	1	C_J	2

Table II: Current state-of-the-art in integrated analog test solutions

	Integrated mixed-signal test core [3]	**Frequency response characterization system [6]**	**SC spectrum analyzer [8]**	**FPGA-Based analog BIST [15]**	**This work**
Generation technique	Filtered ΣΔ-encoded arbitrary waveform	Continuous-time frequency synthesizer	SC variable gain amplifier	Direct digital synthesizer test pattern generator	Modified SC filter
Evaluation technique	Response capture through subsampling	Mixers plus amplitude and phase detectors	Programmable SC bandpass filter	Simplified digital spectral processing	ΣΔ-modulation and simple DSP
Measure capability	External processing required	Magnitude and phase of main tone	Magnitude response including harmonics	Magnitude and phase response including non-linearity (IP3) and Noise Figure measurements	Magnitude and phase response including harmonics and offset measurements
Demonstrated performance (dynamic range)	61dB@20kHz (20MSamples/s)	30dB@130MHz	40dB@10kHz	Limited by 8-bit A/D and D/A converters	70dB@62.5kHz (1MSamples/s)
Technology	0.35μm CMOS	0.35μm CMOS	0.5μm CMOS	FPGA + A/D and D/A converters	0.35μm CMOS
Area	0.67mm^2 (filter not included)	0.3mm^2	0.3mm^2	---	0.3mm^2 (DSP included)
Power	not reported	20mW	0.2mW	---	7mW