On Chopper Effects in Discrete-Time ΣΔ Modulators

Gildas Léger, Antonio Gines, Eduardo J. Peralías, and Adoración Rueda, *Senior, IEEE*

***Abstract*—Analogue to Digital converters based on ΣΔ modulators are used in a wide variety of applications. Due to their inherent monotonous behavior, high linearity and large dynamic range they are often the preferred option for sensor and instrumentation. Offset and Flicker noise are usual concerns for this type of applications and one way to minimize their effects is to use a chopper in the front-end integrator of the modulator. Due to its simple operation principle, the action of the chopper in the integrator is often overlooked. In this paper we provide an analytical study of the static effects in ΣΔ modulators, which shows that the introduction of chopper is not transparent to the modulator operation and should thus be designed with care.**

***Index Terms*—ΣΔ modulation, chopper, noise leakage, design.**

I. Introduction

With the ever decreasing feature size of silicon processes, digital circuits have been implementing more and more functionality. However, most applications require an interface to the real world. At some point, an analog-to-digital converter is thus necessary. Due to their relatively low analog complexity – because part of the conversion is realized in the digital domain by the decimation filter – ΣΔ converters are often the preferred architecture for high-resolution and low to medium frequency applications. These converters are inherently monotonous and usually exhibit high linearity. Although in the past few years continuous time ΣΔ modulators have been introduced to extend the market to higher frequency range, discrete time modulators – mainly based on switched-capacitor techniques – gather the major part of the instrumentation and audio market. These converters can reach very high resolutions (up to 24bits). At this level, any source of noise becomes a concern. This is particularly true at low frequency, where Flicker noise is a limiting factor. For sensor applications where calibration is not possible, the main concerns when using a ΣΔ converter may be Flicker noise, gain and offset errors. There are two main techniques that can be used to reduce offset and Flicker noise. These are correlated double sampling (CDS) and chopping [1].

It is well known that ΣΔ modulators are very sensitive to the non-idealities of the front-end integrator. Indeed, for the integrators located further in the loop, the perturbations induced by the non-idealities are partially modulated to the high frequencies and their contribution to the baseband error is minimal. CDS and chopping are thus applied only to the first integrator in the loop. It has also been proposed in [2] to apply chopper to the complete modulator. This requires designing a high-pass modulator, which is a fundamental and challenging architectural change. For this reason this solution has remained marginal.

Beyond offset and Flicker noise suppression, CDS technique based on Nagaraj's integrator [3], [4] has the advantage of relaxing amplifier DC gain requirements. The use of such an integrator in ΣΔ modulators has been contemplated in [5]. In [6] a noise analysis of the integrator is performed, which shows that the input capacitance of the amplifier should be minimized to effectively cancel Flicker noise contribution. Despite the important benefits of this integrator structure, its use in ΣΔ modulators is not generalized because it requires specific and careful design.

On the other hand, chopping seems to be a much more straightforward approach. Apparently, it can be included in an existing integrator design with little effort. As a matter of fact, the papers describing modulators that include chopping seldom detail chopper implementation and its possible impact on performance [7]–[9]. Neither do reference textbooks [10], [11] or studies on non-ideality modeling [12], [13]. In a recent paper [14], the authors propose to use a pseudorandom chopping sequence and extend the results of [1] to estimate the residual offset due to switch charge injection.

This paper studies the chopper static effects in the front-end integrator of ΣΔ modulators, and will show that chopper implementation is not as straightforward as it seems.

The paper is organized as follows: Section 2 is devoted to the chopper operation in the integrator. A high-level event-driven model is proposed and validated. Section 3 provides a detailed study of chopper effects in ΣΔ modulators. Section 4 points out the peculiarity of high-level simulations. Section 5 presents transistor level simulations that validate the analytical study and Section 6 provides some practical considerations for the designer to account for the referred effects. Finally Section 7 summarizes the paper conclusions.

II. The chopped integrator

Two main implementations of the chopped integrator can be found in the literature. The first and most direct one consists in flipping the amplifier by adding crossed switches in series at its inputs and outputs, as illustrated in Fig.1-a. In that way, the

This work has been partially funded by the Spanish Government project TEC-2007-68072 and the CSIC project 200850I213.

The authors are with the Instituto de Microlectrónica de Sevilla, Centro Nacional de Microelectrónica, Consejo Superior de Investigaciones Científicas (CSIC) and Universidad de Sevilla, 41012 Sevilla, Spain.

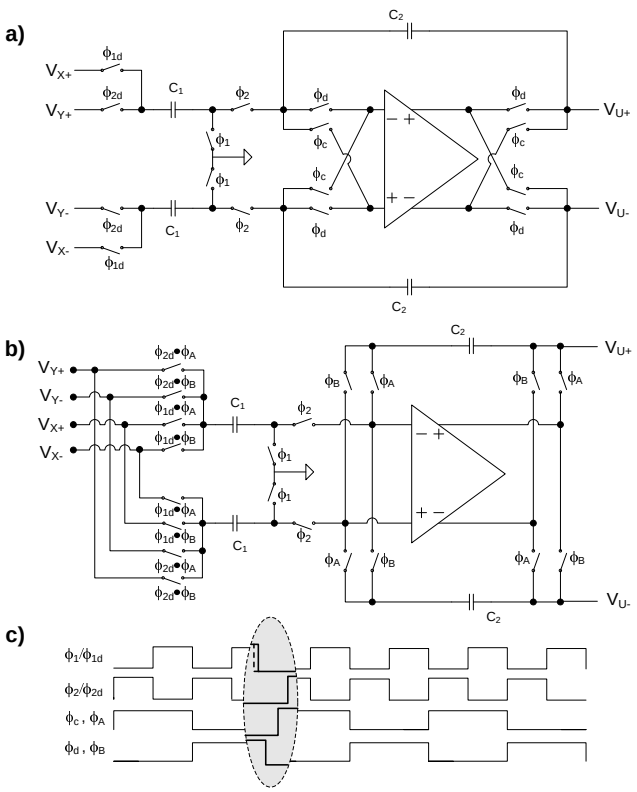

Fig. 1. a) Diagram of a single-branch integrator with a chopped amplifier. b) Diagram of a chopped integrator, where the chopping is implemented on the feedback capacitors and the integrator input. c) Integrator clock phases.

noise and offset introduced by the amplifier are modulated by the chopper signal. The chopper transitions (controlled by ϕ_c and ϕ_d) occur in the interphase between ϕ_1 and ϕ_2 as shown in Fig.1-c. For this implementation, the chopper transitions could also be located during the sampling phase ϕ_1 to limit additional noise sampling as proposed in [8]. However, the amplifier would have less time to properly settle and this may induce a signal-dependent error, particularly if the next integrator also samples on phase ϕ_1.

In the second implementation of the chopped integrator [15], represented in Fig.1-b, the integrating capacitances are flipped instead of the amplifier, which also requires to apply the chopper to the integrator inputs. The first order results are identical to those of the first implementation. The main difference between the two schemes actually lies in dynamic settling requirements that have no contribution to the static behavior.

For a classical integrator without chopping (consider $\phi_c = 1$ and $\phi_d = 0$ in Fig.1-a), the contribution of the amplifier offset V_{off} to the integrator output V_U can be calculated as,

$$V_U \approx \frac{b\left(1-\frac{b+1}{A}\right) z^{-1}\left(V_{in}-V_{off}\right)}{1-z^{-1}\left(1-\frac{b}{A}\right)} \qquad (1)$$
$$V_{in} = V_X - V_Y$$

where $b = C_1/C_2$ and A is the amplifier DC gain.

For a chopped integrator, it is usual to consider that the offset term V_{off} in (1) is simply replaced by its modulated

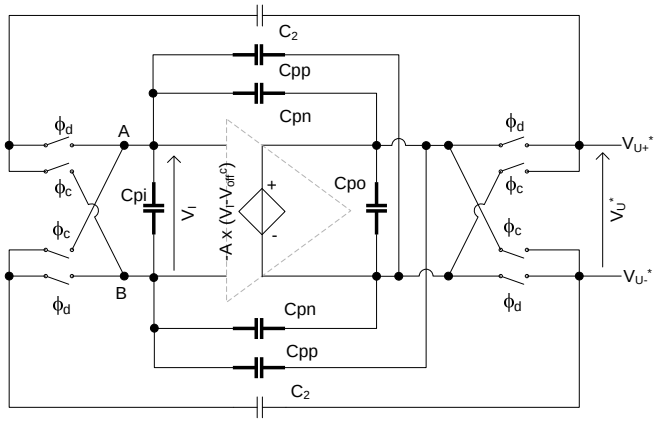

Fig. 2. Integrator schematic during a chopper transition, including the parasitic capacitors on the amplifier.

version V_{off}^c. We have,

$$V_{off} \rightarrow V_{off}^c = V_{off} * CH\left(z\right) \qquad (2)$$

where $CH\left(z\right)$ is the z-transform of the two-valued chopping sequence $ch\left(n\right)$ (either 1 or -1) that represents the amplifier flipping action controlled by phase ϕ_c and phase ϕ_d.

A. Effect of chopper transitions

Let us consider the instant at which the chopper flips the signal paths, in other words a rising or a falling edge of the chopper signal. This chopper transition occurs in the interphase between ϕ_2 and ϕ_1. As both phases are low, the connection to the sampling capacitors is open and the two architectures represented in Fig.1 reduce to the same case study with respect to chopping effects. The integrator schematic during a chopper transition is shown in Fig.2. The parasitic capacitors that may affect the integrator operation during a chopper transition have also been represented. There is an input capacitor C_{pi}, an output capacitor C_{po}, a positive feedback capacitor C_{pp} and a negative feedback capacitor C_{pn}. For these last two capacitors, a differential contribution is considered for the sake of simplicity. Indeed, if the parasitic occurs on a single branch it will affect both the common-mode and the differential signal. The differential contribution can be calculated taking one half of the single branch capacitor value.

Neglecting settling and charge injection mechanisms in the switches, it is obvious that the output capacitor C_{po} has no effect since it is connected to a voltage source. The charge conservation equations at nodes A and B in Fig.2 lead to the modified integrator output V_U^* after a chopper edge,

$$V_U^* = \frac{\left[1+\frac{C_{pp}-C_{pn}}{C_2}+\frac{1}{A}\left(1-\frac{C_{pp}+C_{pn}+C_{pi}}{C_2}\right)\right] V_U - 2V_{off}^c}{1-\frac{C_{pp}-C_{pn}}{C_2}+\frac{1}{A}\left(1-\frac{C_{pp}+C_{pn}+C_{pi}}{C_2}\right)} \qquad (3)$$

where V_U is the integrator output before the chopper edge, given by (1).

Equation (3) can be simplified by neglecting the terms divided by A and considering the offset term small with respect to the integrator output range. In this way and considering

parasitic capacitances smaller than C2, a first order Taylor development of (3) gives,

$$V_U^* \approx (1+\delta)\, V_U - 2V_{off}^c \qquad (4)$$
$$\delta = 2\frac{C_{pp} - C_{pn}}{C_2}$$

Hence, each time that the chopper flips the amplifier, the integrator output voltage will be slightly scaled up or down (depending on the value of C_{pp} and C_{pn}). This is not the case in an integrator without chopper since these parasitic capacitors simply add up to the feedback capacitor C_2, and would appear as an integrator gain error similar to the conventional capacitor mismatch.

The presence of an offset in the amplifier imbalances the virtual grounds, and the charge required to recover the equilibrium (which has to be drawn from the feedback capacitor C_2) modifies the integrator output. There is thus an offset component related to the chopper transitions, in addition to the conventional one already shown in (2). It can be seen in (3) that the parasitic capacitors also modify the coefficient of this offset contribution. However, for low offset values this can be considered as a second order effect.

B. A high-level model of the chopped integrator

We have seen above that beyond the classical chopper modulation effect, there are two spurious contributions to the integrator output that are related to chopper transitions (i.e. the amplifier flipping events). One is an additional offset contribution and the other is a parasitic contribution that modulates the integrator output. These two contributions add to the output samples following a flipping event.

In order to validate (4), we performed transistor-level simulations of an integrator designed in AMS $0.35\mu m$ technology. The gain of the integrator is $b = 0.5$.

First of all, a 10mV voltage source has been introduced in series with one of the amplifier inputs. We performed three transient simulations for three different values of the chopper frequency $f_{ch} = f_s/(2M)$: M=1, M=2 and M=5. The integrator input was set to 0 to see only the offset contribution at the integrator output. Fig.3 displays the obtained results. It can be seen that the integrator output follows the expected behavior: the offset is modulated by a square wave and integrated, but we can also see a component due to the chopper transitions. The classical chopper component, as described in (1) and (2), leads to a step at the integrator output at each sample period of,

$$step_{CH} = b \times V_{off} = 0.5 \times 0.01V = 0.005V \qquad (5)$$

While the transition component, as expressed in (4), leads to an additional increase of,

$$step_{CT} = 2 \times V_{off} = 2 \times 0.01V = 0.02V \qquad (6)$$

This component has to be summed to the classical one, that is why a positive or negative step of $0.025V$ is observed at each chopper transition, for the three chopper frequencies. Notice that the first transition must not be taken into account

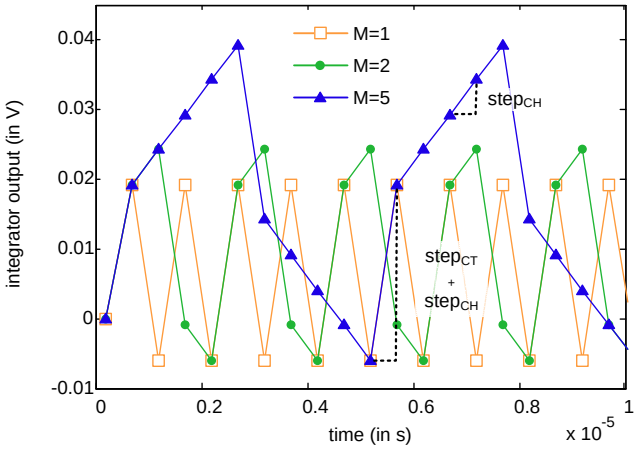

Fig. 3. Integrator output for a 0V input in the presence of a $10mV$ amplifier offset. The transient simulation has been realized for three different chopper frequencies $f_{ch} = f_s/(2M)$: M=1, M=2 and M=5.

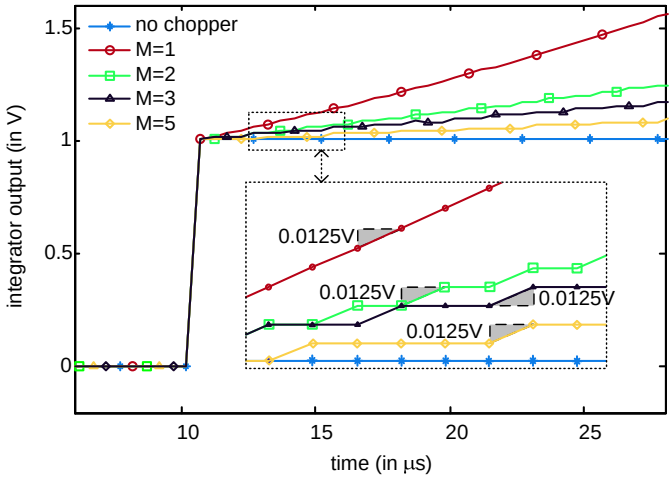

Fig. 4. First integrator impulse response for different chopper frequencies.

because it corresponds to the integrator initial state for which the feedback capacitors are discharged and thus do not hold the offset value.

In order to validate the second spurious contribution (the effect of parasitic capacitors during chopper transitions), the offset has been set to 0 and a positive feedback capacitor has been introduced around the first amplifier ($C_{pp} = 10fF$ in Fig.2). The feedback capacitance C_2 is made of four unit capacitors of $400fF$. Accordingly to (4) we have,

$$\delta = 2\frac{10 \times 10^{-15}}{4 \times 400 \times 10^{-15}} = 0.0125 \qquad (7)$$

The integrator response to a $V_{in} = 2V$ impulse has been simulated. For an ideal integrator of gain $b = 0.5$, the response should be a step signal of $1V$. Amplifier finite DC gain will produce a slow decay of the integrator output, while chopper parasitic effect should give rise to periodic incremental steps of $\delta b V_{in}$ for each chopper transition.

Fig.4 shows the impulse response obtained for five different cases: in the absence of chopper and for a chopper at $f_s/2$, $f_s/4$, $f_s/6$ and $f_s/10$ (i.e. $M = 1, 2, 3, 5$).

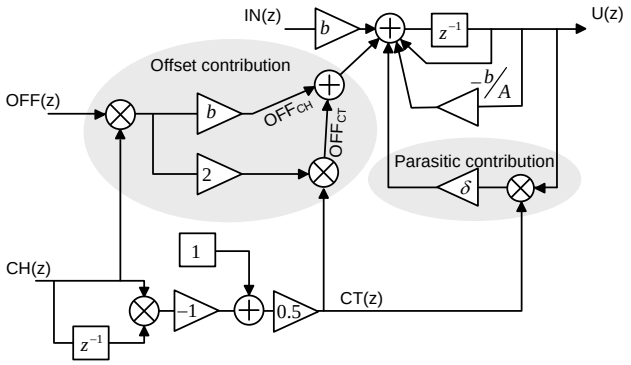

Fig. 5. High level model of a chopped integrator for event-driven simulators, including chopper transition effects.

It can be clearly appreciated how the integrator output is increased by the effect of chopper and that the incremental steps occur every 1, 2, 3 and 5 samples as expected. The increments are also of the expected value: $\delta b V_{in} \approx 0.0125V$. The step value actually increases as the integrator output increases from its initial value of $bV_{in} = 1V$. For the integrator without chopper there is actually a slight decrease of $-4 \times 10^{-5}V$ that corresponds to the pole error induced by the amplifier finite DC gain.

These electrical simulations show that the chopped integrator behaves as predicted by (4), and hence we can use this equation to build a high level event-driven model to facilitate further investigations on the impact of chopped integrators on discrete-time signal processing circuits, such as $\Sigma\Delta$ modulators.

To build this model, we need to analytically define the chopper transition signal. Let us consider the chopper signal, $ch(n)$ as a two valued signal (1 and -1). On other hand, the chopper transition signal, $ct(n)$, must be equal to 1 for the sample immediately following a chopper rising or falling edge, and 0 elsewhere. This signal can be built from the chopper signal as,

$$ct(n) = (1 - ch(n)ch(n-1))/2 \tag{8}$$

The chopped integrator model based on the modulation effect described in (4) can thus be built as shown in Fig.5.

Signal IN is the integrator input and U is its output. We can readily separate the two spurious contributions highlighted in (4) at the summing node of the integrator: one related to the offset and the other to the integrator output modulation due to the parasitic capacitors. To generate the former, signal OFF accounts for the offset and Flicker noise of the amplifier. It is multiplied by the chopping sequence CH to generate the classical chopper component (OFF_{CH}) and also by the chopper transition signal CT to generate the chopper transition component (OFF_{CT}). To generate the latter, the integrator output U is modulated by the chopper transition signal and scaled by the parasitic factor δ.

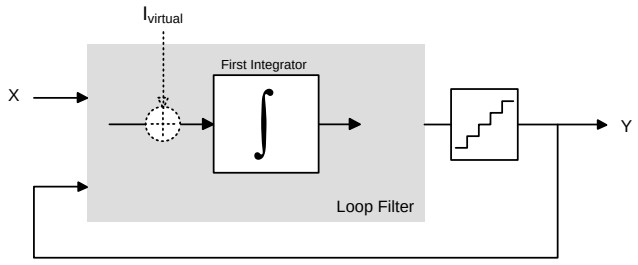

Fig. 6. Generic loop filter for $\Sigma\Delta$ modulator.

III. Chopper impact on $\Sigma\Delta$ modulator performance

A. Referring chopper effects to the modulator output

Let us consider the generic $\Sigma\Delta$ modulator in Fig.6. Due to their non-linear dynamics, the analytical resolution of $\Sigma\Delta$ modulators is particularly involved, even for simple inputs like DC levels [10]. However, a simple approximation is often used in order to evaluate the performance of different architectures. This approximation consists in replacing the quantizer by a noise source that emulates the quantization error. In that way, linear algebra can be used to calculate the Signal Transfer Function (STF) of the modulator as well as its Noise Transfer Function (NTF), which defines the noise shaping capability of the structure.

The modulator output Y is thus related to the input signal X and the quantization error E through,

$$Y = STF(z)\,X + NTF(z)\,E \tag{9}$$

Let us consider a virtual signal $I_{virtual}$ that would add up at the first integrator input, as shown in Fig.6. In the frame of the linearized quantizer approximation, it is possible to calculate the transfer function $TI(z)$ of this new signal to the modulator output such that,

$$Y = STF(z)\,X + NTF(z)\,E + TI(z)\,I_{virtual} \tag{10}$$

In most cases of the widely used CIFB structure (Cascade of Integrators with FeedBack) described in [11], the modulator input signal feedforward coefficients are all set to zero except the first one. As a consequence, a signal added at the integrator input is equivalent to a signal added at the modulator input and thus sees the modulator $STF(z)$,

$$TI(z) = STF(z) \tag{11}$$

For the sake of conciseness, we will further drop the (z) part in the expression of the different z-transforms.

Ideally, the modulator STF must not significantly filter the input signal in the baseband of the converter. As a matter of fact, in an ideal $\Sigma\Delta$ modulator, the STF reduces to a fixed delay. Hence, with respect to power in the baseband, the term TI can be neglected. For other architectures than the CIFB, the calculation of TI with the linearized quantizer approximation is an easy task and the same approximation is likely to be valid.

Using the high level model that we have validated in the previous section (see Fig.5), it is quite straightforward to refer the chopper-related signals at the integrator input, and

therefore at the modulator output (taking into account the integrator gain b). As explained above, there are two distinct contributions: one is the offset and Flicker noise contribution (OFF_{chop}), and the other is a modulation of the integrator output due to the parasitic coupling between the amplifier inputs and outputs (P_{ert}).

The offset contribution can be calculated as,

$$\begin{aligned} OFF_{chop} &= TI \times \frac{OFF_{CH} + OFF_{CT}}{b} \\ &= TI \times \frac{b\,OFF * CH + 2\,OFF * CH * CT}{b} \end{aligned} \tag{12}$$

where we have separated the classical chopper component OFF_{CH} and the chopper transition component OFF_{CT}. For the sake of simplicity, we consider both amplifier Flicker noise and offset in the term OFF.

The parasitic contribution is written as,

$$P_{ert} = TI \times \frac{\delta}{b}\left[U_1 * CT\right] \tag{13}$$

where U_1, the z-transform of the first integrator output, is modulated by the chopper transition signal CT.

Let us study separately the impact of these two perturbations.

B. Offset and $1/f$ noise contribution

Obviously, the chopper transition signal $ct(n)$ is quite different from the chopper signal $ch(n)$. Let us study how it modifies offset and Flicker modulation. It is important to remark that the chopper transition component (OFF_{CT} in Fig.5) is multiplied by both the chopper signal (ch) and the chopper transition signal (ct). We have,

$$\begin{gathered} off_{ct}(n) = 2off(n) \times ch(n) \times ct(n) \\ \Updownarrow \\ OFF_{CT} = 2OFF * CH * CT \end{gathered} \tag{14}$$

The spectrum of the chopper transition signal cannot be known *a-priori* but it is deterministically linked through (8) to the chopper signal. This introduces a direct simplification. Because $ch(n)$ is a square signal between 1 and -1, we have $ch(n)^2 = 1$, which leads to,

$$\begin{aligned} off_{ct} &= 2off(n) \times ch(n) \times ct(n) \\ &= off(n) \times (ch(n) - ch(n-1)) \\ &\Updownarrow \\ OFF_{CT} &= OFF * \left[\left(1 - z^{-1}\right) CH\right] \end{aligned} \tag{15}$$

Hence, the total chopped offset and Flicker noise contribution referred to the modulator output, as shown in (12), simplifies to,

$$OFF_{chop} = TI \times OFF * \left[\left(\frac{1 + b - z^{-1}}{b}\right) CH\right] \tag{16}$$

Depending on the chopping signal nature, the frequency shaping related to the chopper transition contribution can be more or less relevant. As an example, [16] proposes to use a frequency-shaped pseudo-random chopper signal. A white sequence from an LFSR is sent to a simple digital modulator whose transfer function has a zero at DC and another at $f_s/2$. The first one minimizes the power in the baseband while the second one limits possible coupling of high-frequency tones on the full-scale voltage references. We generate such a sequence in Matlab and use it in our model to examine the impact of the chopper transition signal. Without much loss of generality, we neglect the filtering action of the architecture-specific term TI, as discussed above.

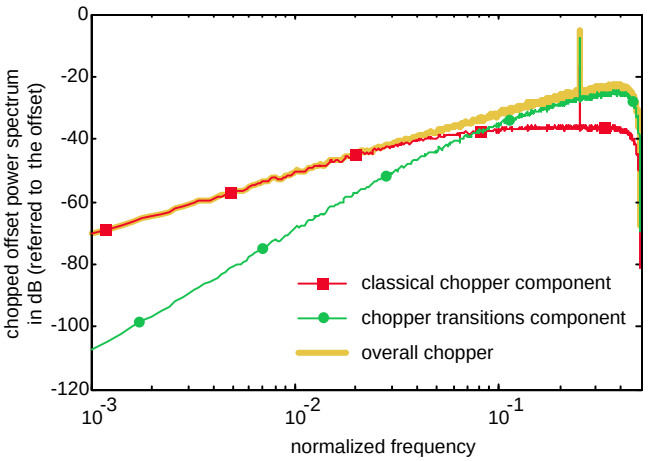

Fig. 7. Chopper effect on the offset, including classical chopper component and chopper transition component. The chopper is a pseudo-random sequence shaped as defined in [16].

Fig.7 shows the chopped-offset spectrum normalized to the offset power. A total of 100 spectrums computed over 2048 samples have been averaged in order to reduce variability. The FFTs were calculated using a high performance window (a Rife-Vincent type-2 window, with 165dB side-lobe attenuation [17]) to avoid any spectral leakage. Together with the overall result (the thick line), we have represented the classical chopper component (with square markers) and the chopper transition component (with round markers). The shaping effect on the latter can clearly be appreciated. At low frequency, the classical chopper component dominates the noise spectrum. At high frequency, the chopper transition component significantly increases the noise power level. In particular, the power density at $f_s/2$ is 14dB higher than expected from the classical chopper component.

If Flicker noise is the main concern, the signal OFF in (16) cannot be considered as a scalar. Actually, its power spectral density is of the form,

$$S_{OFF} \propto \frac{1}{f} \tag{17}$$

and the analytical resolution of the convolution in (16) is not straightforward.

To illustrate its effect, Fig.8 shows the chopped-Flicker spectrum in the same way as in Fig.7. The power spectrum of the Flicker noise without chopper is also represented in order to illustrate the benefits of chopping. It can be seen how chopping effectively brings a reduction of Flicker noise power at low frequency. As expected, the zeros at DC and $f_s/2$ that

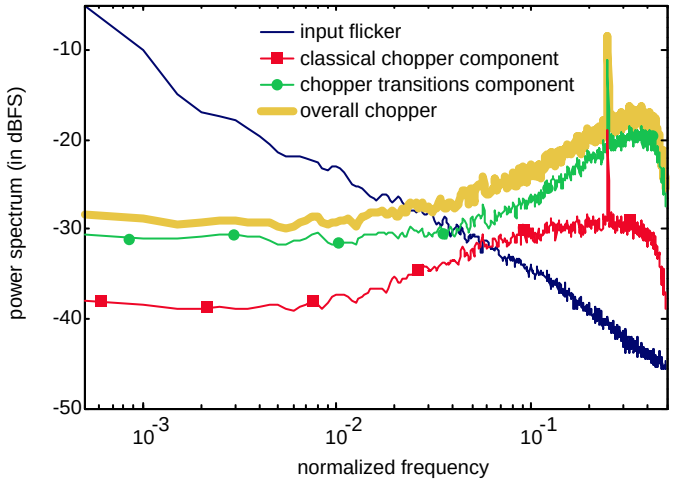

Fig. 8. Effect of chopper transitions on the spectrum of the chopped Flicker noise referred at the integrator input. The chopper is a pseudo-random sequence shaped as defined in [16].

could be seen in Fig.7 for a DC offset are significantly filled by Flicker noise aliasing.

In significant contrast to the DC offset case, it can be seen that the chopper transition component dominates over the classical chopper component on the entire spectrum and not only at high frequency. In particular the power spectral density of the overall chopped Flicker noise is close to 10dB higher than what could be expected with a simple model at low frequencies. This increment is significant and should thus be taken into account during the design phase in order to define a correct design margin for the amplifier Flicker noise, which directly impacts on the minimum size of its input transistors.

C. Parasitic contribution

This section analyzes the impact of the parasitic capacitors that modulate the integrator output, as introduced in (13).

In order to go further in the analysis, we need to develop the terms TI, U_1 and CT. The first two depend on the particular architecture of the $\Sigma\Delta$ modulator. The first integrator of $\Sigma\Delta$ modulators is usually fed with the difference between the input signal and the output bitstream. Taking (9) into account, the output of the integrator (U_1) can thus be written,

$$U_1 = \frac{bz^{-1}}{1-z^{-1}}\left(\left(1-STF\left(z\right)\right)X - NTF\left(z\right)E\right) \tag{18}$$

For the sake of simplicity, in what follows we will consider the case study of an architecture that implements an ideal L^{th} order modulator such that,

$$\begin{aligned} STF\left(z\right) &= TI\left(z\right) = z^{-L} \\ NTF\left(z\right) &= \left(1-z^{-1}\right)^{L} \end{aligned} \tag{19}$$

In this case, the expression of the perturbation (13) can be written as,

$$\begin{aligned} P_{ert} = \delta z^{-L} \times \left[CT * \left(\left(\sum_{i=0}^{L-1} z^{-i}\right)X\right)\right] \\ -\delta z^{-L} \times \left[CT * \left(z^{-1}\left(1-z^{-1}\right)^{L-1}E\right)\right] \end{aligned} \tag{20}$$

From this equation, it can be seen that the perturbation has a signal-dependent term and a noise-dependent term.

For any particular architecture, TI and U_1 should be calculated, but the perturbation will likely be similar to (20); that is, a signal and a noise contribution modulated by the chopper transition signal.

As both noise and signal are convoluted by the chopper transition signal CT, its spectrum is particularly relevant to understand the impact of the chopper parasitics. Up to this point, the type of chopper signal (and consequently the chopper transition signal) has not been specified. Let us consider three cases.

1) Chopping at $f_s/2$: When the chopper frequency is set to half the sampling frequency, the amplifier is flipped at each period. All the samples will get the chopper transition contribution. As a result the chopper transition signal is,

$$CT\left(z\right) = 1 \tag{21}$$

Hence, the signal and noise contributions of the perturbation are not modulated. While the signal contribution simply adds up to the nominal signal, the noise contribution will degrade performance. It can be seen from (20) that some quantization noise shaped at order $L-1$ will leak into the baseband.

For this particular case, it is interesting to come back to the integrator level expression given in (4). Indeed, as a chopper transition occurs at each period, the chopper parasitic contribution appears as a pole error, just like the effect of amplifier finite DC gain. The impact of a pole error in the first integrator on the modulator performance is well known [10], [12]. It is important to notice that, unlike for the amplifier DC gain, the sign of the chopper induced pole error depends on the parasitic capacitances. This can be particularly relevant for stability concerns [18].

The expected power spectral density S_{pert} of the noise term of the perturbation can be calculated analytically. For that, we have to develop the squared modulus of the second term in (20). Under Bennett's conditions, the quantizer error E can be approximated to a white noise of power spectral density,

$$S_E = \frac{\Delta^2}{12f_s} \tag{22}$$

where Δ is the quantizer step and f_s the sampling frequency. It comes,

$$S_{pert} = 2\delta^2\frac{\Delta^2}{12f_s}\left(1-cos\left(2\pi\frac{f}{f_s}\right)\right)^{L-1} \tag{23}$$

This coincides with the classical result obtained for integrator pole error in single stage $\Sigma\Delta$ modulators [10].

2) Chopping at lower frequencies: It is often recommended as a good design practice to isolate the voltage references that define the modulator full-scale from any signal at $f_s/2$, [10]. Such a coupling would likely demodulate high power tones from the quantization error into the baseband. Hence, one could operate the chopper at a frequency lower than $f_s/2$ in order to avoid the introduction of a clock signal at $f_s/2$, like for instance in [7]. However, if the chopper is operated at frequencies lower than $f_s/2$, the chopper transition signal is no longer constant and noise folding occurs.

Let us consider a chopper frequency of $f_s/(2M)$, where M is an integer higher than 2. In order to avoid harmonics at $f_s/2$, M should also be odd, but our study is valid for both odd and even values. The chopper transition signal defined above is thus of the form,

$$\begin{aligned} ct\left(n\right) &= 1 \ for \ n = kM \ with \ k \in \aleph \\ &= 0 \ otherwise \end{aligned} \tag{24}$$

Calculating $CT(z)$ from the definition of the z-transform is not straightforward. Instead, we can remark that multiplying the integrator output by the chopper transition signal is equivalent to downsample and then upsample by a factor M. Such a combination is widely used in multirate analysis and we can thus build on these results.

According to [19], the z-transform of the integrator output multiplied by the chopper transition signal can be written as,

$$CT\left(z\right) * U\left(z\right) = \frac{1}{M}\sum_{k=0}^{M-1} U\left(ze^{j\frac{-2k\pi}{M}}\right) \tag{25}$$

The perturbation spectrum (13) can thus be expressed as a sum of the integrator output spectrum components shifted by kf_s/M. This aliasing is due to the downsampling, while the scaling by $1/M$ is due to the upsampling.

To go further and describe the impact of the perturbation in a better way, we can consider an ideal L^{th} order CIFB modulator, which is what led us to (20). In this case, the perturbation can be written as,

$$\begin{aligned} P_{ert} = &\frac{\delta}{M} z^{-L} \sum_{k=0}^{M-1} \left(\sum_{i=0}^{L-1} z^{-i} X\right)_{z\to ze^{-j2\pi\frac{k}{M}}} \\ &-\frac{\delta}{M} z^{-L} \sum_{k=0}^{M-1} \left(z^{-1}\left(1-z^{-1}\right)^{L-1} E\right)_{z\to ze^{-j2\pi\frac{k}{M}}} \end{aligned} \tag{26}$$

The first term shows that the perturbation contains aliases of the modulator input signal around the frequencies kf_s/M. Taking into account that in the majority of cases, the modulator OSR is much higher than the modulator order L, the input signal X can be considered as a low-frequency and we can make the following approximation,

$$OSR >> L \Rightarrow \sum_{i=0}^{L-1} z^{-i} X \approx LX \tag{27}$$

Furthermore, for moderate values of M the input signal bandwidth is also likely to be inferior to $f_s/(2M)$ and thus, no overlapping of the aliases should occur. In this case, the power spectrum of the perturbation signal part can be easily calculated as,

$$S_{sig} = \left(\frac{\delta L}{M}\right)^2 \sum_{k=0}^{M-1} \left\| X\left(ze^{-j2\pi\frac{k}{M}}\right)\right\|^2 \tag{28}$$

If the OSR of the modulator is large, the signal aliases should be correctly suppressed by the decimation filter, and its impact on the modulator performance should be limited. However, $\Sigma\Delta$ modulators are often touted for their low anti-aliasing requirements. If high frequency and high power tones were present in the modulator input signal, they could leak into the baseband. This part of the perturbation should thus not be completely overlooked.

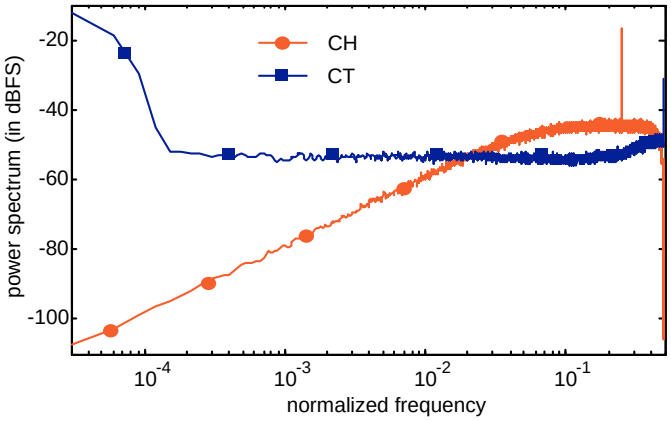

Fig. 9. Power spectra of the chopper signal (CH) proposed in [16], and of its associated chopper transition signal (CT).

The second term in (26) is related to the modulator quantization noise. Considering that the aliases of the quantization error are uncorrelated, the power spectral density can be calculated as,

$$\begin{aligned} S_{noise} &= \left(\frac{\delta}{M}\right)^2 S_E \sum_{k=0}^{M-1} \left\|1-e^{-j2\pi\left(\frac{f}{f_s}-\frac{k}{M}\right)}\right\|^{2(L-1)} \\ &= \left(\frac{\delta}{M}\right)^2 S_E 4^{L-1} \sum_{k=0}^{M-1} sin^{2(L-1)}\left(\pi\left(\frac{f}{f_s}-\frac{k}{M}\right)\right) \\ &= \frac{\delta^2}{M} S_E \frac{\left(2\left(L-1\right)\right)!}{\left(L-1\right)!\left(L-1\right)!} \end{aligned} \tag{29}$$

It comes that for any L^{th} order modulator that implements an ideal NTF of the form $\left(1-z^{-1}\right)^L$, the quantization noise folding due to chopper modulation should have a flat power spectrum. The total perturbation power that falls into the modulator baseband can thus be easily calculated, taking (22) into account:

$$\begin{aligned} &for \ M \geq 2, \\ &P_{noise} = \frac{\delta^2}{M}\frac{\Delta^2}{12OSR}\frac{\left(2\left(L-1\right)\right)!}{\left(L-1\right)!\left(L-1\right)!} \end{aligned} \tag{30}$$

The particular case $M = 1$ corresponds to the chopper operated at the Nyquist frequency and has been treated in the previous sub-section.

3) Random chopping: The developments carried out for the chopper operated at a frequency lower than $f_s/2$ allow us to foresee what should happen with a random chopping. Indeed, expression (13) remains valid, and the z-domain transform of the integrator output will now be convoluted by a a random signal. Notice, though, that the chopper transition signal is not the chopper signal, and the shape of their spectra may be quite different.

This is illustrated in Fig.9, which shows the power spectrum of the chopper signal (CH) proposed in [16] together with the corresponding chopper transition signal (CT). It can be seen that the chopper transition signal has a spectrum that is

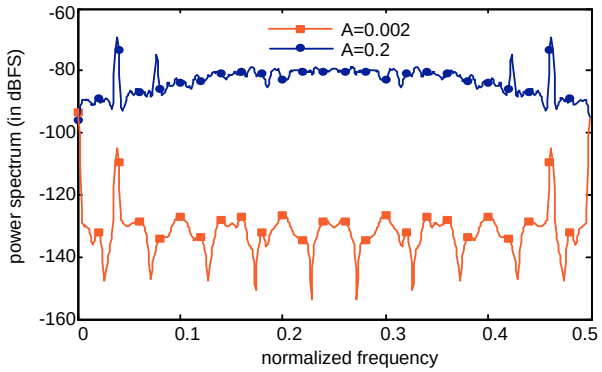

Fig. 10. Perturbation power spectrum for a 2^{nd} order modulator with chopper at $f_s/4$, for two amplitudes of the input sine-wave.

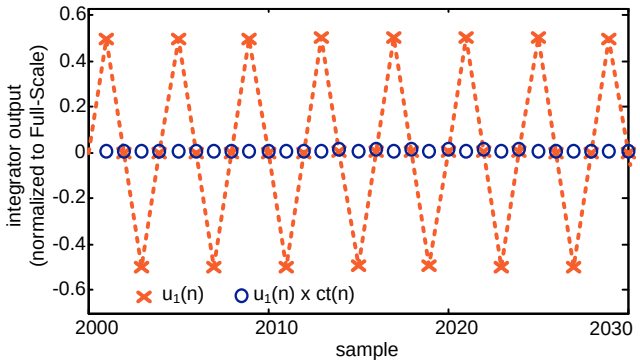

Fig. 11. Integrator output for a small amplitude input sinewave.

quite different from the chopper signal. Excepting a significant DC component and a tone at $f_s/2$, the spectrum is almost flat. Because the first integrator output is not correlated to the chopper transition signal (at least in first order), we can expect that the perturbation spectrum will have three contributions. The convolution with the DC component will lead to a scaled replica of the integrator output. The convolution by the tone at $f_s/2$ will lead to an alias of the integrator output. And finally, the convolution with the white noise will lead to a white noise. In order to calculate a closed form expression of the perturbation spectral density an analytical expression of $CT(z)$ would be necessary.

IV. The Pitfalls of High-Level Simulation

In order to reach closed form analytical expressions, we have used a well-known but strong approximation: modeling the quantization error E as a white noise source. The validity of this approximation is quite limited for $\Sigma\Delta$ modulators, particularly those that rely on a single-bit quantizer.

In order to illustrate this assertion, we perform a high-level simulation of a 2^{nd} order modulator like the one presented in [20], including our chopped-integrator model. A chopper with a parasitic parameter $\delta = 0.01$ at a frequency of $f_s/4$ is considered. Fig.10 shows the spectrum of the perturbation (acquired at the output of the gain block δ in Fig.5) for two different amplitudes of the input sine-wave. It appears clearly that the noise part of the perturbation spectrum is not flat and that it is very different in the two cases. There is thus a strong correlation between the input signal and the quantizer error E.

In the case of the small amplitude, the perturbation is almost negligible. This can be better understood taking a look at the integrator output in the time-domain.

The dashed line with cross markers in Fig.11 shows the integrator output for a small amplitude sine-wave (there is one marker per sample). The round markers correspond to the integrator output multiplied by the chopper-transition signal ct, which is the signal that is fed to the integrator input through the parasitic capacitor. For input signals close to zero, the integrator output follows a regular pattern whose period can be a multiple of the chopper transition period. In this particular case, the samples that coincide with chopper transitions are casually all close to zero. For that reason, the perturbation

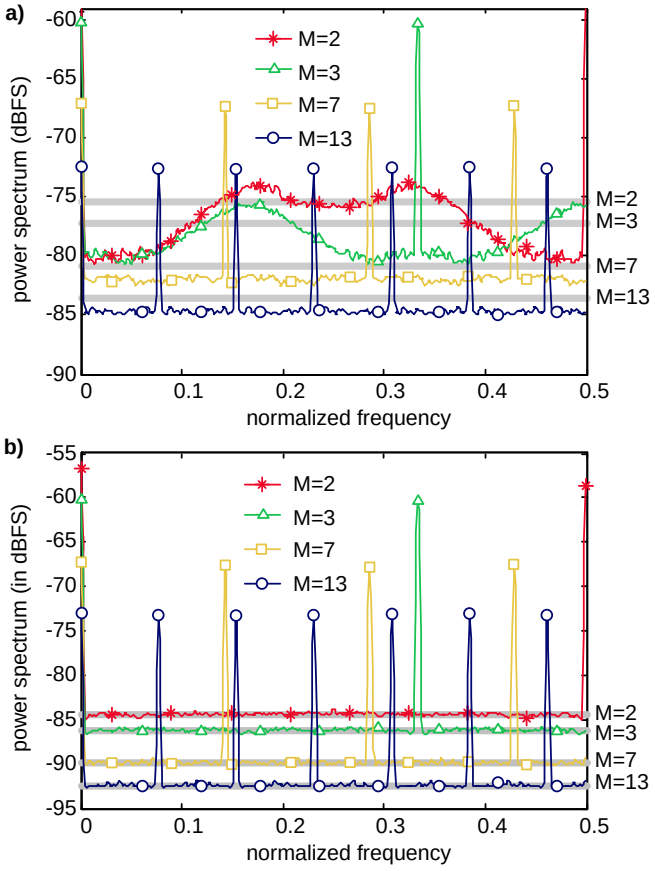

Fig. 12. Perturbation spectra for four chopper frequencies. These spectra have been produced by averaging the FFT of the perturbation signal for 1000 input sine-waves with a fixed amplitude but random DC level and phase. The modulator is a 2^{nd} order a) with a single-bit quantizer, b) with a 2-bit quantizer.

power is much lower than expected because the chopper does not capture the "noisy" component of the integrator output.

In order to get rid of the input signal correlation, we can perform 1000 simulations of the modulator for 1000 input sine-waves of identical amplitude and frequency but random DC level and random phase. By averaging the FFT results (computed with a Rife-Vincent window, over 1024 samples) for the 1000 sine-waves, we make the average correlation between the integrator output and the chopper transition signal

almost negligible. This allows retrieving a general trend in the perturbation that should be valid for realistic inputs (i.e. non pure tones). Fig.12-a shows the average spectrum obtained for four different chopper frequencies $f_s/(2M)$. The thick gray lines labeled on the right side of the figure represent the flat spectral density level that was expected according to (29).

Notice that the tones correspond to the signal part of the perturbation. The input signal is modulated at $kf_s/(2M)$, but only the DC level contribution can be appreciated because the small sine-wave amplitude (-60dBFS) falls below the noise floor.

It can be seen that the perturbation spectrum is still not truly flat for $M = 2$ and $M = 3$. The spectra present a valley at low frequency. This implies that the perturbation power in the baseband is lower than specified in (30) for low values of M. For $M = 7$ and $M = 13$, the perturbation spectra are much flatter, and (29) only overestimates the perturbation power in 1dBFS approximately.

The second order single-bit modulator chosen for the simulation exhibits strongly non-linear dynamics. It is well-known that Bennett's conditions are better fulfilled for higher order modulators, multi-bit quantizers or by the use of dithering. To illustrate this, we performed the same simulation on the same 2^{nd} order architecture but with a 2-bit quantizer. Fig.12-b displays the obtained results. It can be seen that in this case, the matching of the power spectra with (29) is almost perfect.

Two conclusions can be drawn from these simulations. The first one is that the closed-form expressions proposed in previous subsection are correct while the linearized quantizer approximation holds. When this approximation does not hold, they still give a good insight into the expected behavior, but high-level simulations would give more accurate results. The second conclusion is that some care must be taken with high-level simulation to ensure that we are not considering a particular case which would lead to underestimating the impact of chopper. Fortunately, with our event-driven model such simulations are computationally inexpensive and several cases can easily be explored.

V. Electrical validation

We have already studied static effects in chopped integrators, and verified that the analytical developments allow us to lay down a high level model for further investigation of chopper effects in discrete-time $\Sigma\Delta$ modulators. This section closes the validation loop and presents electrical simulations of a complete modulator with chopper.

For this purpose, we have designed a simple 3^{rd} order cascaded modulator at transistor level. The schematics shown in Fig.13 makes use of a $0.35\mu m$ CMOS technology. For the sake of simplicity, the three integrators are identical, with folded cascoded amplifiers of 83dB nominal gain. All the switches are balanced CMOS to approximate a signal-independent ON-resistance. The unit capacitor value is 423fF. Capacitor C_1 uses 2 unit capacitors and Capacitor C_2 uses 4. The gain of the integrator (b in Fig.5) is thus 0.5. The modulator is operated at 2MHz.

Notice that the expressions calculated from (19) hold for single-loop modulators. The results are still valid for our

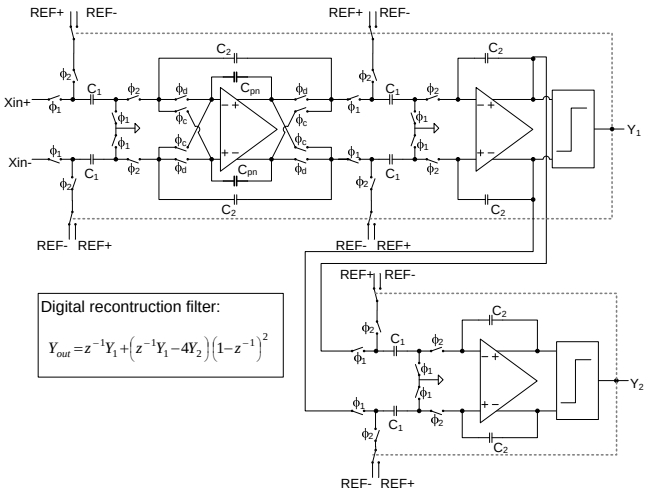

Fig. 13. $\Sigma\Delta$ modulator schematic used for electrical simulations.

cascaded modulator, but the order of the modulator ($L = 3$) has to be replaced by the order of the first stage ($L_1 = 2$).

The reconstruction filter (whose transfer function is quoted in Fig.13) combines the output bit-streams of the two stages to give the final modulator output. It is implemented as a post-processing task in order to keep the electrical simulation complexity as low as possible.

The effects described in this paper are particularly relevant for low-frequency, high-resolution applications. In order to reach a high resolution, the oversampling ratio (OSR) must be high. Combined with the fact that we want to resolve at least 256 FFT bins in the baseband, this leads to long transient simulation. Furthermore, very high accuracy settings must be considered to avoid arithmetic errors that would corrupt the results. Simulation times to reach 18 bit accuracy would be overwhelmingly long on our hardware. In order to present several simulation results, we preferred to consider a lower 16 bit resolution, typical in the audio market. This resolution is achieved with an OSR of only 64, and thus a transient simulation of only $256 \times 64 \times 0.5\mu s = 8.3ms$ can be considered. In order to validate our study, we have to choose a parasitic capacitor (and thus the parameter δ) sufficiently large such that the perturbation be visible in the output spectrum. Using (30), we can calculate that a parasitic parameter of $\delta = 4.6 \times 10^{-3}$ would lead to a resolution of 11.3 effective bits (ENOB) at an OSR of 64 and for a chopper operated at $f_s/8 = 250kHz$ (i.e. $M = 4$). This value should thus be sufficient to clearly notice the perturbation in the output spectrum. Taking into account the value of the integrating capacitor C_2, a parasitic capacitor $C_{pn} = 3.9fF$ is obtained. For our $0.35\mu m$ technology, such a parasitic may arise from a parallel routing of $50\mu m$ metal lines, as can be found in a signal bus. It is thus a realistic value.

With these parameters, we finally perform four different transient simulations of the modulator shown in Fig.13 including the parasitic capacitor. The simulator is Spectre in a Cadence Framework and uses the Bsim 3v3 models provided by the foundry. The accuracy option is set to "conservative", but the relative error is calculated with respect to global

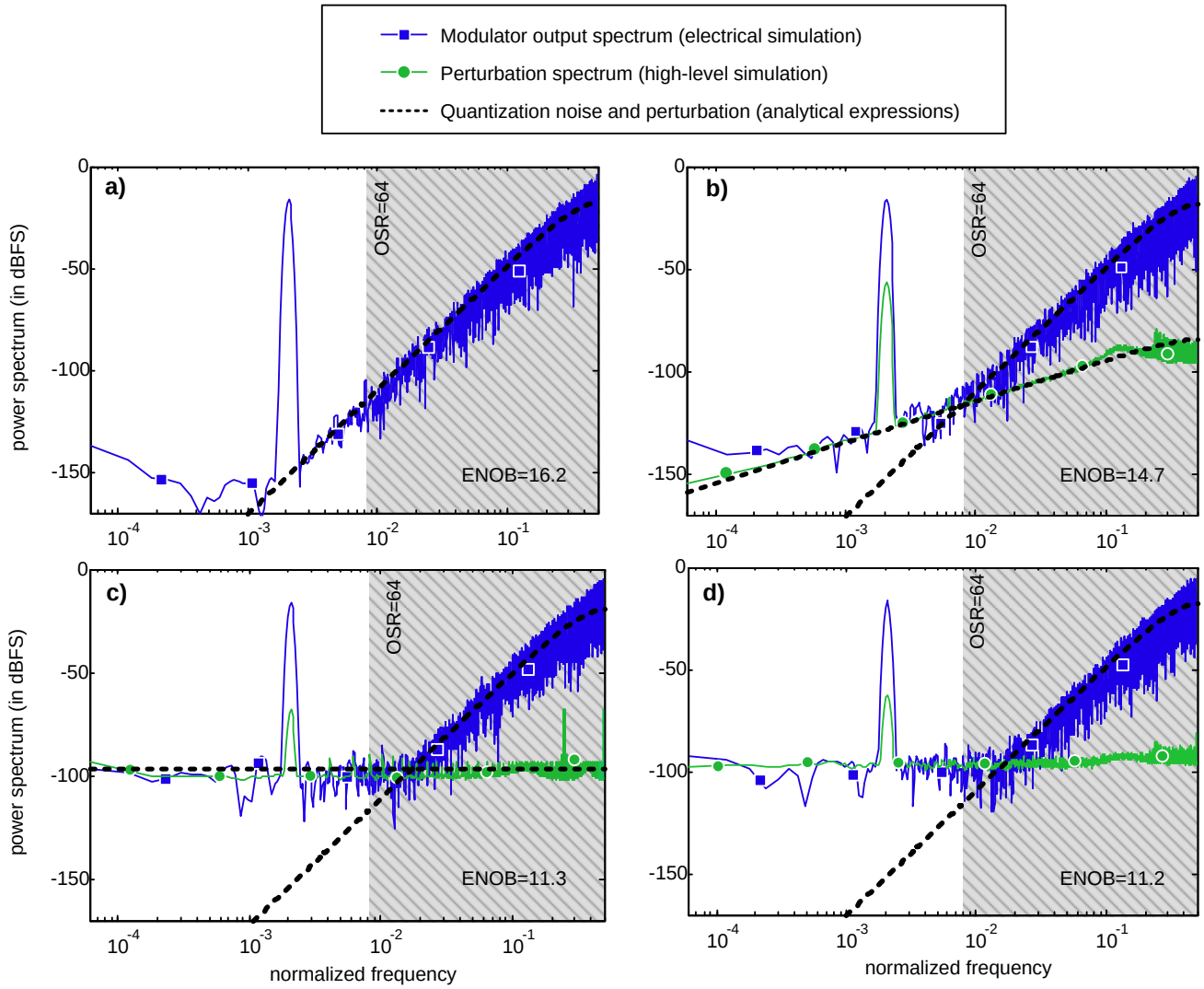

Fig. 14. Power spectrum of the modulator output obtained from electrical simulation. a) without chopper, b) with chopper at $f_s/2$ ($M = 1$), c) with chopper at $f_s/8$ ($M = 4$), d) with random chopper as proposed in [16].

signals instead of local signals, which greatly speeds up the simulation while maintaining the desired 16bit accuracy. The first simulation is done without chopper, the second in the particular case of a chopper operated at $f_s/2$ (i.e. $M = 1$), the third with a chopper operated at $f_s/8$ (i.e. $M = 4$) and the fourth with a random chopper as proposed in [16].

In addition to these electrical simulations, we have also performed simple high-level simulations in order to demonstrate that the perturbation approximation is reliable enough to take design decisions. More concretely, we have simulated an ideal model of the modulator architecture without chopper, for an input sine-wave of the same characteristics as for the electrical simulation and for the same number of samples (64×256). The chopper transition signals (ct) for the four cases described above have also been generated. This is straightforward for the first three cases and only the random chopper requires a specific simulation of the random sequence.

In this way, the expected perturbation can be built multiplying the ideal integrator output by the chopper transition signal and scaling the result by δ. As high-level simulation is almost inexpensive in terms of CPU time, the process is repeated 100 times, varying the phase of the input sine-wave. The FFT outputs are averaged in order to reduce spectrum variability. We could have built-up the high-level simulations with the proposed chopped-integrator model, but the selected approach validates the perturbation approximation that have been made for the analytical developments.

Fig.14 displays the obtained results. For all FFTs, the same high performance window as previously has been used. For the first case (a), there is no expected perturbation since there is no chopper. It can be seen that there is a white noise floor that limits the resolution of the modulator. This is due to arithmetic errors of the simulator, as explained above. For the second case (b), the perturbation appears to be shaped to a first order, as expected, taking into account that the first stage of the modulator is of order $L_1 = 2$. The analytical expression of the expected power density, according to (23), is also represented by a dashed line. The matching is almost perfect in the baseband, where the perturbation dominates the quantization noise. Notice that operating the chopper

at $f_s/2$ may lead to an additional degradation through the coupling to the voltage references. This effect may outweigh the perturbation but it does not appear here because we used ideal voltage sources for the references. For the third case (c), we also see that the perturbation derived from the ideal high-level simulation almost perfectly match the electrical results. Here again, we have represented by a dashed line the analytical power spectral density derived in (30). As commented before, the modulator quantizer is single-bit so the quantization error cannot accurately be approximated to a white noise, at least not for a pure tone input. Anyhow, the analytical expression still gives a reliable order of magnitude for the perturbation. Noticeably, the measured ENOB for the electrical simulation is 11.3, exactly the expected value calculated using (30). Indeed, the tonal components of the perturbation compensate for the slightly lower noise floor. And for the fourth and last case (c), the high-level simulation of the perturbation perfectly matches the electrical results in the baseband. We can see that the perturbation is almost flat, as expected. There is also a signal alias around $f_s/2$ that cannot be clearly seen on the figure due to the logarithmic scale of the frequency axis. The measured ENOB is 11.2, which is quite similar to the value obtained for the chopper at $f_s/8$.

For validation purpose, we have considered a parasitic capacitance of $3.9fF$. However, the perturbation theory tells us that the smaller the perturbation the more accurate the approximation. Thus, we can be confident that the results for smaller parasitics will be valid. As a matter of fact, we would only have to scale down the perturbation by the new δ.

So these results are significant in two ways. Not only do they validate our developments but they also show that simple high-level simulations of an ideal model are sufficient to generate an accurate perturbation for different chopper signals and parasitic values.

VI. Practical considerations

From the chopped-integrator effects studied in this paper we can draw some practical implementation considerations to avoid chopper-related performance degradation in discrete-time $\Sigma\Delta$ modulators. The goal of these guidelines is to help the handling of coupling parasitic capacitances effects derived from the chopping scheme that were chosen for the particular application. In general, the chopping signal is selected to meet the requirements of offset and Flicker noise attenuation. Operating the chopper at $f_s/2$ is possibly the most efficient solution but entails the risk of coupling onto the voltage references. Using a lower frequency $f_s/2M$ only requires a frequency divider but may lead to more noise folding. Finally, random chopping may completely remove the risk of coupling onto the voltage references but involves more hardware.

In any case,

- Consider the use the chopped-integrator model illustrated in Fig.5 in order to verify the chosen scheme and the impact of the chopper transition component on the offset and Flicker noise. The latter is particularly sensitive to folding.
- Evaluate, either analytically or with high-level simulations, the maximum δ that does not cause performance degradation for your application. Remember that several simulations must be performed (for instance with different input waveforms) to avoid any particular case that would underestimate the chopper impact. For example, if the objective is to reach 20bits with a 5^{th} order single-loop modulator (i.e. $L = 5$) with a quantizer of $q = 3$ bits, for an OSR of 64, operating the chopper at $f_s/4$ (i.e. $M = 2$), you must ensure that,

$$P_{noise} \leq \frac{1}{12\left(2^{ENOB}-1\right)} \tag{31}$$

which, using (30), reduces to

$$\delta \leq \frac{2^q-1}{2^{ENOB}-1}\sqrt{\frac{M \times OSR}{(2\,(L-1))!}} = 3.2 \times 10^{-6} \tag{32}$$

- Calculate the maximum parasitic capacitance that is affordable for your design, taking into account the value of the integrating capacitance. In the above example, an integrating capacitance as high as 20pF would lead to a maximum parasitic capacitance between the amplifier input and output as small as 32aF.
- Lay out the chopped integrator taking care of possible couplings between the input and output nodes of the amplifier. In particular, avoid crossings of metal lines or adjacent routing in an analog bus. If this is not possible, consider the possibility not to use consecutive metals for the crossings and a larger separation of the metal lines in the bus. We have seen that $50\mu m$ parallel metal lines at minimum separation lead to a parasitic capacitance of 3.9fF for the technology that we have used. A minimum metal crossing would give a 85aF capacitance, which is still 3 times higher than the required value.
- Verify that the extraction rules for your design kit consider parasitic capacitances lower than your maximum affordable parasitic capacitance. If not, you cannot fully rely on the extractor and you should modify the minimum extracted capacitor. In our case, the minimum extracted capacitance is 250aF for the default settings, so we had to calculate the value for minimum metal crossing from the technology data.
- Perform extraction of the modulator layout and probe the parasitic between the amplifier input and output nodes. Modify the layout until the parasitics are within your design guard-band.

VII. Conclusion

Despite its conceptual simplicity, chopper should not be regarded as the simple addition of four switches around the amplifier. It has been shown in this paper that the introduction of a chopper in the first integrator of a $\Sigma\Delta$ modulator effectively modulates the amplifier offset and Flicker noise out of the base-band. However, these contributions are not simply modulated by the chopper signal but also by a signal that depends on the chopper transitions. This must be taken into account to meet precision requirements, particularly when the chopper signal is not a square signal. Furthermore, it has been demonstrated that even a small parasitic capacitance may

lead to significant performance degradation due to quantization noise demodulation into the base-band. Hence the chopper in a $\Sigma\Delta$ modulator should be designed and laid out with care.

ACKNOWLEDGMENT

The authors would like to thank the reviewers for their very constructive comments.

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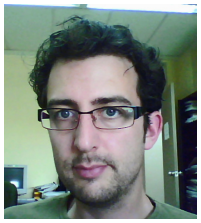
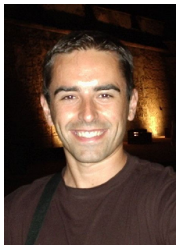


Gildas Léger received the Physics engineering degree from the *Institut National des Sciences Appliquées* (INSA) of Rennes, France, in 1999 and the Ph.D. degree in microelectronics from the University of Sevilla, Spain, in 2007.

He is currently holding a position of Tenured Scientist at the *Instituto de Microelectrónica de Sevilla* (IMSE-CNM-CSIC), Spain.

He has participated in different research projects financed by the European Community and the Spanish government but also in development projects for industrial partners. His fields of interest include the design of mixed-signal circuits and systems, for specific applications like biomedical or space. More particularly, his research focuses on design for testability in the domain of analog to digital conversion.



Antonio J. Gines Arteaga received the Physics degree in electronics in 2000 from University of Seville (Spain) and joined the Instituto de Microelectrnica de Sevilla (IMSE-CNM-CSIC), where is currently a researcher. In July 2008, he obtained the Ph.D. degree in microelectronics also from the University of Seville.

His current research interests include the design, modeling and testing of CMOS analogue mixed-signal circuits with emphasis on high-speed high-resolution data converters with digital background calibration and RF front-ends for wireless communications.

Eduardo J. Peralías Macías Eduardo J. Peralías Macías was born in Seville, Spain in 1964. He received the Licenciado en Fsicas degree in 1992 and the Doctor en Ciencias Fsicas degree in 1999, both from the University of Seville, Spain. From 1999 to 2001, he was with the Departamento de Electrnica y Electromagnetismo at the University of Seville as Assistant Professor. Since 2001, he has been with the Instituto de Microelectrnica de Sevilla (IMSE-CNM-CSIC), where he is currently a Tenured Scientist. His research interests are in the areas of Mixed Design with emphasis on Analog-to-Digital converters, Test and Design for Testability of Analog and Mixed-Signal Circuits, and Statistical Behavioral Modeling.

Adoración Rueda obtained the Ph.D. degree in 1982 from the University of Sevilla, Spain. From 1984 to 1996 she was Associate Professor in that University, where she now holds the position of Professor in Electronics. In 1989, she became researcher at the Department of Analog Design of the National Microelectronics Center (CNM), now Institute of Microelectronics at Seville (IMSE).

She has participated in many research projects financed by the Spanish government, and by different programs of the European Community. She has co-authored many papers in international journals and major conferences or books. In 1992 she won the Best Paper Award of the 10^{th} IEEE VLSI Test Symposium. Her research interests currently focus on the topics: Design and Test of Analog and Mixed-Signal Circuits, RF design, Behavioral Modeling of Mixed-Signal Circuits, and Biomedical applications. She is an IEEE senior member.