Analog sinewave signal generators for mixed-signal built-in test applications

Manuel J. Barragán, Diego Vázquez, Adoración Rueda

Instituto de Microelectrónica de Sevilla - Centro Nacional de Microelectrónica - Consejo Superior de Investigaciones Científicas (IMSE-CNM-CSIC), Universidad de Sevilla, Ed. IMSE-CNM, Av. Americo Vespucio, s/n 41092, Seville, Spain

Abstract: *This work presents a technique for the generation of analog sinusoidal signals with high spectral quality and reduced circuitry resources. Two integrated demonstrators are presented to show the feasibility of the approach. The proposed generation technique is based on a modified analog filter that provides a sinusoidal output as the response to a DC input. It has the attributes of digital programming and control, low area overhead, and low design effort, which make this approach very suitable as test stimulus generator for built-in test applications. The demonstrators –a continuous-time generator and a discrete-time one– have been integrated in a standard 0.35μm CMOS technology. Simulation results and experimental measurements in the lab are provided, and the obtained performance is compared to current state-of-the-art on-chip generation strategies.*

Keywords: On-chip Signal Generators, On-chip Sinewave Generators, Analog BIST, Mixed-Signal BIST.

I. Introduction

Commercial trends of ICs industry, including telecommunications, multimedia, instrumentation, automotive, etc. have forced the realization of complex mixed-signal electronic systems consisting of tightly integrated analog and digital circuitry onto a single IC substrate. Consequently, the increasing cost associated with testing and fault diagnosis of these complex systems has motivated research efforts to explore efficient testing methodologies. This issue is identified in the SIA Roadmap for Semiconductors [1] as one of the key problems for current and future mixed-signal SoCs.

Ususally, the main test difficulties are due to the test of the analog parts. Traditional test methods for analog circuits rely in functional tests, but the sensitivity of analog cores to loading effects, environmental conditions and process variations make their test a difficult task. Moreover, they demand high quality input stimuli, high data volume acquisition and processing capability, etc., requiring expensive ATE (Automatic Test Equipment). BIST (Built-in Self-Test) schemes are a well-accepted solution to overcome some of these problems. These schemes consist of moving part of the required test resources from the ATE to the chip [2].

This work demonstrates an efficient technique for the on-chip generation of sinusoidal analog test stimuli. This kind of signals has a wide variety of potential applications in the

field of analog and mixed-signal testing, and represents a key point for many testing schemes. In fact, most of the analog and mixed-signal subsystems in a SoC, such as analog filters, A/D converters, signal conditioners, etc, can be characterized by applying a sinusoidal test stimulus and analyzing the response. Providing an efficient method for the on-chip generation of analog sinusoidal stimuli can be identified as a key point to extend many testing procedures to a full-BIST scheme.

This paper is organized as follows. Section II reviews briefly different techniques, previously reported, for the generation of analog test stimuli, with a special focus in the generation of sinusoidal signals. Section III details the theoretical basis of the proposed generation method. After that, Section IV presents the design of two different integrated generators based on the proposed concepts. Section V summarizes some relevant experimental results obtained from the prototypes, and finally Section VI details the main contributions of this work.

II. Review of previous signal generation techniques

Analog test stimulus generation for BIST applications continues to be a hot topic in the test research community, and a number of different strategies for analog signal generation have been published for the last years [4]-[10], [12]-[17].

A classical solution for the generation of sinewave signals is the closed-loop oscillator [3]-[6], that consists of a filtering section with a non-linear feedback mechanism in the arrangement shown in Fig. 1a. The quality of the generated signal depends on the linearity and selectivity of the filter and the shape of the non-linear function. Highly selective filters and smooth non-linear functions are needed for the generation of high-accuracy, low-distorted waveforms.

Most of the proposed strategies for on-chip generation of test signals adopt the open-loop scheme in Fig. 1b. These waveform generators are usually based on a digital pattern generator followed by a D/A conversion. The digital pattern generator outputs a digital sequence, the D/A converter translates the digital pattern to the analog domain, and finally the signal is fed to an analog filter that attenuates all the non-desired components in the output signal. It has the advantages of a digital interface for control and programming tasks, and it also offers the characteristics of robustness and reusability that are common to the digital circuitry.

An interesting implementation of this open-loop generator, proposed in [7]-[9], is based on exploiting the noise-shaping characteristics of ΣΔ encoding schemes [11]. Basically, its functionality consists of generating a ΣΔ-encoded version of the desired signal, and then matching the shape of a reconstruction filter with the noise shaping characteristics of the encoded bit-stream. Single-tones with a high spectral quality can be obtained, and also arbitrary band-limited multi-tone waveforms can be easily generated. However, this technique demands a highly selective analog filter, at least one order higher than the order of the ΣΔ scheme used to generate the bitstream, to remove the noise.

A recent proposal for signal generation [10] combines closed-loop and open-loop strategies: it employs a simple closed-loop digital oscillator followed by a digital harmonic cancellation block and a passive low-pass filter to suppress low-frequency and high frequency harmonic components, respectively.

On the other hand, a very simple open-loop scheme for discrete-time periodic analog signal generation is reported in [12]-[13]. It consists of a variable-gain step-wise amplifier (VGA) where each gain step represents a value of a sampled and held signal. The performance that can be achieved, in terms of spectral purity, is limited by the accuracy and number of the generated steps. Improving spectral purity would require the use of an output filtering stage to reduce the level of unwanted components.

The discussed approaches achieve the desired signal generation using a variety of different techniques. However, some common elements can be identified:

• Both closed-loop and open-loop generators make use of analog filters to smooth the output signal, attenuate all the non-desired frequency components and, in the digital case, reconstruct the analog signal after the D/A interface. This analog output filter is essential for the generation of single-tone analog sinewaves, where a given spectral purity has to be assured.

• Focusing on open-loop generators, which are usually the preferred solutions, the unavoidable output filter must match the linearity of the previous digital circuitry in the generation chain. Otherwise, the linearity of the filter will limit the performance of the generator. This analog output filter effectively limits the maximum achievable performance of the complete system.

• The output filtering stage becomes a key element in these generation schemes.

Based on these common elements, authors presented in [14]-[15] a very simple generation

strategy that combines signal generation and filtering of the unwanted spectral components in a single system. This work is an extended and improved version of the previous one.

III. Proposed sinewave generation technique

This section reviews the theoretical basis of the generation technique, discusses briefly its possible implementation, and studies its main performance limitations.

A. Theoretical basis

Firstly, it is convenient to remark that although the discussion will be restricted to the continuous-time domain, it can be straightforwardly extended to the discrete-time case.

Let be a n-th order linear system as the one conceptually depicted in Fig. 2, with one input, $u(t)$, and one output, $y(t)$, described in terms of its state variables, $[x(t)]$, as,

$$\begin{aligned} [\dot{x}(t)] &= [a][x(t)] + [b(t)]u(t) \\ y(t) &= [c][x(t)] + d(t)u(t) \end{aligned} \qquad (1)$$

where $[x(t)]$ is an $n \times 1$ column vector, coefficient $[a]$ is an $n \times n$ matrix, coefficient $[b(t)]$ is an $n \times 1$ column vector, coefficient $[c]$ is a $1 \times n$ row vector, and coefficient $d(t)$ is a scalar function. Coefficients $[b(t)]$ and $d(t)$, which represent the dependence of the state variables $[x(t)]$ and the output $y(t)$ with respect to the input $u(t)$, are time dependent.

Let us consider the particular case,

$$\begin{aligned} [b(t)] &= [b]f(t) \\ d(t) &= d\,f(t) \end{aligned} \qquad (2)$$

where $[b]$ and d are constants and $f(t)$ is a time-dependent, externally controlled function. This particular case means that the input elements of the linear system, that is, the ones that relate the input, $u(t)$, to the evolution of both the state variables, $x(t)$, and the output, $y(t)$, vary in time according to a given function, $f(t)$. Fig. 3 shows a diagram of the described system, in which an external control over $f(t)$ have been included. Using the Laplace Transform, it can be shown from (1) that,

$$Y(s) = H(s)\{F(s) \otimes U(s)\} \qquad (3)$$

$$y(t) = h(t) \otimes \{f(t)u(t)\}$$

where capital letters denote the Laplace Transform, operator $\otimes$ represents the convolution product, $H(s)$ is a transfer function of value,

$$H(s) = [c]\{s[I] - [a]\}^{-1}[b] + d\,, \qquad (4)$$

function $h(t)$ is the Inverse Laplace Transform of $H(s)$, and $[I]$ is the $n \times n$ identity matrix.

From (3) it should be clear that the system performs, in the most general case, the processing of the product $f(t)\ u(t)$ according to the impulse response $h(t)$. Let us consider the particular case $u(t) = U$, where U is a constant DC level. Then, the output of the system can be rewritten as,

$$y(t) = h(t) \otimes \{U \cdot f(t)\} = U \cdot \{h(t) \otimes f(t)\} \qquad (5)$$

$$Y(s) = U\, H(s)\, F(s)$$

Under these conditions, as a response to a constant input, the system delivers an output signal $y(t)$, which is the function $f(t)$ processed accordingly to the impulse response $h(t)$ and scaled by a factor U.

B. Generator implementation: the choice of function f(t) and transfer function H(s)

Our sinewave signal generator takes advantage of the previous analytical results. Indeed, under specific conditions, the described system can be used as a sinewave generator. Thus, according to (5) the output of the system when excited by a DC signal is directly controlled by two functions: the externally controlled function $f(t)$, and the transfer function defined by the system coefficients $H(s)$. Consequently, if $f(t)$ is a periodic function, and $H(s)$ corresponds to a filter tuned to select one of the harmonic components in $f(t)$, then the output of the system will be a sinusoidal-like waveform. Moreover, both the amplitude and frequency of the output signal can be easily controlled. The amplitude is controlled by the input DC level, U, and the frequency by the frequency of the function $f(t)$ and the tuning of $H(s)$.

A trade-off arises between the spectral content of function $f(t)$ and the shape of the transfer function $H(s)$: the more similar function $f(t)$ is to a pure sinewave, the more relaxed the selectivity of $H(s)$ can be made.

Step-wise sinewaves offer a good trade-off in this sense. The spectral content of a step-wise sinewave, depicted in Fig. 4, is essentially the same of a sampled sinewave, but modulated by a sampling function. The practical realization of $f(t)$ as a step-wise sinewave also offers advantages in terms of simplicity. Step-wise variation of the input devices of a system can be achieved simply by switching devices in a digitally controlled device array.

Regarding the system transfer function, what is needed is to match its shape to the frequency of interest in the application. In this sense, lowpass and bandpass shapes are clearly

the most convenient whenever the main harmonic of function $f(t)$ is in the passband and any unwanted spectral components are in the rejection band, as depicted in Fig. 5.

C. Performance limit estimation

This subsection analyzes the performance that can be reached with the proposed generation strategy. In order to be realistic in the estimation, it is needed to make some considerations regarding the main limiting factors of the proposed technique. In this line, it should be clear that the main performance limitations of the proposed approach are given by:

• The realization of function $f(t)$: restricting the discussion to the case of step-wise sinewaves, both the number of steps per period, N, and the possible errors affecting the step levels will have a direct impact on the performance.

• The selected linear system: the shape of its transfer function $H(s)$ defines the attenuation of the non-desired frequency components of function $f(t)$, while its non-idealities in terms of non-linear behavior will introduce distortion in the output signal.

In fact, a trade-off can be defined between the number of steps composing $f(t)$ and the selectivity and linearity of the filtering stage. Thus, a high number of steps in $f(t)$ will push its spectral replicas to high frequencies, which allows to relax the specifications of the filter, but increases the overhead and complexity in the implementation of $f(t)$. On the contrary, a low number of steps reduces this complexity, but the spectral replicas are in this case closer to the main frequency and will need a sharper filter to be attenuated.

In addition, possible errors in the step levels (due to mismatching between devices, process variations, etc.) will introduce harmonic distortion in the $f(t)$ spectrum. Possible random errors in the duration of the steps can be also modeled as an added jitter noise. However, these timing errors have not been included in this analysis for the sake of simplicity. Other limiting factors, such as the non-linearity or the noise characteristics of the selected linear system are related to the particular implementation of the filtering stage, and not to the proposed generation scheme itself. For this reason, they will not be considered in this analysis either.

The proposed strategy has been analyzed in terms of Total Harmonic Distortion (THD) and Spurious-Free Dynamic Range (SFDR). Our analysis considers step-wise sinewaves for $f(t)$ functions, with N steps per period of duration T_s. Concerning the system transfer function, $H(s)$, in the view of the spectral content of function $f(t)$ the analysis considers lowpass first and second order filtering sections. The main tone in $f(t)$ has been made coincident to the

corner frequency of the filters. Thus, the unwanted harmonic components will lay in the rejection band.

We performed a set of Monte-Carlo numerical simulations using maximum errors of 0.1% and 1% in the levels of the step-wise sinewave, $f(t)$, for the different filtering sections considered (with different values of the pole quality factor, Q, in the case of the second order sections). Fig. 6 shows the obtained worst cases in terms of SFDR and THD for a maximum error in the step levels of 0.1% as a function of the number of step levels and the quality factor Q. On the other hand, Fig. 7 shows the worst cases for a fixed Q value, as a function of the number of step levels and their maximum error.

It is clear to see that for a low number of step levels the obtained THD and SFDR are limited mainly by the first spectral replica, which, in this case, is close to the main tone of $f(t)$. This effect can be observed in Fig. 7, where it is shown that for $N \leq 16$ there is no significant improvement in the performance when the error level is decreased. On the other hand, from $N>16$ the effect of the replicas can be neglected, as they are far enough from the main tone and are effectively canceled by the filtering. The performance in this case is mainly limited by the accuracy of the steps and the selectivity of the filter.

The results show that very good SFDR and THD can be obtained for a relatively low number of steps per period and a low-order filter. However, it is important to remark that these estimations are optimistic, since other limiting factors such as the non-linearity or the noise characteristics of the filtering section were not considered. That is, results in Fig. 6 and Fig. 7 mark the maximum performance achievable by the proposed generation strategy, and it may be limited by the particular filter implementation. Nevertheless, it is convenient to remember that this limitation is unavoidable and common to any of the other approaches discussed in Section II.

IV. Prototypes design

Two prototypes have been designed to prove the feasibility of the proposed generation strategy: a continuous-time generator based on the OTA-C technique, and a discrete-time one based on the SC technique. The goal of these demonstrators is to show the feasibility of the proposed generator using two common filter design styles. In both cases, the selected filtering stage correspond to a second-order lowpass filter, while function $f(t)$ is a step-wise sinewave with 16 steps per period. According to the previous analysis, these choices offer a good trade-off solution between performance and implementation complexity. In a particular

test application, these choices can be made using the results in Fig. 6 and Fig. 7 in order to accommodate the test stimulus to the target linearity requirements.

Both prototypes were developed on a 0.35μm 4-metal 2-poly 3.3V CMOS technology. In the following, the design of the continuous-time OTA-C generator and discrete-time SC generator will be considered separately.

A. Continuous-time OTA-C generator

The continuous-time prototype has been derived from a typical fully-differential 2nd-order lowpass OTA-C filter. Fig. 8 shows the block diagram of this reference filter. Table 1 shows the design parameters, which correspond to a peak gain frequency tuning range from 20 MHz to 40 MHz approximately, a pole quality factor Q=5, and a peak gain of around 14 dB. The design parameters have been chosen using matching considerations. Thus, capacitors have been made equal, and transconductors are integer multiples of a unit transconductor. That is, transconductors G_{mA}, G_{mC}, and G_{mD} have been chosen to be five times larger than the unit transconductor G_{mB}, and they are built from five matched unit transconductors G_{mB} in parallel.

The block diagram of the developed generator is shown in Fig 9a. The only modification with respect to the reference filter is that the input transconductor G_{mA} has been replaced by a switching scheme controlled by the digital signal Φ_{in} and a programmable transconductor $G_{ma}(t)$ to implement the step-wise sinewave levels. Notice that due to the particular symmetry of a sinewave signal, only five different values are enough to describe the whole 16-step period. Thus, transconductor $G_{ma}(t)$ is composed by four transconductors in parallel (G_{m1} to G_{m4}) as depicted in Fig 9b, whose contributions are switched on or off in an incremental way accordingly to the time scheme shown in Fig. 9c. This way, the required five steps of the positive half sinewave are generated, while the input switching scheme controlled by signal Φ_{in} sets the weight, positive or negative, of the step. The resulting transconductance $G_{ma}(t)$ can be described as,

$$G_{ma}(t) = \{\Phi_{in}(t) - \overline{\Phi}_{in}(t)\}\left\{\sum_{k=0}^{4}\Phi_k(t)G_{mk}\right\} \qquad (6)$$

where

$$G_{mk} = G_{mA}\left[\sin\left(\frac{k\pi}{8}\right) - \sin\left(\frac{(k-1)\pi}{8}\right)\right] \qquad k = 1,\ 2,\ 3$$
$$G_{m4} = G_{mA}\left[\sin\left(\frac{4\pi}{8}\right) - \sin\left(\frac{2\pi}{8}\right)\right] \qquad (7)$$

Fig. 10 shows the transistor level schematic of the elemental OTA (bias circuitry is not shown for simplicity). It is a typical linearized transconductor with a source degeneration resistor (implemented by transistors M2a and M2b in Fig. 10) followed by a folded-cascode stage. The folded-cascode stage is used to provide impedance matching at every node and is shared by all the transconductors that are incident in the same node. Transistor sizing was performed according to the guidelines in [18] to get the desired transconductance value, and tuning range. Table 2 lists the sizes of the transistors in the elemental OTA, while Fig. 11 shows the output current versus input voltage transfer characteristic of the unit transconductor for V_{DD} = 3.3 V and different bias current conditions.

Concerning the design of the programmable input OTA, G_{ma}(t) the elemental transconductors G_{m1} to G_{m4} are similar to the unit transconductor in Fig. 10, but their input transistors M1 and M2 have been scaled to achieve the transconductance values defined in equation (7). Table 3 shows the sizes of the input transistors for each elemental transconductor G_{mk}.

B. Discrete-time SC generator

The discrete-time prototype has been derived from a Fleischer-Laker biquad [19] in a fully-differential lowpass configuration, as it is shown in Fig. 12. The filter operates with two non-overlapped clock phases ϕ_1 and ϕ_2. Table 4 lists the design parameters, which correspond to a peak gain of 6dB, a pole quality factor Q=5, and a corner frequency placed at one-sixteenth of the clock frequency. The proposed design reduces the capacitance spread to 12.75.

The system level block diagram of the discrete-time generator is shown in Fig. 13a. The only modification with respect to the original reference filter is that the input capacitor C_J has been replaced by a switching scheme controlled by signal ϕ_{in} and a programmable capacitor $C_j(t)$, that is composed by an array of four capacitors (C_{j1} to C_{j4}) as depicted in Fig. 13b, which are connected in parallel and to the signal path sequentially, according to the time scheme shown in Fig. 13c. Similarly to the OTA-C approach, this time-variant input scheme generates the required steps of a positive half sinewave, while the input switching scheme controlled by signal ϕ_{in} in Fig. 13c sets the weight (positive or negative) of the step. That is, the input capacitor can be described as,

$$C_j(t) = \{\phi_{in}(t) - \overline{\phi}_{in}(t)\}\left\{\sum_{k=0}^{4} c_k(t) C_{jk}\right\} \qquad (8)$$

where,

$$C_{jk} = C_J \sin\frac{k\pi}{8} \qquad k = 0,1,...,4 \qquad (9)$$

Given that, by construction, the peak frequency of the filter core is one-sixteenth of the clock frequency, the output signal frequency and the peak frequency are coincident when the control signals in Fig. 13c and clock phases ϕ_1 and ϕ_2 are synchronized to the same master clock. In this case the frequency of the generated signal and the central frequency of the filter core have been made coincident by design.

The selected amplifier architecture is a one-stage folded-cascode fully-differential amplifier. This kind of structure offers a good trade-off between gain and bandwidth. Moderate-to-high gain and bandwidth are possible, at the cost of a reduction of the output swing of the amplifier due to the cascode elements. Fig. 14a shows the transistor level schematic of the amplifier together with its bias circuitry. The necessary common-mode feedback is provided by the dynamic circuit in Fig. 14b. In addition, the 1.2 pF capacitors connected to the output nodes (C_2 in Fig. 14b) provide the needed frequency compensation for the amplifier. Table 5 lists the sizes of the transistors in Fig 14, while Table 6 shows the performance characteristics of the amplifier obtained by electrical simulation for biasing conditions V_{DD} = 3.3 V and I_{BIAS} = 60 μA. Typical minimum size CMOS switches have been adopted to reduce clock feedthrough effects.

V. Results

The developed OTA-C and SC generators were fabricated in the selected 0.35μm CMOS technology. Fig. 15 shows microphotographs of the integrated sinewave generators. The OTA-C generator occupies an area of 395μm × 230μm, while the SC one occupies 280μm × 550μm, excluding pads in both cases.

This section summarizes the most significant results obtained from these integrated prototypes. Electrical post-layout simulations and experimental results obtained in the laboratory are provided.

A. Continuous-time OTA-C generator

A.1. Post-layout simulation results

Fig. 16 shows the spectra of four different generated signals, obtained by electrical simulation of the full extracted view of the OTA-C generator. In these simulations the

frequency of the generated signal has been set to 40.7 MHz, while its peak-to-peak amplitude has been swept from 175 mV to 590 mV. In terms of spectral purity, the achieved SFDR keeps between 70 dB for the 175 mVpp signal, and 56 dB for the 590mVpp one. It is also clear in Fig. 16 that the spectral replicas in the $f(t)$ spectrum are attenuated by the filtering. Another set of simulations is shown in Fig. 17. This figure shows the obtained linearity parameters when sweeping both the amplitude and the frequency of the generated signal.

As it is shown, the quality of the signal decreases with the amplitude due to the limited linear range in the transconductors, and increases with the frequency due to the improved linearity of the OTAs caused by the higher bias currents needed to increase the filter peak frequency. It seems clear that in this case the linearity of the employed transconductors limits the performance of the generator.

In order to contemplate the effect of process, supply voltage, and temperature variations (PVT variations) over the linearity of the OTA-C generator, the system has been simulated in the eight worst-case process corners defined by the foundry. Fig. 18 shows the obtained THD and SFDR for an output signal of 345 mVpp at 40.7 MHz in the different process corners obtained by post-layout simulation. It is important to notice that the peak frequency of the filter was independently tuned for each corner to the desired 40.7 MHz frequency. As it can be derived from the results in Fig. 18 a ±2 dB worst-case variation in THD and SFDR is to be expected due to PVT variations.

A.2. Experimental results

The continuous-time generator was characterized via indirect measurements. A complete functional characterization in the lab was not possible at the present moment because the test equipment to generate the needed control signals at the required frequency (i. e. 640MHz clock frequency for a 40MHz output signal) was not available in our facilities.

Thus, In order to provide an indirect validation of the integrated prototype in the lab, the prototype was configured as a filter in the four gain configurations that define the step levels of the stepwise sinewave. The magnitude response was extracted using an arbitrary waveform generator to provide a test stimulus, and a digital oscilloscope to acquire the response. However, the limitations of our experimental set-up restrict the measurements to low frequencies. The four different gain step levels of the system were measured. For that, the set of digital control signals $\{\phi_{in}, \phi_1, \phi_2, \phi_3, \phi_4\}$ was fixed to the corresponding gain step level, and the magnitude response of the filter was extracted for each configuration. Fig. 19 shows

the obtained gain measurements (marked with stars), together with the expected gain of each step obtained by electrical simulation of the extracted view (solid lines). The agreement is good, however, the acquired data are not enough to give an estimation of the performance that could be achieved by the OTA-C prototype because at-speed THD and SFDR characterization were not possible. Nevertheless, these measurements validate the accuracy in the generation of the sinewave step levels in our prototype.

B. Discrete-time SC generator

B1. Post-layout simulation results

Fig. 20 shows the output signal spectrum for a 1 V peak-to-peak signal at 62.5kHz (1 MHz clock frequency), obtained by electrical simulation of the full extracted view of the SC generator. In terms of spectral purity, the achieved SFDR is 86 dB and the THD is 82 dB, which is in good agreement with the theoretical results obtained in Fig 7. The even harmonics are due to parasitic contributions that unbalanced the fully-differential architecture.

In order to contemplate the effect of PVT variations over the linearity of the SC generator, the previous simulation was repeated using the eight worst-case process corners provided by the foundry. Fig. 21 shows the obtained THD and SFDR. As it can be derived from the results in Fig. 21, THD worst-case variations are bounded in the [81 dB, 83 dB] interval, while SFDR worst-case variations are in the range [82 dB, 87 dB].

B2. Experimental results

A set of experiments has been developed to test the functionality and performance of the discrete-time sinewave generator. The test set-up makes use of the mixed-signal test system Agilent 93000. This test system generates the digital control signals and clock, provides the supply and analog reference voltages, and acquires and processes the output of the generator under test. However, the digitizer board available in the test system, that we employed to capture the analog output signal of the generator, features a 12-bit resolution A/D converter, with 75 dB THD at 1 MHz. These figures are below the performance predicted by the simulations, so it is expected that our test instrument limits the performance obtained in the measurements.

Fig. 22 shows four output waveforms from the sinewave generator and their corresponding spectra. The frequency of these signals is fixed to 62.5 kHz (1 MHz clock frequency). The generated output amplitude has been varied from 600 mV to 300 mV. The provided spectra were evaluated taking one sample per clock cycle.

Fig. 23 details THD and SFDR measurements as a function of the output amplitude for a given signal frequency, and as a function of the output frequency for a given signal amplitude. As it can be deduced, the quality of the signal is approximately constant over the whole operational range of the generator. As expected, a drop in the linearity performance is observed due to our experimental set-up. This limitation may explain also the fairly constant performance figures obtained in the measured amplitude and frequency range.

C. Comparison with state-of-the-art on-chip signal generators

Table 7 and Table 8 show a comparison to other reported solutions for analog signal generation in the continuous-time and discrete-time domains, respectively. The selected solutions are compared in terms of area, linearity, and output amplitude to supply range ratio (denoted as V_{pp}/V_{dd} in both tables). However, rather than a direct comparison between very different techniques, Table 7 and Table 8 are aimed to put the obtained results into perspective. Concerning the continuous-time generation domain, the analog ΣΔ oscillator in [6] gives the best performance figures, but at the cost of a higher circuit complexity (a 6^{th}-order Butterworth lowpass filter is used to cancel the quantization noise). The RAM-based generator in [7] makes use of ΣΔ encoding schemes to generate analog test signals. It offers comparatively high linearity figures, but needs also a selective analog filter (a 4^{th}-order low-pass filter is employed) to remove the shaped noise. The signal generator in [9] offers the lowest area occupation, the best V_{pp}/V_{dd} ratio among the considered designs, and a comparatively good linearity is demonstrated for low frequency applications. It reports a SNR of 60 dB at 0.833 kHz. The time-mode digital oscillator reported in [10] is mostly digital, achieves very good linearity figures by using a digital harmonic cancellation technique, and a comparatively high output swing. However, the area overhead is also high due to the integrated passive output filter. Finally, our proposed continuous-time OTA-C generator offers a good trade-off between performance and circuit complexity, although the output swing is penalized by the limited transconductor linear range. It is convenient also to remember that the presented figures for the OTA-C generator correspond to post-layout simulations.

In the discrete-time case, the measured performance figures, although they may be limited by the test set-up, compare well with the analog SC oscillator reported in [4], and represent a significant improvement with respect to the step-wise generator reported in [13], at the cost of a slightly higher silicon area.

The main advantage of the proposed technique is its inherent simplicity; while the required circuitry is mainly reduced to a low-order filter, it offers comparatively high linearity figures. On the other hand, its main disadvantage is that its application is limited to single-tone signals.

D. Application examples

The described generation technique can be used to extend many analog and mixed-signal test strategies to a built-in scheme. As an example of application, the work in [16]-[17] describes a built-in network analyzer that employs this generation technique to provide the test stimulus, enabling the test of analog components in the audio frequency range. The characterization of A/D converters is another clear application. For instance, characterizing the distortion of a 10-bit ADC requires a sinewave with THD above 68 dB [20], which can be achieved with the proposed generation technique.

VI. Conclusion

A methodology for the on-chip generation of analog sinusoidal signals with reduced circuitry resources has been presented. It is based on a modified low-order analog filter with a DC input and programmable input elements, in such a way that the filter itself performs two operations: signal generation and filtering of the unwanted components.

Two integrated prototypes have been presented to demonstrate the feasibility of the approach. The obtained performance figures compare well to other generation strategies presented in the literature. The developed continuous-time generator achieves a SFDR of 70 dB at 40.7 MHz, while the discrete-time one demonstrates a SFDR of 73 dB at 62.5 kHz. The developed generators have the attributes of digital programming and control capability, robustness and reduced area overhead. These characteristics make the proposed generation technique very suitable for BIST applications.

ACKNOWLEDGEMENTS

Authors want to thank Mr. José Miguel Mora Gutiérrez for his invaluable help with the test equipment. This work has been funded in part by the Spanish Government and FEDER funds through projects TEST (TEC2007-68072/MIC), SR2 (TSI-020400-2008-71/MEDEA+2A105), TOETS (CATRENE CT302), and by the Junta de Andalucia through project ACATEX (P09-TIC-5386).

REFERENCES

[1] SIA Roadmap for semiconductors 2009. http://public.itrs.net

[2] Huertas JL (2004) Test and design-for-testability in mixed-signal integrated circuits. Kluwer Academic Publishers, The Netherlands

[3] Sedra A, Smith KC (2004) Microelectronics Circuits, 5th Ed. Oxford University Press, New York

[4] Dominguez MA, Ausin JL, Duque-Carrillo JF, Torelli G (2006) A 1MHz area-efficient on-chip spectrum analyzer for analog testing. J Electron Test 22(4-6):437-448

[5] Park SW, Ausin JL, Bhamani F, Sanchez-Sinencio, E (2007) Non-linear shaping SC oscillator with enhanced linearity. IEEE J Solid-State Circuits 42(11):2421-2431

[6] Lu AK, Roberts GW, Johns D (1994) A high quality analog oscillator using oversampling D/A converters technique. IEEE Trans Circuits Syst II 41(7):437-444

[7] Dufort B, Roberts GW (1999) On-chip analog signal generation for mixed-signal BIST. IEEE J Solid-State Circuits 33(3):318-330

[8] Rolindez L, Mir S, Prenat G, Bouncer A (2004) A 0.18μm CMOS implementation of on-chip analogue test signal generation from digital patterns. In: Design Automation and Test in Europe, pp 704-705

[9] Prenat G, Mir S, Vázquez D, Rolíndez L (2005) A low-cost digital frequency testing approach for mixed-signal devices using ΣΔ modulation. Elsevier Microelectronics Journal 36(12):1080-1090

[10] Elsayed MM, Sánchez-Sinencio E (2010) A low THD, low power, high output-swing time-mode-based tunable oscillator via digital harmonic-cancellation technique. IEEE J Solid-State Circuits 45(5):1061-1071

[11] Norsworthy S, Schereier R, Temes G (1997) Delta Sigma Data Converters. IEEE Press, New York

[12] Patangia HC, Zenone B (1994) A programmable switched-capacitor sinewave generator. In: Midwest Symposium on Circuits and Systems, pp 165-168

[13] Mendez-Rivera MG, Valdes-Garcia A, Silva-Martinez J, Sanchez-Sinencio E (2005) An on-chip spectrum analyzer for analog built-in testing. J Electron Test 21(3):205-219

[14] Barragan MJ, Vazquez D, Rueda A, Huertas JL (2006) On-chip analog sinewave generator with reduced circuitry resources. In: Midwest Symposium on Circuits and Systems, pp 638-642

[15] Barragan MJ, Vazquez D, Rueda A, Huertas JL (2010) Guidelines for the efficient design of sinewave generators for analog/mixed-signal BIST. In: IEEE International Mixed-Signals, Sensors, and Systems Test Workshop

[16] Barragan MJ, Vazquez D, Rueda A (2010) A BIST Solution for Frequency Domain Characterization of Analog Circuits. J. Electron Test 26(4):429-441

[17] Barragan MJ, Vazquez D, Rueda A (2008) Practical Implementation of a Network Analyzer for Analog BIST Applications. In: Design Automation and Test in Europe, pp 80-85

[18] Kardontchik JE (1992) Introduction to the design of transconductor-capacitor filters. Kluwer Academic Publishers, The Netherlands

[19] Laker KR, Sansen WMC (1994) Design of analog integrated circuits and systems. McGraw-Hill International Edition

[20] Standard for Terminology and Test Method for Analog to Digital Converters, IEEE Std 1241, Jun. 2001

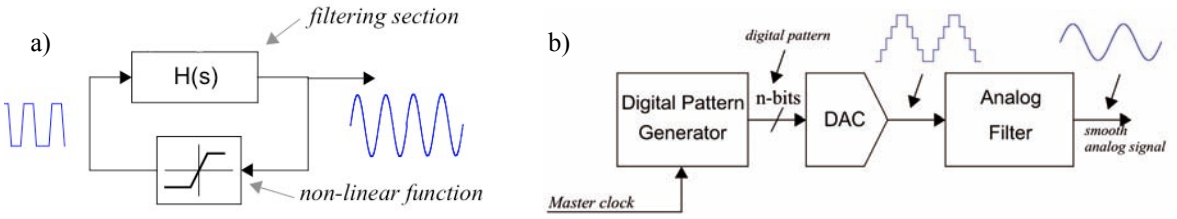

Fig. 1: a) Typical closed-loop signal generator; b) Typical open-loop signal generator

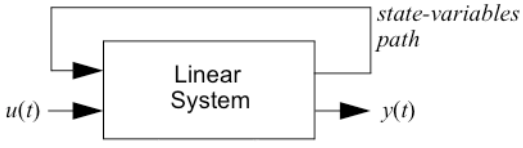

Fig. 2: Conceptual diagram of a generic linear system with one input and one output

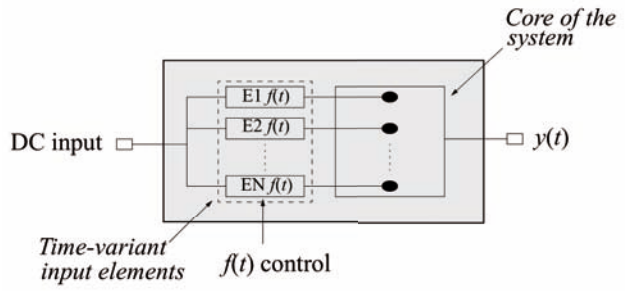

Fig. 3: Conceptual diagram of the proposed linear system with externally controlled time-variant input elements

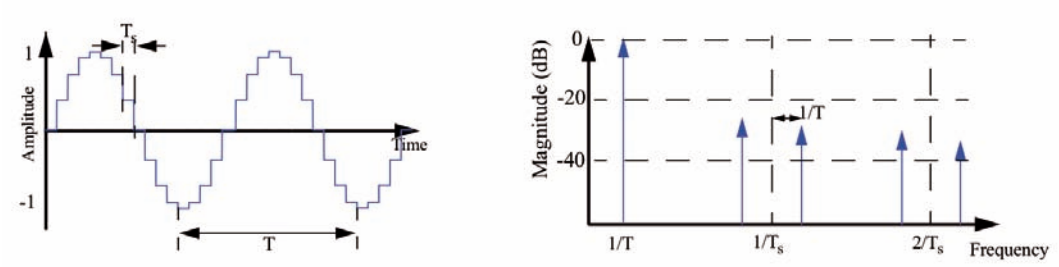

Fig. 4: Ideal step-wise sinewave: a) waveform; b) spectrum

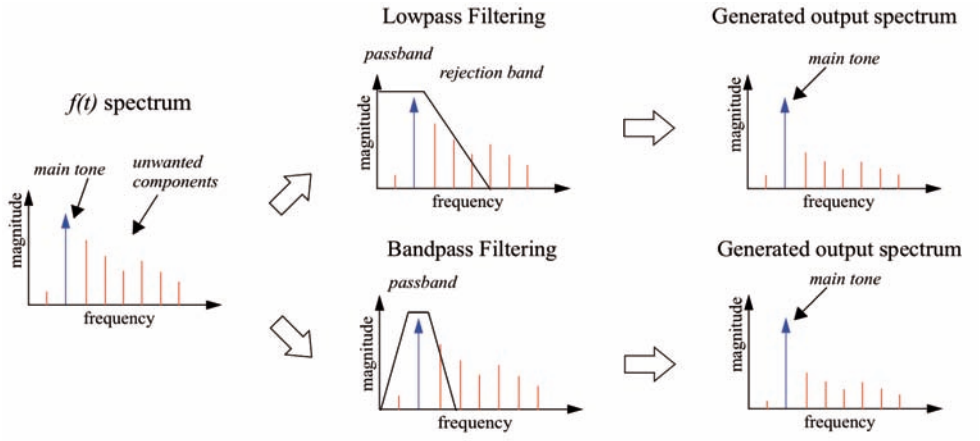

Fig. 5: Matching the shape of the filter and the target waveform

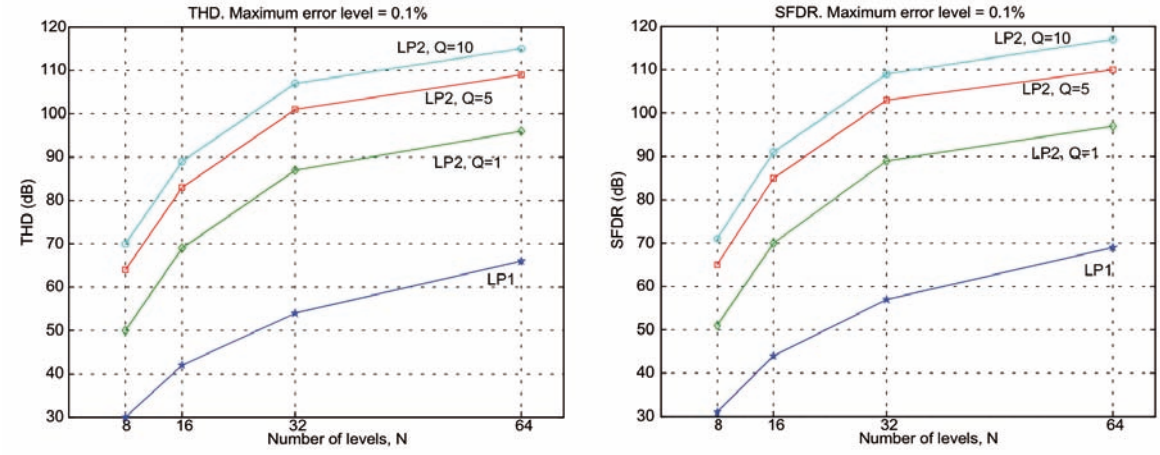

Fig. 6: THD and SFDR estimations for a maximum step error of 0.1% as a function of *N* and *Q*

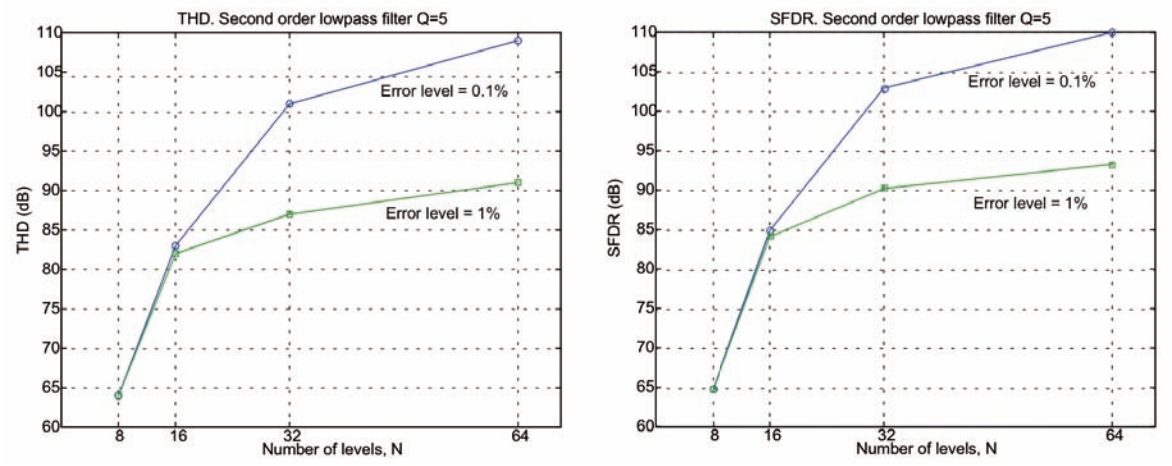

Fig. 7: THD and SFDR estimations for Q=5 as a function of *N* and the step error

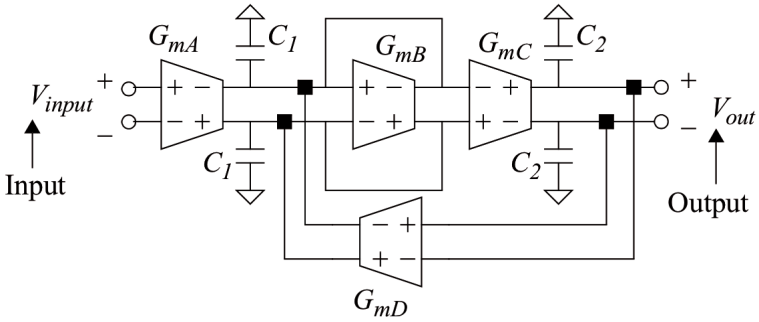

Fig. 8: Block diagram of the OTA-C reference filter

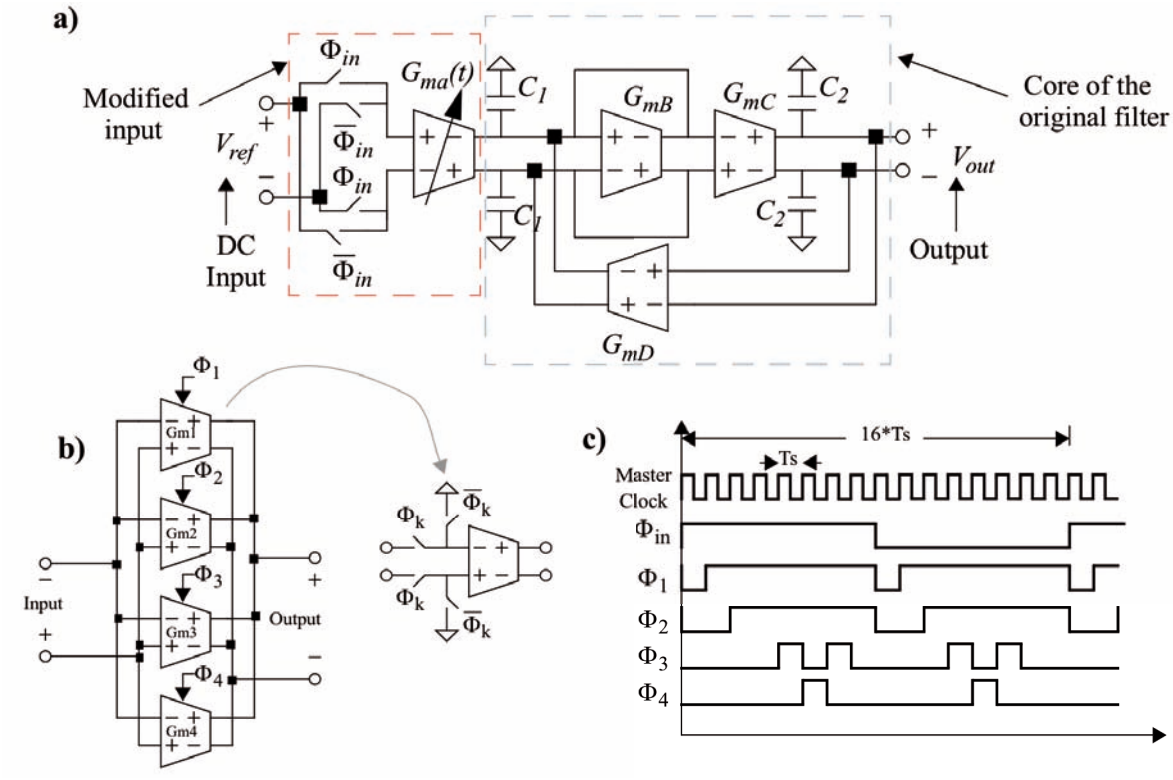

Fig. 9: a) Block diagram of the OTA-C sinewave generator; b) Implementation of the time-variant input transconductor; c) Timing diagram

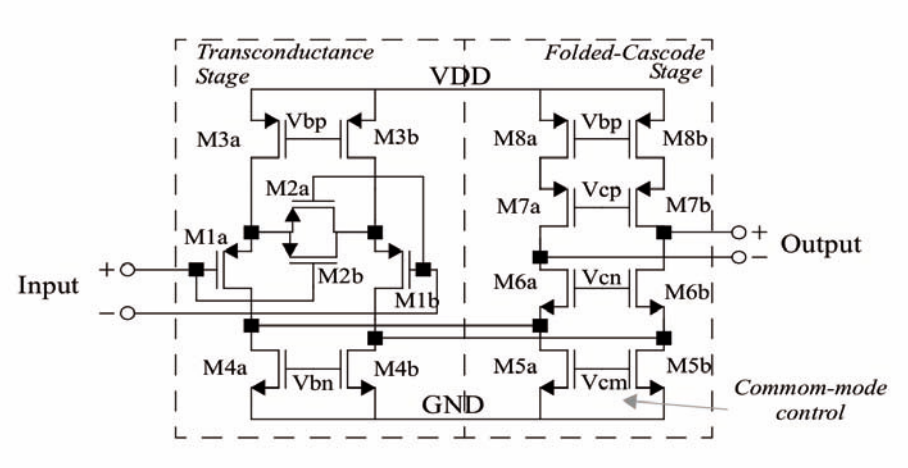

Fig. 10: Transistor level schematic of the implemented OTA

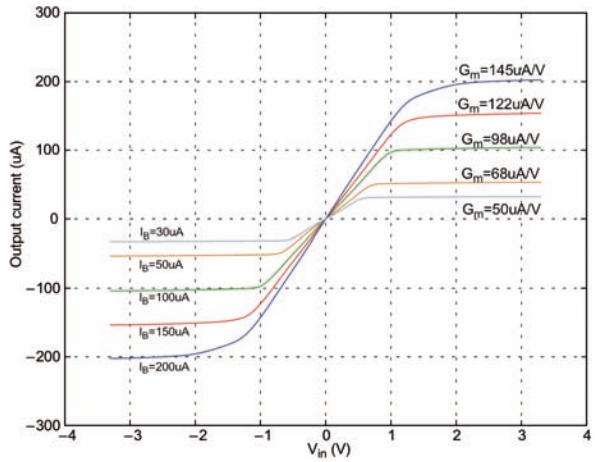

Fig. 11: Transfer characteristic of the unit OTA

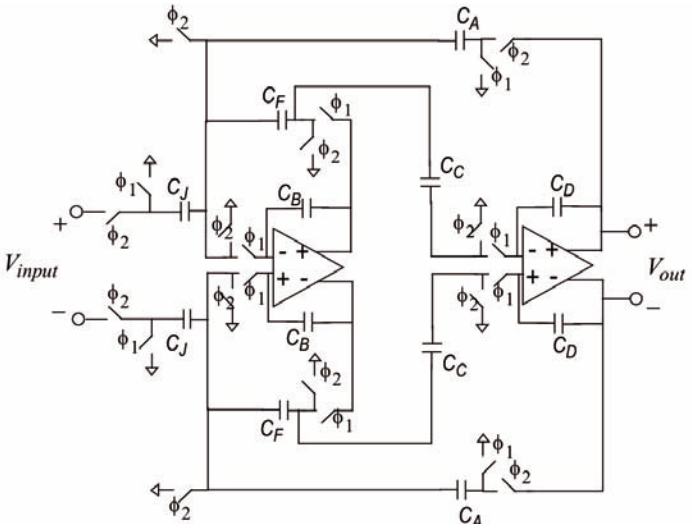

Fig. 12: Block diagram of the SC reference filter

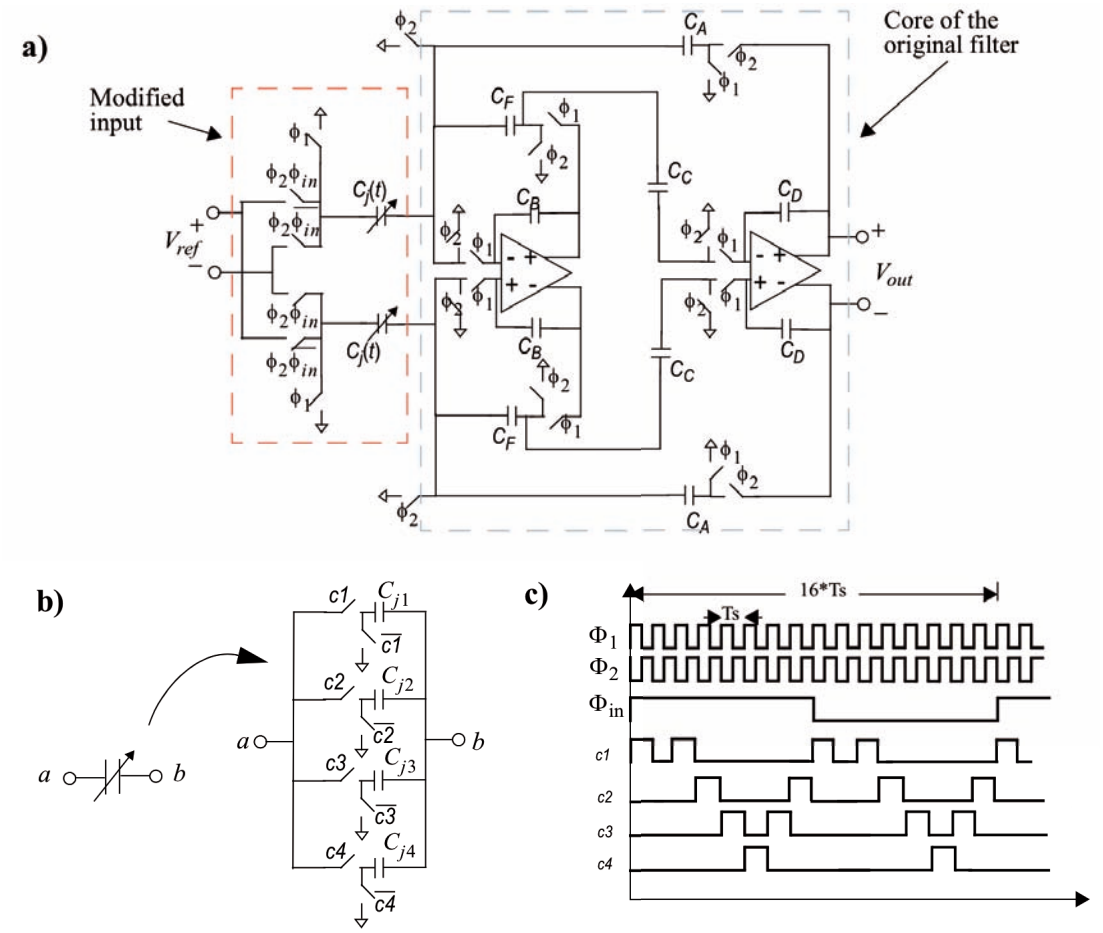

Fig. 13: a) Block diagram of the SC sinewave generator; b) Implementation of the time-variant input capacitor; c) Timing diagram

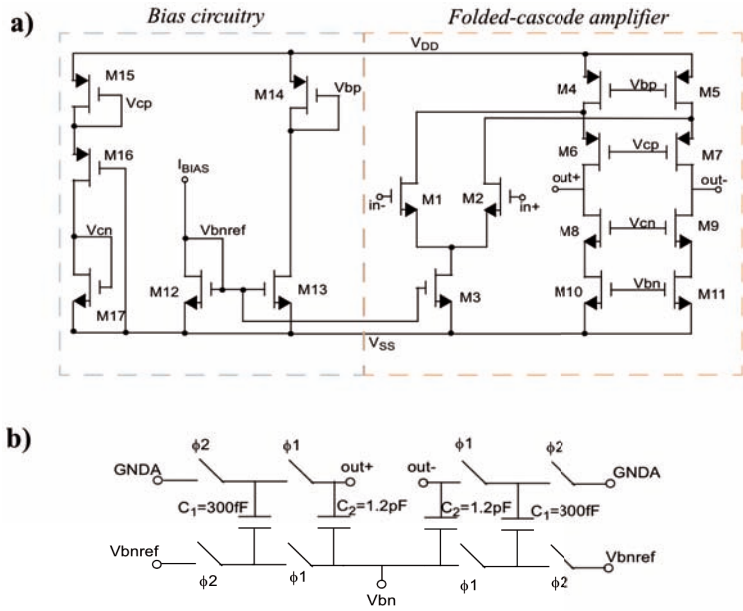

Fig. 14: a) Fully-differential folded-cascode amplifier; b) Dynamic common-mode feedback circuit

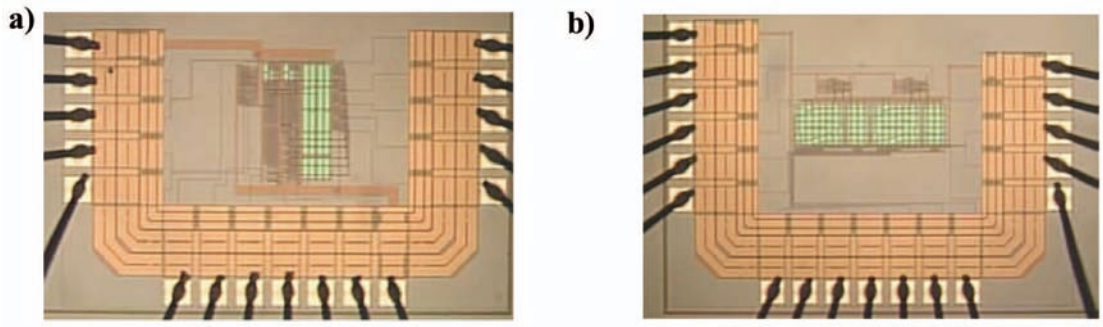

Fig. 15: Microphotographs of the integrated prototypes: a) Continuous-time OTA-C generator; b) Discrete-time SC generator

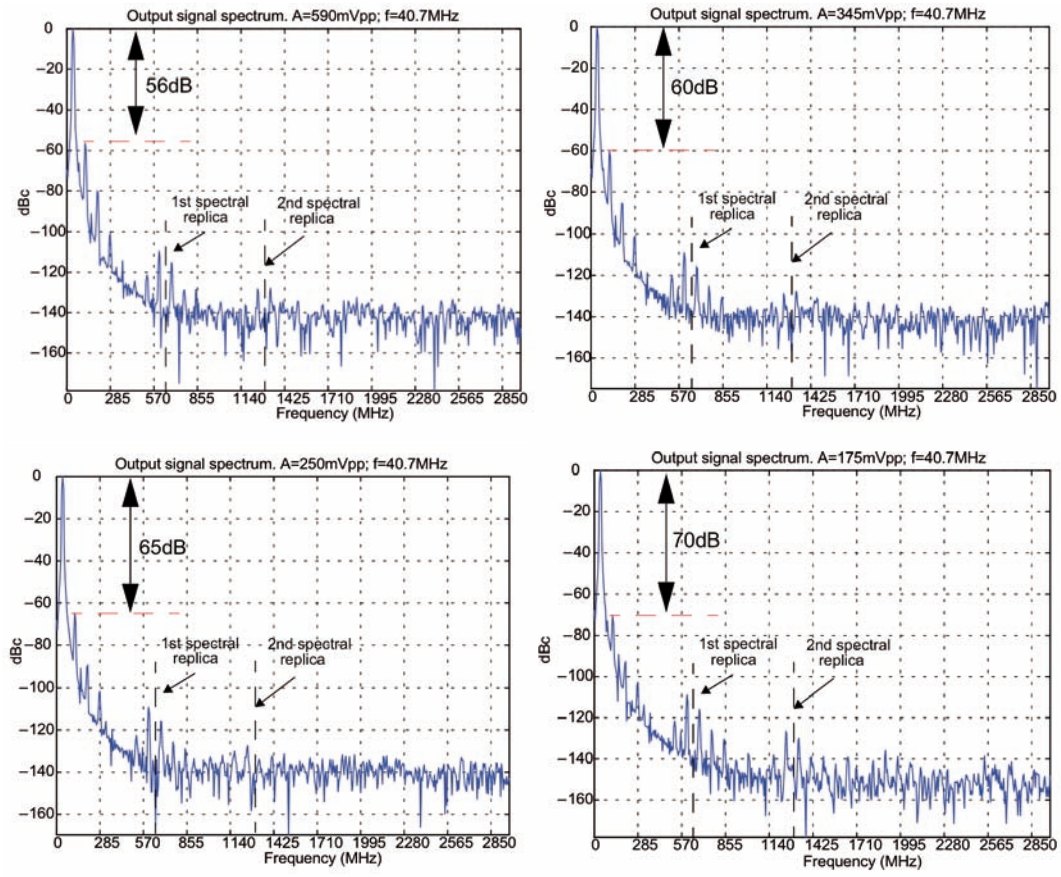

Fig. 16: OTA-C generator output signal obtained by post-layout simulations

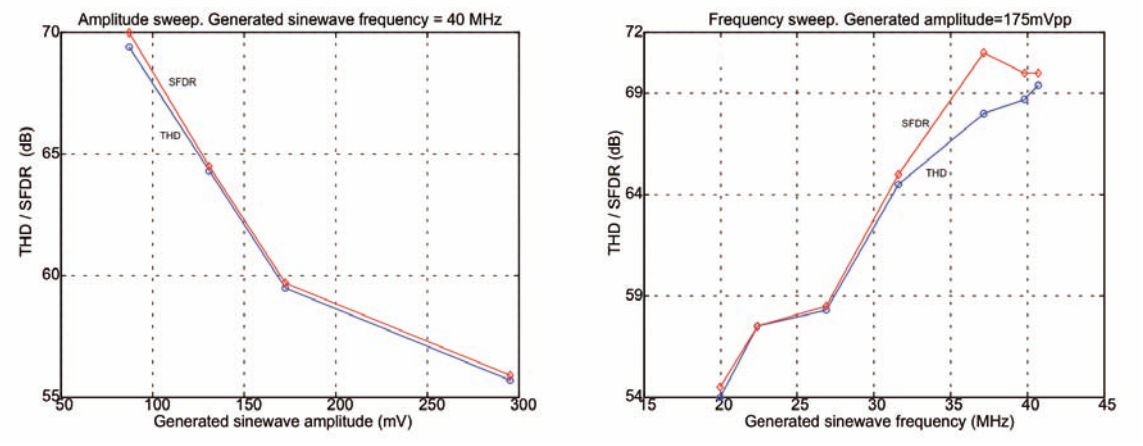

Fig. 17: Generator output THD and SFDR as a function of the: a) output amplitude; b) output frequency

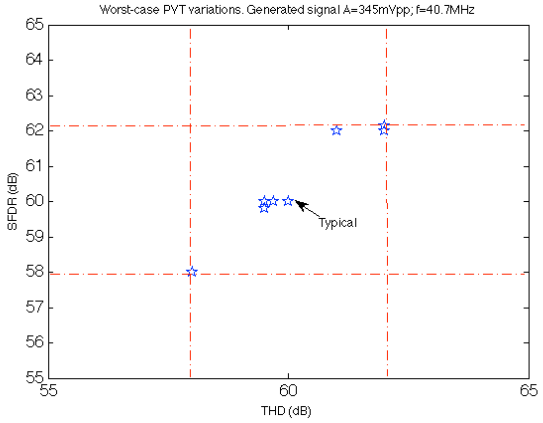

Fig. 18: Corner analysis: effect of worst-case PVT variations over the linearity of the OTA-C generator

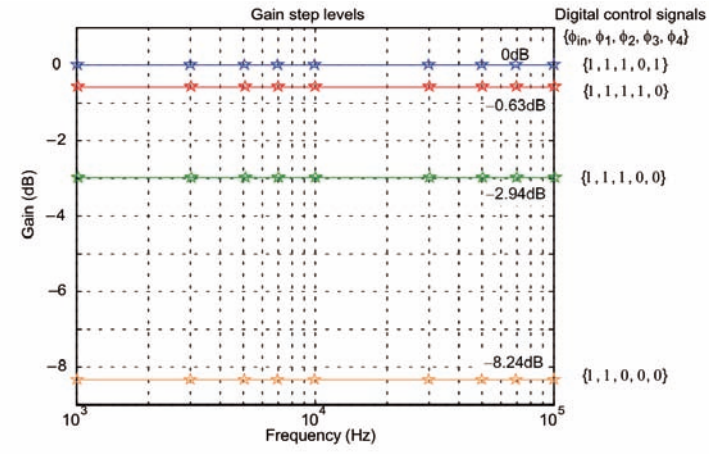

Fig. 19: Indirect validation of the OTA-C generator: gain steps for the different control signal configurations

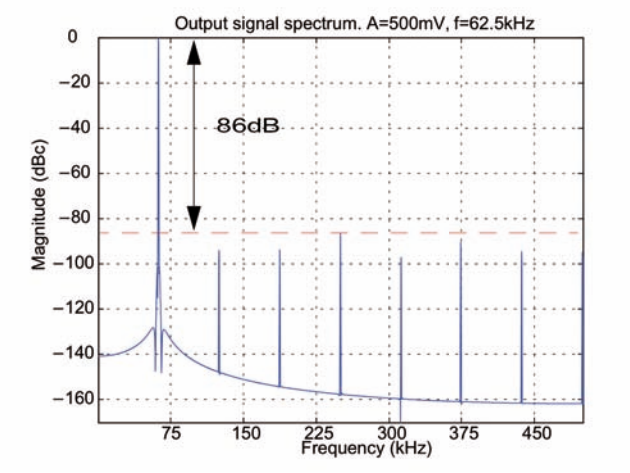

Fig. 20: SC generator output signal obtained by post-layout simulation

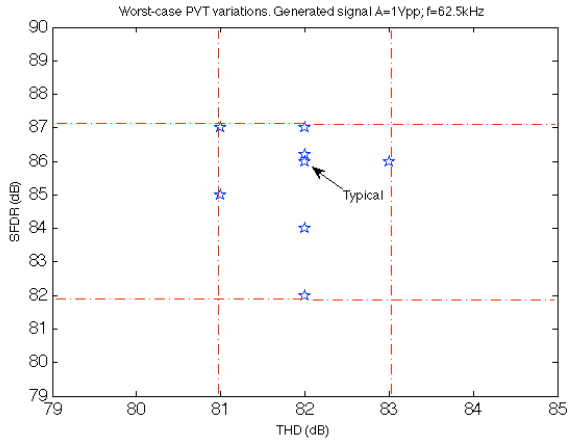

Fig. 21: Corner analysis: effect of worst-case PVT variations over the linearity of the SC generator

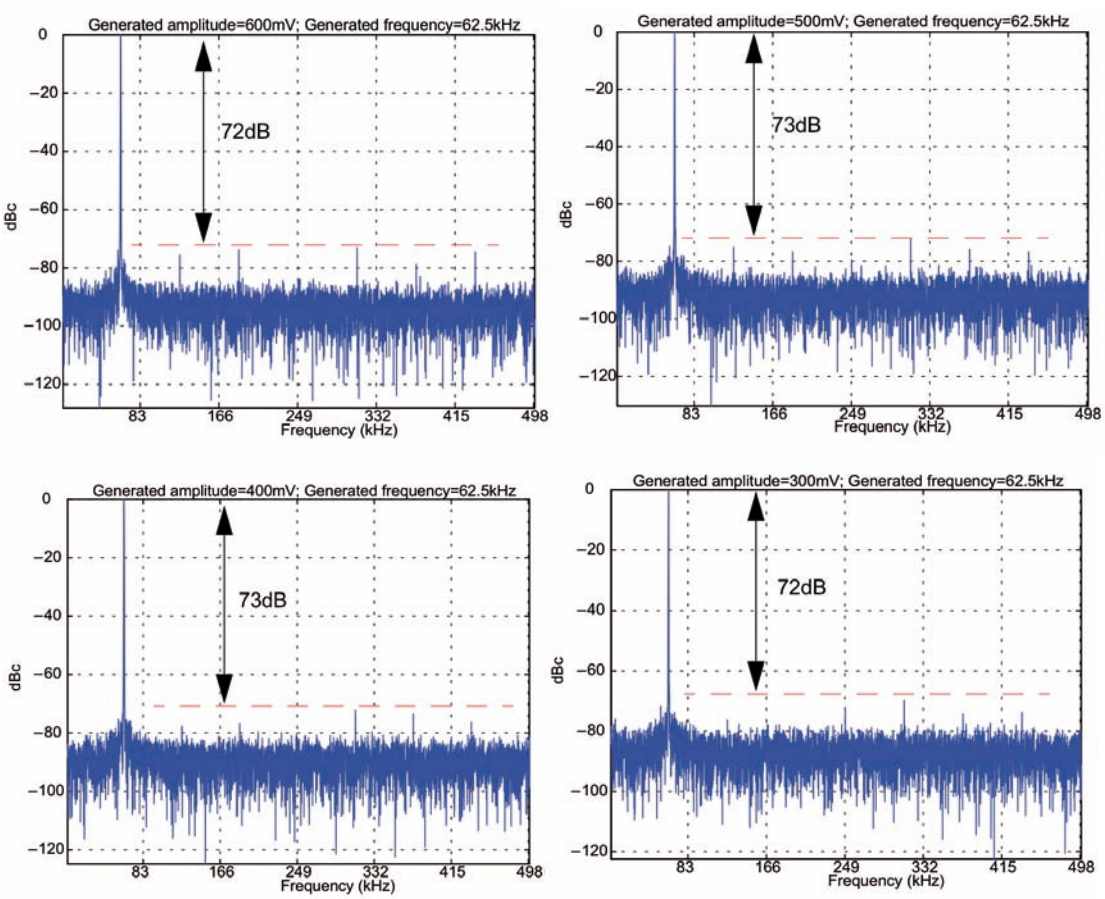

Fig. 22: Measured SC generator output signal spectra

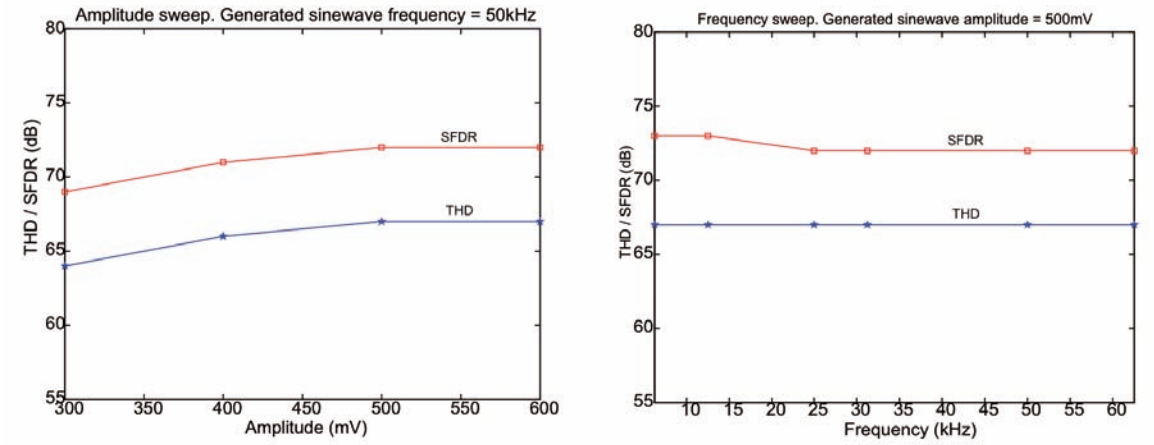

Fig. 23: Measured generator output THD and SFDR as a function of the: a) output amplitude; b) output frequency

Table 1: Design parameters for the OTA-C reference filter (tuning range for corner frequency from 20 MHz to 40 MHz)

G_{mA}	275 μA/V to 550 μA/V	G_{mD}	275 μA/V to 550 μA/V
G_{mB}	55 μA/V to 110 μA/V	C_1	4 pF
G_{mC}	275 μA/V to 550 μA/V	C_2	4 pF

Table 2: Transistor sizes for the unit OTA in Fig. 11

	M1	**M2**	**M3**	**M4**
W/L (μm/μm)	25/0.5	4/0.5	50/1	16/1

Table 3: Size of the input transistors for OTAs G_{m1} to G_{m4}

	G_{m1}		G_{m2}		G_{m3}		G_{m4}	
	M1	**M2**	**M1**	**M2**	**M1**	**M2**	**M1**	**M2**
W/L (μm/μm)	18/0.5	3/0.5	69/0.5	11/0.5	28.7/0.5	4.7/0.5	56/0.5	9.35/0.5

Table 4: Normalized capacitor values

C_A	5.194	C_D	2.574
C_B	12.749	C_F	1.014
C_C	1	C_J	2

Table 5: Transistor sizes for the amplifier in Fig. 15

	M1=M2	**M3**	**M4=M5**	**M6=M7**	**M8=M9**
W/L (μm/μm)	100/1	96/1	180/1	180/1	96/1
	M10=M11	**M12=M13**	**M14**	**M15=M16**	**M17**
W/L (μm/μm)	48/1	16/1	30/2	5/4	2.6/4

Table 6: Amplifier performance parameters (V_{DD} = 3.3 V, I_{BIAS} = 60 μA)

DC gain	80 dB
Gain-bandwidth product	180 MHz
Phase margin	55º
Settling time (1%)	4.0 ns
Slew-rate	170 V/μs

Table 7: Comparison to other continuous-time generation schemes

	ΣΔ-oscillator [6]	**RAM-based generator [7]**	**ΣΔ-modulation based generator [9]**	**Time-mode digital oscillator [10]**	**This work: OTA-C generator**
Technology	FPGA	0.8 μm BiCMOS	0.18 μm CMOS	0.13 μm CMOS	0.35 μm CMOS
Area	---	0.83 mm^2 + 4^{th} order filter	0.068 mm^2	0.186 mm^2	0.1 mm^2
THD	84 dB@5 kHz	Not reported	Not reported	72 dB@10 MHz	69 dB@40.7 MHz
SFDR	86 dB@5 kHz	65 dB@1 MHz	60 dB @0.833 kHz	74 dB@10 MHz	70 dB@40.7 MHz
V_{pp}/V_{dd}	Not reported	Not reported	720mV/V	190.1mV/V	53mV/V

Table 8: Comparison to other discrete-time generation schemes

	SC oscillator [4]	**Step-wise generator [13]**	**This work: SC generator**
Technology	0.35 μm CMOS	0.5 μm CMOS	0.35 μm CMOS
Area	0.13 mm^2	0.09 mm^2	0.15 mm^2
THD	58 dB@1 MHz	49 dB@1 kHz	67 dB@62.5 kHz
SFDR	60 dB@150 kHz	38 dB@10 kHz	73 dB@62.5 kHz
V_{pp}/V_{dd}	167mV/V	300mV/V	364mV/V