

# A new cascade $\Sigma\Delta$ modulator for low-voltage wideband applications

A. Morgado, R. del Río, J. M. de la Rosa

This letter presents a new cascade  $\Sigma\Delta$  modulator architecture with unity signal transfer function that avoids the need of digital filtering in the error cancellation logic. The combination of these two aspects make it highly tolerant to noise leakages, very robust to non-linearities of the circuitry and especially suited for low-voltage implementations at low oversampling. Behavioral simulations are presented that demonstrate the higher efficiency of the proposed topology compared to existing cascades intended for wideband applications.

**Introduction:** Many new communication systems have arisen in recent years that demand for high-bandwidth  $\Sigma\Delta$  modulators ( $\Sigma\Delta$ Ms) in low-voltage technologies [1]-[3]. Since oversampling must be restricted to low values in wideband applications, a usual design choice in order to achieve the required performance is to employ multi-stage noise shaping (MASH) architectures with multi-bit quantization. These  $\Sigma\Delta$  topologies circumvent the stability problems of high-order loops, but are sensitive to quantization noise leakages caused by mismatches between the analog and digital signal processing in the  $\Sigma\Delta$  cascade [4].

An alternative  $\Sigma\Delta$ M architecture that reduces the sensitivity to noise leakages of traditional cascade  $\Sigma\Delta$ Ms is the so-called Sturdy MASH (SMASH) modulator, recently presented in [1].

This topology, which is illustrated in Fig. 1 in the case of a 2-2 cascade, replaces the error cancellation logic required in traditional MASH modulators to properly combine the stages outputs by direct feedback paths from the 2nd-stage output to the 1st-stage input (marked in Fig. 1 with  $\otimes$  for clarity). The modulator output can be thus obtained from the direct digital subtraction of the two stages outputs, with no need of digital filtering of the stages outputs and therefore, the subsequent elimination of matching requirements between analog and digital filtering.

This letter presents a novel  $\Sigma\Delta$  cascade intended for high-speed low-voltage applications which extends the underlying principle of SMASH  $\Sigma\Delta$ Ms to the implementation of unity signal transfer functions (STFs) —i.e.,  $STF(z) = 1$ —, while circumventing the problems detected in the former ones. On the one hand, by using unity STFs, integrators ideally process quantization error only, so that the tolerance to amplifiers non-linearities is largely increased [2] [3]. On the other, by modifying the strategy to combine the stages outputs, digital filtering can still be avoided, while increasing the robustness and the simplicity of the  $\Sigma\Delta$ M.

**Proposed Cascade Topology:** The SMASH modulator in Fig. 1 suffers from several drawbacks associated to the direct feedback path from the 2nd-stage output to the first stage, namely:

- It requires, at least, one extra highly linear digital-to-analog converter (DAC) in the added feedback path to the 1st-stage input.

- It is very sensitive to mismatching effects in the added feedback paths with respect to the 1st-stage analog coefficients, which causes low-order noise leakages.

The proposed modulator architecture, depicted in Fig. 2, circumvents the above-mentioned drawbacks by means of the following strategies:

- On the one hand, the proposed architecture preserves the appealing features of implementing unity STFs, such as high overload levels and relaxed output swings and non-linearities for the amplifiers [2] [3].
- On the other hand, feedback paths from the 2nd-stage output to the first stage are removed by directly feeding the modulator output back to the first stage input. Note that, at the same time, the digital subtraction of the quantizers outputs is performed inside the 1st-stage loop. This strategy eliminates the need of, at least, one extra feedback path, so that the number of linear DACs required is not increased. However, a DAC with a full scale larger than that of the analog-to-digital converters (ADCs) in the cascade ( $B_1$  and  $B_2$ ) is required in order to account for the summation of the digital outputs of the stages. Although, as will be shown in the next section, the location of the digital adder helps to considerably increase the robustness to mismatches of the proposed cascade, thanks to the additional filtering obtained for noise leakages.

Considering a linear model for the quantizers in Fig. 2, it can be shown that the Z-domain

transform of the modulator output is given by:

$$Y(z) = X(z) - 1/d \cdot (1 - z^{-1})^4 \cdot E_2(z) \quad (1)$$

where  $X(z)$  stands for the input signal and  $E_2(z)$  is the quantization error of the second stage. Note that –contrary to the SMASH modulator in Fig. 1– the quantization error of the first stage,  $E_1(z)$ , is cancelled, while avoiding any digital filtering. In addition, using a scaling factor  $d$  that is a power of 2 will help to reduce the power of the 2nd-stage quantization error at the output and will require only a shift register before the digital subtraction. This scaling strategy can not be directly applied to the SMASH modulator, since in that case, the output will be given by:

$$Y(z) = z^{-2} \cdot X(z) + (1 - z^{-1})^4 \cdot E_1(z) - 1/d \cdot (1 - z^{-1})^4 \cdot E_2(z) \quad (2)$$

thus reducing the power of  $E_2(z)$  at the output, but not that of  $E_1(z)$ .

**Simulation results:** The performance of the proposed modulator (Fig. 2) has been compared to traditional 2-2 cascades and to the SMASH modulator (Fig. 1) by behavioral simulation using SIMSIDES, a Simulink-based time-domain simulator for  $\Sigma\Delta$  modulators [5]. All topologies operate with an oversampling ratio of 16, 4-bit internal quantizers and a 1-V reference voltage for comparison purposes with data reported in [1].

Fig.3 depicts the Signal to Noise and Distortion Ratio (SNDR) achieved by the diverse modulators versus the input level when considering quantization errors only. Note that the overload level of the proposed cascade is considerably larger compared to the SMASH and also improves that of traditional cascades. As shown in Fig.3, the attainable SNDR peak can be increased by operating the proposed topology with  $d > 1$ .

Table 1 shows both the overload levels and the output swing requirements of the amplifiers along the cascades. Note that the combined usage of unity STFs and multi-bit quantization leads to a remarkable relaxation of the output swing for the proposed modulator compared to MASH and SMASH topologies, what simplifies its low-voltage implementation.

The sensitivity to noise leakages due to mismatches has been studied for the diverse architectures on the basis of a Monte Carlo simulation. Fig.4 shows the SNDR at -6dBFS obtained for the SMASH modulator and the cascade proposed in Fig.2 for a 50-run Monte Carlo simulation considering a standard deviation of 0.1% in all capacitors. Note that mismatches at the additional feedback paths ( $\otimes$ ) are responsible of a large variation of the resolution in the SMASH topology, what results in its unreliable practical implementation. However, the location of the digital summation of the stages outputs inside the 1st-stage loop results in additional filtering and provides the proposed cascades with a large immunity to mismatches. As shown in Fig.4, the low sensitivity to mismatches is still maintained despite using a scaling  $d > 1$  to obtain large SNDRs.

Fig. 5 compares the SNDR obtained for the diverse  $\Sigma\Delta$  structures against the amplifier gain

in the integrators for a -6dBFS input level. Note that the required amplifier gain in the traditional MASH with  $d = 1$  and the SMASH to achieve a SNDR of 95dB are 50dB and 40dB, respectively. These values are relaxed to 30dB for the proposed cascade with  $d = 1$ .

Thanks to the implementation of unity STFs, the proposed cascade proves to have also considerably larger tolerance to non-linearities in the amplifier gain. Fig. 6 shows the SNDR of the diverse topologies against the gain non-linearity for a -6dBFS input level. For all structures the amplifiers gain is assumed to be 55dB and non-linearities are contemplated in amplifiers of the first modulator stage. Note that non-linearity requirements are also greatly relaxed for the proposed architecture.

**Conclusions:** A novel topology of cascade  $\Sigma\Delta$  modulator has been proposed. This architecture is capable of achieving large SNDRs at low oversampling with very relaxed output swing and gain demands in the amplifiers, so that it is especially suited for wideband applications in low voltage scenarios. Its efficiency relies upon two main strategies, namely: the reduction of the error cancellation logic to a single digital adder that is placed inside the 1st-stage  $\Sigma\Delta$  loop, and the implementation of unity STFs in both cascade stages. Behavioral simulation results prove the higher efficiency and robustness to mismatches of the proposed cascade compared to existing ones.

## References

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### Authors' affiliations:

A. Morgado, R. del Río and J. M. de la Rosa (Instituto de Microelectrónica de Sevilla - IMSE-CNM (CSIC/Universidad de Sevilla). Edif. CICA-CNM, Avda. Reina Mercedes s/n, 41012-Sevilla, SPAIN).

**E-mail:** alonso@imse.cnm.es

**Table captions:**

Table 1 Overload levels and output swing requirements.



**Figure captions:**

Fig. 1 SMASH modulator [1]

Fig. 2 Proposed topology

Fig. 3 SNDR versus input amplitude

Fig. 4 Monte Carlo simulation results for capacitors mismatching effects

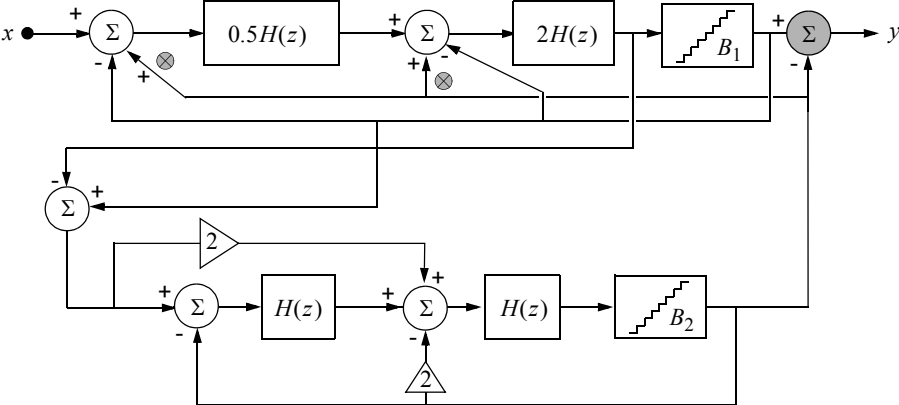
Fig. 5 SNDR versus amplifier finite gain

Fig. 6 Effect of the amplifier non-linearity on the SNDR

Table 1

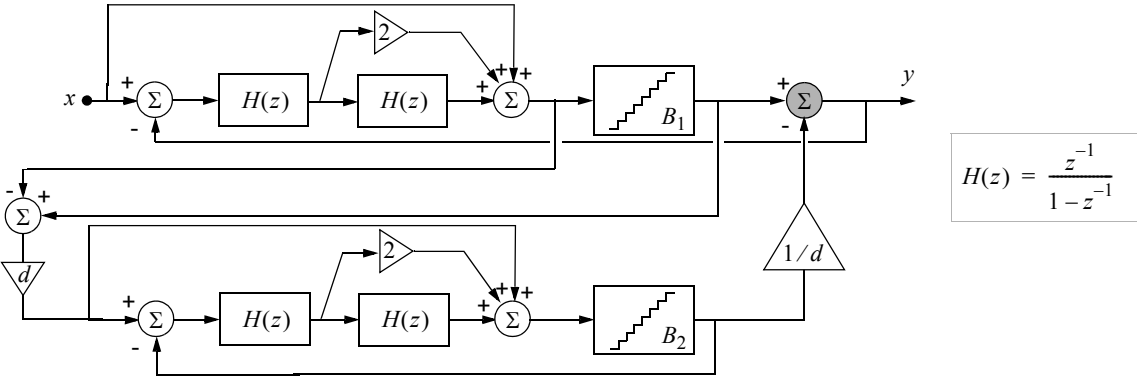
Architecture	Overload level (dBFS)	Relative Output Swing (V)			
		1st opamp	2nd opamp	3rd opamp	4th opamp
MASH $d = 4$	-0.50	0.60	0.70	0.35	0.50
SMASH	-5.50	0.75	1.24	1.49	2.69
Proposed $d = 4$	0.50	0.15	0.10	0.15	0.10

Figure 1



$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$

Figure 2



$$H(z) = \frac{z^{-1}}{1 - z^{-1}}$$

Figure 3

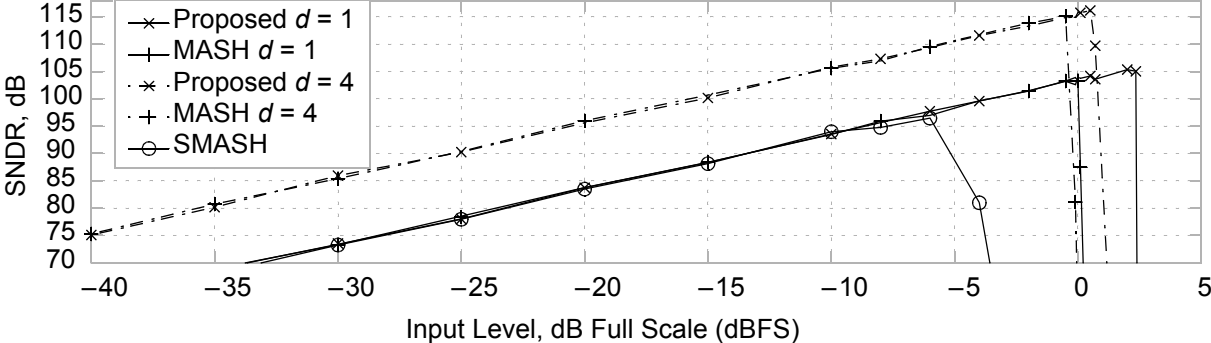


Figure 4

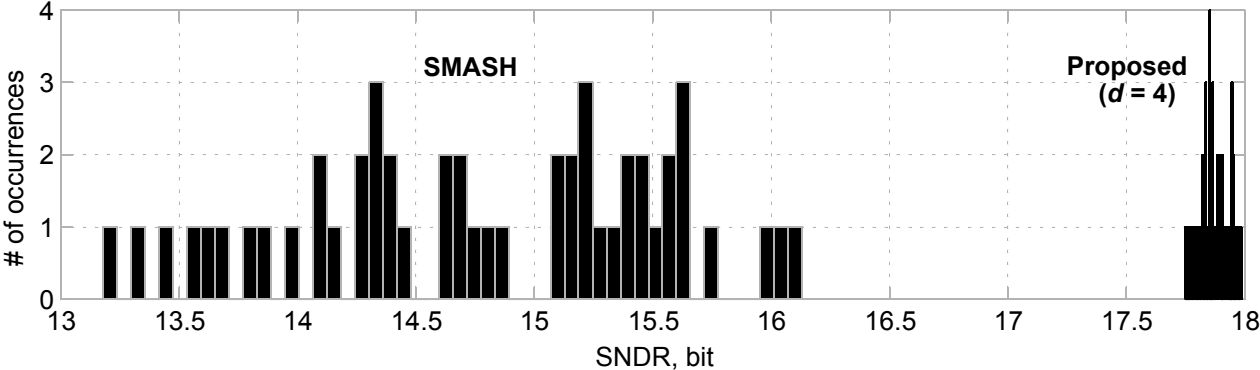


Figure 5

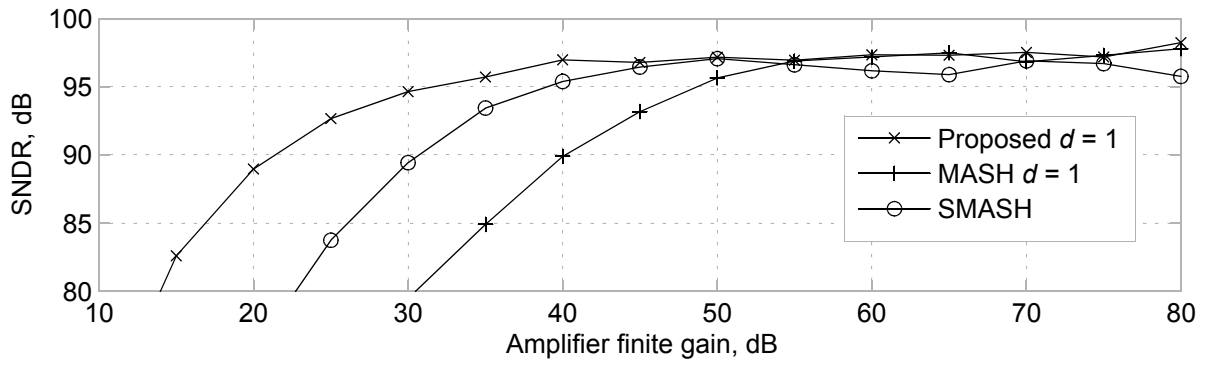


Figure 6

