Novel topologies of cascade $\Sigma\Delta$ modulators for low-voltage wideband applications

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Abstract – **This work presents two novel topologies of cascade $\Sigma\Delta$ modulators with unity signal transfer function that avoid the need of digital filtering in the error cancellation logic. The combination of these two aspects make them highly tolerant to noise leakages, very robust to non-linearities of the circuitry and especially suited for low-voltage implementations at low oversampling. Behavioral simulations are presented that demonstrate the higher efficiency of the proposed topologies compared to existing cascades intended for wideband applications.** [†1]

I. INTRODUCTION

Many new communication systems have arisen in recent years that demand for high-bandwidth $\Sigma\Delta$ modulators in low-voltage technologies [1] [2]. Since oversampling must be restricted to low values in wideband applications, a usual design choice in order to achieve the required dynamic range is to employ multi-stage noise shaping (MASH) architectures with multi-bit quantization. These $\Sigma\Delta$ topologies circumvent stability problems related to high-order loops, but are sensitive to quantization noise leakages caused by mismatches between the analog and digital signal processing in the $\Sigma\Delta$ cascade [3]. Thus, MASH modulators usually require integrators with higher accuracy than their single-loop counterparts for limiting noise leakage effects, what increases the power consumption in the amplifiers and thus the overall modulator power.

An alternative $\Sigma\Delta$ architecture that reduces the sensitivity to noise leakages of traditional MASH structures has been recently presented in the so-called Sturdy MASH (SMASH) modulator [4]. This topology, which is illustrated in Fig. 1[†2] in the case of a 2-2 cascade, replaces the error cancellation logic required in traditional MASH modulators to properly combine the stages outputs by direct feedback paths from the 2nd-stage output to the 1st-stage input (marked with $\otimes$ for clarity). The modulator output can be thus obtained from the direct digital subtraction of the two
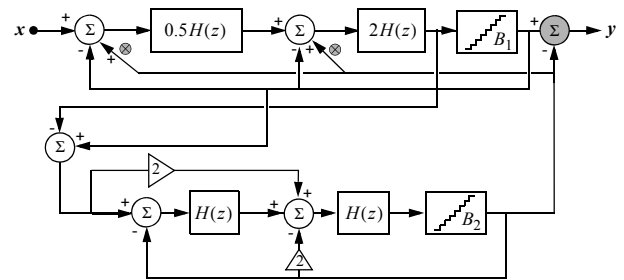

Figure 1. 2-2 SMASH modulator [4].

stages outputs, resulting in

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^4 E_1(z) - (1-z^{-1})^4 E_2(z) \quad (1)$$

where $X(z)$ stands for the input signal and $E_1(z)$ and $E_2(z)$ stand for the quantization error in the 1st and 2nd stage, respectively. Note that both quantization errors are 4th-order shaped thanks to analog filtering only, with no need of digital filtering of the stages outputs. Thus, as that in [5], the topology in [4] eliminates the matching between analog and digital filtering required in traditional MASH modulators.

Besides, the implementation of $\Sigma\Delta$ modulators with a unity <u>S</u>ignal <u>T</u>ransfer <u>F</u>unction (STF) —i.e., $STF(z) = 1$ — has demonstrated in the last years to be an excellent approach to reduce the impact of circuit non-linearities on the modulator performance, especially when considering low oversampling and a low-voltage scenario. Several $\Sigma\Delta$ topologies have been reported that apply this technique to either 2nd-order modulators [6]-[9] or to every stage of traditional cascades [10] [11].

This paper presents two novel topologies of $\Sigma\Delta$ cascades intended for high-speed, low-voltage applications which extend the underlying principle of SMASH structures to the implementation of unity STFs, while circumventing the problems detected in the former ones. Section II illustrates the direct extension of 2-2 SMASH modulators to unity STFs and addresses the main issues related to this direct approach. Section III describes the two novel $\Sigma\Delta$ topologies proposed in this paper. Behavioral simulation results are shown in Section IV that demonstrate their higher efficiency and robustness to circuit imperfections when compared to existing cascades.

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†2. $H(z)$ stands for the transfer function of a Forward-Euler integrator; i.e., $H(z) = z^{-1}/(1-z^{-1})$.

II. EXTENSION OF SMASH MODULATORS

As stated in [4], the SMASH modulator in Fig. 1 obviates the matching requirement between analog and digital filtering of traditional cascades, what allows using low-gain amplifiers with no significant degradation of the modulator performance.

Additional improvements can be obtained from extending SMASH topologies to implement unity STFs, since integrators in the $\Sigma\Delta$ modulator will ideally process quantization error only, with no trace of the input signal [7]. Thus, non-linearities associated to the amplifiers can be largely tolerated, what allows to relax their requirements of gain non-linearity and output swing and constitutes an appealing feature for low-voltage implementations.

Fig. 2 illustrates two extensions of the 2-2 SMASH modulator to unity STFs. The cascades shown in Fig. 2*a* and Fig. 2*b* are based on the 2nd-order modulators proposed in [7] and [9], respectively. Unity STFs are implemented in both stages of the 2-2 cascades in order to also reduce the output swing needed at the third and fourth integrators. Note that if multi-bit quantization is used in the stages, a scaling factor $d > 1$ can be used to accommodate the inter-stage gain, which is compensated in the analog feedback paths from the second stage to the first one and before the digital subtraction of the stages outputs.

The output of both modulators in Fig. 2 results in

$$Y(z) = X(z) - 1/d(1 - z^{-1})^4 E_2(z) \qquad (2)$$

where the overall STF equals unity and $E_1(z)$ is cancelled —contrary to eq.(1)—, while avoiding any filtering in the digital domain.
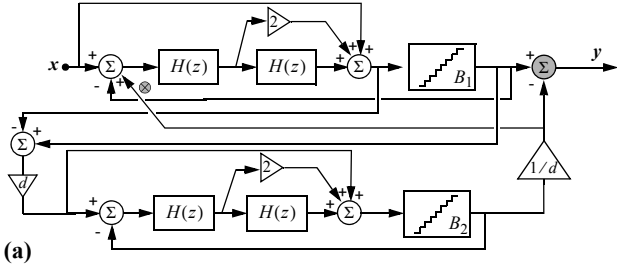
Note also from eq.(2) that using a scaling factor d that is a power of 2 will help to reduce the power of the 2nd-stage quantization error at the output and will require only a shift register before the digital subtraction. This scaling strategy can not be directly applied to the SMASH modulator in Fig. 1, since eq.(1) will modify to

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})^4 E_1(z) - 1/d(1 - z^{-1})^4 E_2(z) \quad (3)$$

thus reducing the power of the 2nd-stage quantization error at the output but not that of the first stage.

Although improving the performance of the 2-2 cascade in Fig. 1, the modulators illustrated in Fig. 2 still suffer from several drawbacks associated to the direct feedback path from the 2nd-stage output to the first stage, namely:

- They require, at least, an extra highly linear DAC in the added feedback path to the 1st-stage input.
- They are very sensitive to mismatch effects in the added feedback paths with respect to the 1st-stage analog coefficients, which cause low-order noise leakages.

III. PROPOSED CASCADE TOPOLOGIES

The drawbacks addressed for the modulators in Fig. 2 can be circumvented replacing the feedback paths from the 2nd-stage output to the first stage by directly feeding the modulator output to the first stage, as shown in Fig. 3. Note that, in both of the proposed 2-2 cascades, the digital subtraction of the quantizers outputs is performed inside the 1st-stage loop. This strategy, generally presented in [4] but not particularly applied in the proposed SMASH cascade, results in no modification of the overall output compared to
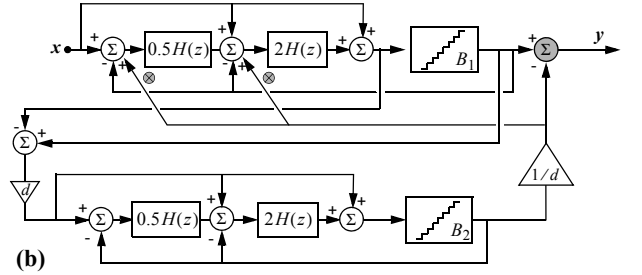

Figure 2. Extensions of the 2-2 SMASH modulator in [4] to unity STFs and inter-stage gain scaling.
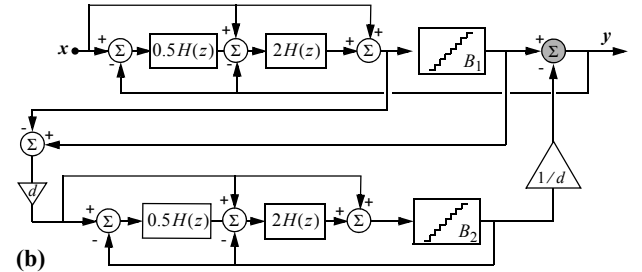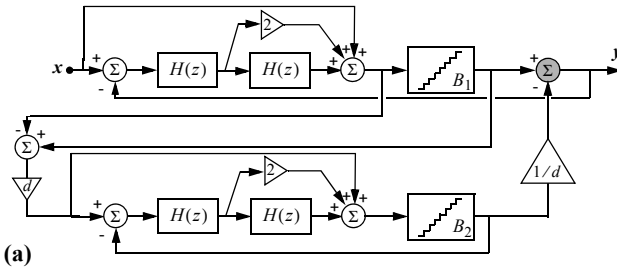

Figure 3. Proposed topologies for the robust implementation of 2-2 SMASH modulators with unity STF: (a) Proposed I, (b) Proposed II.

the one obtained in eq.(2) for the modulators in Fig. 2. This preserves the appealing features of implementing unity STFs, such as high overload levels and relaxed output swings and non-linearities for the amplifiers.

This strategy of locating the digital adder inside the 1st-stage loop eliminates the need of extra feedback paths, so that the number of linear DACs required is not increased. However, note that feeding the modulator output back to the input requires a DAC with double full scale and one more bit than the largest of the resolutions of the ADCs in the stages in order to account for the digital summation of the stages outputs. Although, as will be shown in Section IV, this location of the digital adder helps to considerably increase the robustness to mismatch of the proposed cascades compared to the SMASH 2-2 modulator in [4], thanks to the additional filtering obtained for noise leakages.

IV. SIMULATION RESULTS

The performance of the proposed cascades (Fig. 3) has been compared to traditional 2-2 cascades and to the SMASH modulator (Fig. 1) by behavioral simulation in SIMSIDES, a Simulink-based time-domain simulator for $\Sigma\Delta$ modulators [12]. All topologies operate with an oversampling ratio of 16, 4-bit internal quantizers and a 1-V reference voltage for comparison purposes with data reported in [4].

Fig.4 depicts the Signal to Noise and Distortion Ratio (SNDR) achieved by the diverse modulators versus the input level when considering quantization errors only. Curves corresponding to the proposed and traditional cascades with an inter-stage gain $d = 1$ can be directly compared with the performance of the SMASH modulator. Note that the overload level of the proposed cascades are considerably larger compared to the SMASH and also improve that of traditional cascades. As shown in Fig.4, the attainable SNDR peak can be increased by operating the
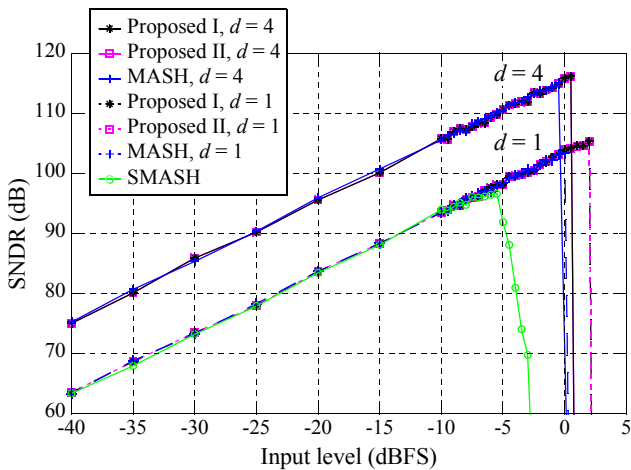
proposed topologies with $d > 1$.

The overload level of the diverse topologies is shown in Table I, together with the output swing requirements of the amplifiers along the cascades. Note that the combined usage of unity STFs and multi-bit quantization leads to a remarkable relaxation of the output swing for the proposed cascades compared to MASH and SMASH topologies, what simplifies their low-voltage implementation.

The sensitivity to noise leakages due to mismatch has been studied for the diverse architectures on the basis of Monte Carlo simulation. Fig.5 shows the SNDR at -6dBFS obtained for the SMASH modulator and the cascade proposed in Fig.3a for a 50-run Monte Carlo simulation considering a standard deviation of 0.1% in all capacitors. Note that mismatches at the additional feedback paths ($\otimes$) are responsible of a large variation of the resolution in the SMASH topology, what results in its unreliable practical implementation. However, the location of the digital summation of the stages outputs inside the 1st-stage loop results in additional filtering and provides the proposed cascades with a large immunity to mismatches. As shown in Fig.5, the low sensitivity to mismatches is still maintained despite using a scaling $d > 1$ to obtain large SNDRs.

Fig. 6 compares the SNDR obtained for the diverse $\Sigma\Delta$ structures against the amplifier gain in the integrators for a -6dBFS input level. Note that the required amplifier gain in the traditional MASH with $d = 1$ and the SMASH to achieve an SNDR of 95dB are 50dB and 40dB, respectively.

TABLE I. OVERLOAD LEVEL AND OUTPUT SWING REQUIREMENTS OF THE DIVERSE ARCHITECTURES.

Architecture	Overload level (dBFS)	1st opamp	2nd opamp	3rd opamp	4th opamp
MASH, $d = 4$	-0.50	0.60	0.70	0.35	0.50
SMASH	-5.50	0.75	1.24	1.49	2.69
Proposed I, $d = 4$	0.50	0.15	0.10	0.15	0.10
Proposed II, $d = 4$	0.50	0.10	0.20	0.10	0.20

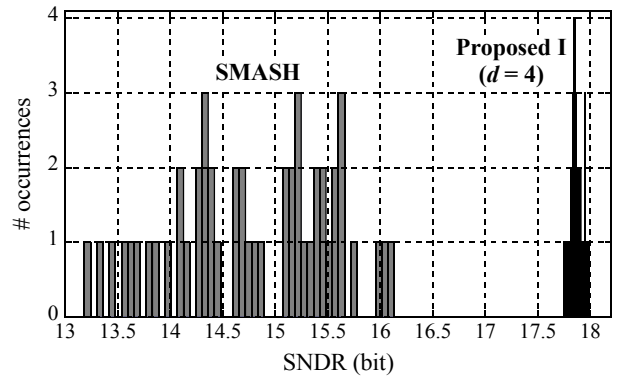**Figure 4.** SNDR curves of the diverse architectures.

Figure 5. SNDR variation of the SMASH and the proposed topology I considering a 0.1% capacitor mismatch (-6dBFS input level, Monte Carlo with 50 runs).
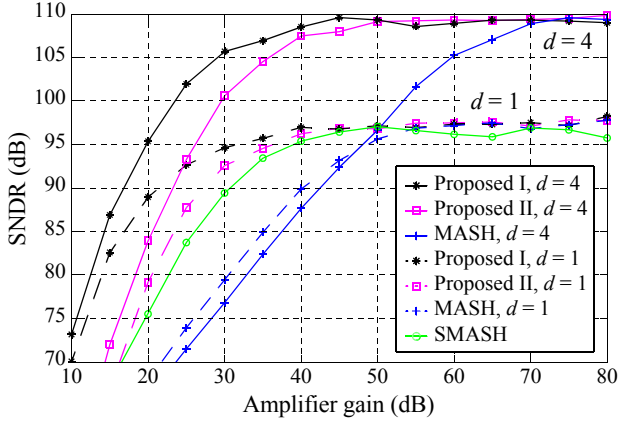
Figure 6. Variation of the SNDR with the amplifier gain for the diverse architectures (-6dBFS input level).

These values are relaxed to 30-35dB for the proposed cascades operating with $d = 1$. In addition, as shown in Fig. 6, SNDRs of 105dB can be faced with similar gain values if the proposed topologies operate with $d = 4$.

Thanks to the implementation of unity STFs, the proposed cascades prove to have also considerably larger tolerance to non-linearities in the amplifier gain. Fig. 7 shows the SNDR of the diverse topologies against the gain non-linearity for a -6dBFS input level. For all structures the amplifiers gain is assumed to be 55dB and non-linearities are contemplated in amplifiers of the first modulator stage. Note that non-linearity requirements are greatly relaxed for the proposed architectures, especially for that in Fig. 3*a*.

Some of the former results are summarized in Table II. On the one hand, the first column shows the amplifier gain required in all ΣΔ topologies to obtain an SNDR that is only 3dB lower than the ideally attainable and assuming linear amplifier gains. On the other, the second column shows the
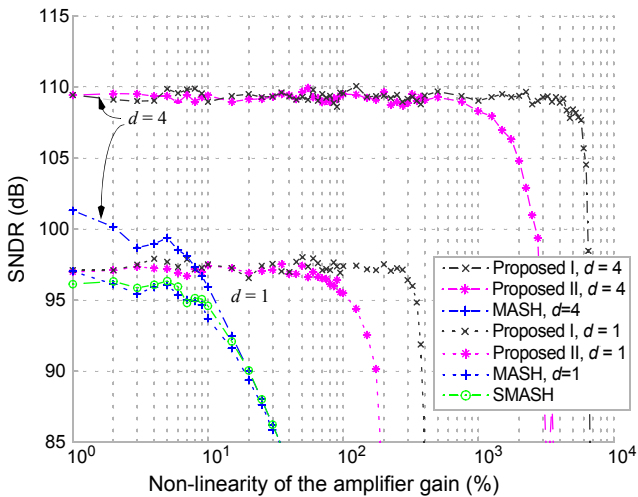
TABLE II. AMPLIFIER GAIN AND NON-LINEARITY REQUIREMENTS FOR A 3-dB SNDR DROP.

Architecture	Amplifier gain (dB)	Gain non-linearity (%)
MASH, $d = 4$	63.71	6
SMASH	36.57	15.72
Proposed I, $d = 4$	33.57	6000
Proposed II, $d = 4$	38.93	1750

linearity required for the same SNDR drop while assuming a gain of 55dB in all amplifiers. Note from the data in Table II that the performance of the proposed topology I outstands in comparison to MASH and SMASH cascades.

V. CONCLUSIONS

Two novel topologies of 2-2 ΣΔ cascades have been proposed. The architectures are capable of achieving large SNDRs at low oversampling with very relaxed output swing and gain demands in the amplifiers, so that they are especially suited for wideband applications in low voltage. Their efficiency relies upon two main strategies, namely: the reduction of the error cancellation logic to a single digital adder that is placed inside the 1st-stage ΣΔ loop, and the implementation of unity STFs in both cascade stages. Behavioral simulation results prove the higher efficiency and robustness to mismatches of the proposed cascades compared to existing ones.

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Figure 7. SNDR variation with the non-linearity of the opamp gain (-6dBFS input level, 55dB opamp gain).