Detecting single electron events in TEM using low-cost electronics and a silicon strip sensor

Running title: Detecting electrons in TEM with an SSD

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Abstract

There is a great interest in developing novel position-sensitive direct detectors for transmission electron microscopy (TEM) that do not rely in the conversion of electrons into photons. Direct imaging improves contrast and efficiency, and allows the operation of the microscope at lower energies and at lower doses without loss in resolution, which is especially important for studying soft materials and biological samples. We investigate feasibility of employing a Silicon Strip Detector (SSD) as an imaging detector for TEM. This device, routinely used in high-energy particle physics, can detect small variations of electric current associated with the impact of a single charged particle. The main advantages of using this type of sensor for direct imaging in TEM are its intrinsic radiation hardness and large detection area. Here, we detail design, simulation, fabrication and tests in a TEM of the frontend electronics developed using low-cost discrete components and discuss the limitations and applications of this technology for TEM .

Introduction

In electron microscopy electrons are accelerated, interact with a sample and a sensitive film or a pixelated detector (a camera) is used to collect the electrons forming an image of the sample [1-2]. The most common technology used for imaging cameras is based on charge-coupled-devices (CCD); however this technology is not radiation hard or *radhard* and electrons must be converted first into photons using a scintillator and optical coupling. In contrast with the indirect approach, novel direct detectors are being developed which do not need scintillators or optical coupling, and therefore can significantly improve resolution, speed and sensitivity [3]. Although multiple *scattering* can still decrease the effective resolution of a direct camera, direct sensing in combination with back-thinning can overcome this problem and provide a

much improved Detector Quantum Efficiency (DQE) and Modulation Transfer Function (MTF). And if the detector is operated in counting mode, then the dynamic range (DR) can also be extended [4-11].

For beam sensitive samples like biological samples it is a must the use of lower electron energies and electron doses to reduce beam damage in TEM [5]. If electrons can be detected directly without using scintillators/coupling then the efficiency of the camera system will increase. This means that if noise is kept low, lower electron doses on the TEM sample can be used and still have a suitable signal-to-noise ratio at the image. Moreover, lower electron beam energies can be used without degrading resolution, effectively reducing the PSF (point spread function) at the sensor because the penetration depth of the incoming electron is lower [12,13].

There are several technologies suitable for the design of direct detectors that can be readily applied to TEM, such as monolithic active pixels sensors (MAPS) in complementary metal-oxide-semiconductor (CMOS) technology and *radhard* layout [14-18], BiCMOS technology [19], hybrid circuits [20,21], or *Silicon-on-Insulator* (SOI) technology [22,23]. SOI in particular has the advantage that it has higher speed than conventional CMOS, and also it can be thinned down more deeply. Here we explore the application of Silicon Strip Detectors (SSDs) to TEM, a technology that has been traditionally used in high-energy particle physics because the sensor and readout electronics are physically separated, and therefore it is intrinsically very *radhard*, and can be fabricated on large surface areas with very flexible geometries [24-26]. The performance of a SSD sensor for its application in TEM depends greatly on the energy of the electron beam because of the soft interaction between the primary electrons and the sensor. Monte Carlo simulations show that the detection efficiency of thin SSDs comply with TEM requirements, provided that an adequate design with an optimised thickness and strip pitch is employed [8].

The simplest SSD is the single-sided one that consists of a semiconductor substrate with a number of strip-diodes very close to each other, and an ohmic contact at the backside. The semiconductor bulk is n-type doped silicon of high resistivity, with p+ electrodes that properly biased conforms the the sensitive area. A more complex employs electrodes at both sides of the die, and these sensors are called double-sided SSD (DSSD) (see Fig. 1). Bi-dimensional information on the impact position of a particle is readily provided with such devices [27,28]. As illustrated in Fig. 1a, parallel electrode strips cross the full length of the sensor area on the upper side of the die, and correspond to X-coordinate. The opposite side of the sensor also contain parallel electrode strips oriented at 90 degrees and correspond to the Y-coordinate. The overall structure is equivalent to a distributed array of diodes. When the appropriate voltage is applied, these diodes are placed under reverse bias conditions, each producing a large depletion zone, and acting together similar to an array of capacitors of value C_b. When an electron impacts the sensor, it loses energy and thus generates mobile charge carriers in the depletion region. The electron loses its energy gradually along its trajectory, which can span hundreds of micrometres (see Fig. 1b), generating in turn a cloud of electron-hole pairs, until the particle is completely absorbed or exits the sensor. The bias voltage applied to the sensor induces an electric field across the depletion region, in addition to the built in voltage, forcing electrons and holes to drift towards opposite sides of the sensor until they are collected at the respective electrodes. These mobile charge carriers induce an electric current that can be amplified, thus allowing the detection of the event, and also the measurement of the energy deposited by the particle.

The detection approach of DSSD sensors provides an ideal technology for imaging in TEM, provided that sufficient speed is achieved by the readout electronics to detect single electrons under typical TEM operating conditions. In this paper we demonstrate feasibility of front-end readout electronics for detection of single electrons using a commercial DSSD sensor. We have

calculated the amplitude and frequencies of electrons expected to reach the detector in a typical TEM experiment to derive specifications for the design and fabrication of a front-end circuit using discrete electronic components. The front-end schematics have been designed to meet these specifications, and the boards have been manufactured and connected to *one* side of the DSSD sensor. Single electron events have been observed using this proof-of-principle system using a Philips CM200 TEM operated at 200 keV. Also, we discuss the limitations and applications of this technology for TEM .

Methods and Results

1. System Architecture

Whilst DSSD devices do not have pixelated geometry, they are suitable for detecting the position of an event. Under the assumption that electrons will arrive to the sensor *one at a time* (see section 2.3 below), when electric signals are detected at two strip/electrodes on opposite sides of the sensor within a short temporal window, they can be safely considered to be caused by the same electron. Such coincident pulses between two strips/electrodes along X and Y directions provide impact coordinates of single electrons, and the sum of such events at each intersection position provides the image.

When the required number of strips is low, the front-end circuit can be implemented using discrete electronics with temporal window resolutions down to 10 ns [29], and/or field-programmable gate arrays (FPGAs). For example, a low-cost FPGA *Spartan* from *Xilinx* has been used with a DSSD detector of 128 channels monitored at a speed of 30 kHz [30]. When the required number of strips is high, the common strategy is the integration of the readout circuitry within an application-specific integrated circuit (ASIC) in CMOS technology [31-38].

Fig. 2a illustrates overall architecture of an asynchronous circuit for a position-sensitive counting detector using a DSSD, where the main components are:

(1) front-end circuits connected to each electrode of the DSSD for the amplification/conformation of the electric pulses generated in the sensor,

(2) coincidence detection module, and

(3) a communication module.

Each strip of the sensor is connected to a front-end circuit, identical for all N strips of the vertical (p-type) and horizontal (n-type) sides of the sensor. At both detector sides, a simple one-hot to binary encoder can be employed to codify which of the strips outputs a pulse at a given time instant. The position is encoded in a binary word such as if there are N input lines the word has B bits so that $N=2^B$.

When an electron impacts the sensor, the amplitude of the generated current pulse will be highest at the closest electrodes on each side of the sensor. The pulsed signal is amplified and digitized at the corresponding front-ends of the two electrodes. These pulses are then processed in the coincidence detection module (Fig. 2b) to check if they correspond to same electron event. The coincidence detection module continuously samples the output of the encoders, and detects the moment in which two digital words different from zero are generated within the same correspondence window. Logic OR gates can be used to monitor changes in the output of either the X-position or Y-position encoder. A simple 2-input logic AND gate can be employed to detect the correspondence. If the AND-gate outputs a logic 1, it means that words X and Y correspond to the same event and therefore define the respective horizontal and vertical coordinates of the impact of an electron. The output signal of the coincidence module in Fig. 2 for interrupt request (IRQ in Fig 2) indicates the streamer block to transfer these coordinates to a host computer for further processing.

2. System Specifications

2.1. DSSD sensor

In this study, we have used a commercial DSSD sensor, the *BB1(DS)-1000* fabricated by *Micron Semiconductors Ltd.*, shown in Fig. 2a. The DSSD has 40 x 40 strips at opposite sides and oriented orthogonally. The silicon has a thickness d = 1 mm, and resistivity R = 5 kΩ. The strips have a current leakage of I_L = 4 nA at room temperature, length $l = 40$ mm, pitch $p = 1000$ μm and width $w = 800$ μm. Using these specifications we can calculate electrical parameters needed to optimise the design of readout electronics, such as the total capacitance of the sensor under reverse bias C_d, the sum of inter-strip capacitance C_{ss}, and backplane (or bulk) capacitance C_b [29]. C_{ss} is approximately proportional to the peripheral dimensions of the strips $2(l + w)$ and if $w << l$ then $C_{ss} \approx 2lC'_{ss}$ with

$$C'_{ss} = \left(0.03 + 1.62 \, \frac{w + 20}{p}\right) \left[\frac{pF}{cm}\right] \qquad (1)$$

where *l* is the length of the strip in cm, and w is the width and p is the strip pitch in μm [38].

And backplane capacitance is

$$C_b = \varepsilon \varepsilon_0 \, p \, l/d \qquad (2)$$

where ε=11.6 is the relative dielectric constant of silicon and d is the distance between the junction and the end of the depletion region. Using the dimensions of the sensor and Eqs. (1) and (2) the total capacitance is $C_d = C_{ss} + C_b = 15 \, pF$.

The dimensions (width and length) of the metal contacts are the same as the strips, therefore the resistance of the metal electrodes is $R_s = \rho w t l$, with ρ the resistivity, and t the thickness of the metal contact of the strip. For sputtered aluminium $\rho \approx 4$ μΩ·cm and t = 1 μm, which gives for this sensor $R_s = 2\Omega$.

2.2. Free charge generated by the impact of one electron

We can now calculate the amount of charge generated by the impact of one single electron in the SSD sensor. The charge induced in a semiconductor is a function of the incident particle energy and the detector material, and is given by

$$Q_d = \frac{E\,e}{\epsilon} \qquad (3)$$

where E is the energy in eV of the incident radiation, e is the charge of an electron (1.6 x 10[-19] Coulombs), and ϵ is the amount of energy required to produce an electron-hole pair. In silicon ϵ is approximately 3.6 eV. For a typical TEM experiment operated at 200 keV and the thick DSSD used here, an incident electron fully absorbed by the sensor is generating a total charge of 8.8 fC.

Fig. 1b shows a Monte Carlo simulation, illustrating the trajectories that electrons accelerated at 200 keV undertake in silicon [39]. The multiple scattering means that incident electrons follow irregular trajectories and that randomly shaped clusters of electron-hole pairs are generated by each event, which may extend laterally many microns in the silicon. Although the sensor we used here is 1.000 μm thick, simulations show that 200 keV electrons will be generally absorbed after travelling an average distance of 200-250 μm, and also that a percentage of electrons will be backscattered and thus depositing only a fraction of their energy.

2.3. Frequency of impacts

We can calculate the speed required for the detector to operate as a counting device, which is equivalent to calculating how many electrons are in the TEM column at any given time as described in reference [40]. A reasonable approximation is that electrons are generated at the

electron gun at regular intervals of time. For a typical current of 1 nA (or equivalently $6.25 \ x \ 10^9 \ electrons \cdot s^{-1}$) the linear density of electrons in the TEM column n_e is

$$n_e = \frac{6.25 \ x \ 10^9}{v} \qquad (4)$$

where v the speed of the electrons. If electrons are accelerated at E = 200 kV, their speed is $v = 0.695 \ c$, with c the speed of light. Substitution in equation (4) gives n_e = 30 electrons m^{-1} nA^{-1} , hence the average distance between two consecutive electrons is $\overline{\Delta z} \cong$ 3.3 cm. This means that electrons in a TEM for a current of 1 nA will impact the sensor one at a time and the average arrival time between successive electrons will be $\Delta t_{min} = \overline{\Delta z}/v = 3.3 \ \times \ 10^{-2}/2.085 \ \times 10^8 = 1.44 \ \times 10^{-10}s \ \cong$ 16 ns.

In practice, the frequency of electron impacts will depend on the total sensing area, illumination conditions, beam current, geometry of the sensor and the type of signal being measured (coherent scattering, Rutherford scattering, inelastic scattering, etc.). For example, a typical current density in TEM bright-field mode may be 0.1 nA/cm^2 what gives 160 ns between electron events per cm^2 of sensing area. The active sensing area of one strip of the DSSD sensor used in our research is A$_{strip}$ = 40 mm x 1 mm = 0.4 cm^2, therefore, under typical bright-field conditions electrons will impact one sensor strip every 160 / 0.4 = 400 ns. Because here we are interested in counting electron pulses, we have used this temporal value as a reference for design specification, i.e. the electronics shall operate at a frequency f ≥ 1/400 ns or 2.5 Mhz.

3. Front-end electronics

3.1. Circuit blocks

Now we describe the electronic circuit that, together with the DSSD sensor, must provide a narrow digital pulse each time an electron impacts close to the respective strip [25,28]. Fig. 3a shows the functional blocks of a typical front-end circuit used with semiconductor detectors, where the sensor converts the energy of incident radiation into electric pulses that are amplified by the preamplifier and shaped by a signal processing block also called shaper. The shaper circuit has the mission of increasing the signal-to-noise ratio (SNR), which is achieved by limiting the bandwidth and which in turn changes the time response (shape) of the pulse. There is therefore a trade-off between the SNR and the speed of the system. The end block in Fig. 3a is used for the digitization of the analogue pulse for further processing and/or transmission of data.

Fig. 3b shows the circuit schematic of the designed front-end. Resistance R_B is used to bias the sensor, which is represented here by its capacitance C_d (equals to the capacitance of the reverse-biased diode junction). It is common to connect the sensor to the preamplifier input through a coupling capacitor (C_c in the diagram) [41]. This capacitor isolates the input of the preamplifier from any DC bias that might lead to saturation, and also from the leakage current of the sensor. In this way shifting and possible fluctuations of the baseline are minimised.

Just after the coupling capacitor, the first stage of the circuit is the preamplifier, designed to integrate the electric charge injected from the sensor and to amplify the voltage built on C_d. This is the most critical block because it determines the overall sensitivity the system. The preamplifier consists on an operational amplifier configured as a charge-sensitive amplifier (CSA), as shown in Fig. 3b. The CSA employs a negative feedback network with a capacitor C_f, and a resistor R_f. For the CSA to act as a current integrator, the values of R_f and C_f of the CSA must be chosen so that the time constant $T_f = R_f C_f$ is high. At the same time the total input capacitance must be low to minimise noise, therefore C_f must be small. However this value is set in accordance to the sensor capacitance, and therefore must be sufficiently large to

minimise cross-coupling between strips. On the other side, a high value of R_f is required to minimise thermal noise. As shown in Fig. 3b, the feedback network of the CSA was chosen with a time constant of 500 μs, with C_f = 0.5 pF and R_f = 1 GΩ (a large feedback resistance also minimises thermal noise). In first approximation if the resistance of the bias R_B is high, Johnson noise is reduced. Moreover, if $R_B \gg T_f/C_d = 33$ MΩ most of the current of the sensor will flow to the input of the preamplifier and sensitivity of the system will not be degraded.

In order to build the preamplifier stage with low-cost commercial operational amplifiers, we have considered three candidates, namely:

(1) OPA657, 1.6 GHz FET from *Texas Instruments*;

(2) LMH6624, 1.5 GHz, from *National Semiconductors;* and

(3) OPA847, 3.9 GHz, from *Texas Instruments*.

Given that the intrinsic noise of a preamplifier will depend mainly on the transistors used at the input stage, we have chosen OPA657, which is a low input-voltage noise ($e_{na} = 4.8\,nV/\sqrt{Hz}$) operational amplifier popular for low-noise transimpedance. It has a high 1.6 GHz gain bandwidth product that will render more than 10 MHz signal bandwidth at gains of 160 V/V (44dB). Its junction gate field-effect transistor (JFET) input contributes virtually no current noise, resulting in a negligible input-current noise of $i_{na} = 1.8\,pA/\sqrt{Hz}$ over a 10 MHz bandwidth.

After the preamplifier stage in Fig. 3b, the next block is the shaper where the signal is filtered and amplified in two stages using two operational amplifiers contained in the integrated circuit AD812AR from *Analog Devices*. The opamps are current-feedback amplifiers that allow higher bandwidth even with high gains, at the expense of more noise, but are also more stable and easier to compensate.

Since noise is distributed over the entire frequency spectrum, the bandwidth must be reduced with a band pass filter to improve the SNR of the circuit, which in turn increases the duration of the pulse. However, for the case of this application, the pulses must be processed at high speed in order to discriminate locations of the electron events. If the pulses in the electronic system are processed too slowly, or if they are too wide, they will overlap (pile-up) and it will not be possible to determine the X and Y coordinates of each impact.

The simplest band pass filter consists of resistors and capacitors forming a differentiator (CR) followed by an integrator (RC). The band pass filter can be obtained from a combination of the intrinsic low-pass characteristic of the CSA amplifier and the use of passive first order differentiators (see Fig. 5a) to a satisfactorily time constant of $T_s = 1\,k\,\Omega \cdot 100\,pF = 100$ ns. The shaper also amplifies the signal 8.6 times in each operational amplifier of the AD812AR integrated circuit and outputs an amplitude level that can be used as input for the analogue-to-digital (A/D) converter. This A/D converter consists of a fast comparator AD8611 from *Analog Devices* that has 4 ns propagation delay and that can operate up to 100 Mhz. The voltage reference required at the input of the comparator was set with a variable resistive voltage divider.

3.2. Noise vs speed

Noise present at the input of the CSA preamplifier determines the sensitivity of the circuit, because it will be amplified by subsequent stages [41-45]. Noise in charge-sensitive preamplifiers is generally controlled by five components:

- transistors of the input stage of the preamplifier,
- total capacitance seen at the input C,
- bias resistance R_B,

- serial resistance at the input (here we have considered only the strip resistance, R_s), and

- diode dark current I_d.

In our calculations we have considered the spectral densities of only the most important sources of noise. *Shot noise* i_{nd} of the sensor current is a source in parallel to the sensor capacitance. The Johnson noise of the resistance of the strip and of the bias resistor can be modelled as voltage and current sources e_{ns} and i_{nb}, respectively. Finally, the operational amplifier will have its own white type sources of voltage and current noise, e_{na} and i_{na} respectively, with values given by the manufacturer of the integrated circuit [47].

The spectral densities of all these sources can be described as

$$i_{nd}^2 = 2q_e I_d; \quad i_{nb}^2 = 4kT/R_b; \quad e_{ns}^2 = 4kTR_s \quad (5)$$

Discarding the contribution of the flicker noise, as low-frequency components will be filtered by the shaper, the total noise at the input of the CSA, expressed as the equivalent charge for an SNR equal to one, i.e. the equivalent noise charge (ENC), is given by:

$$Q_n^2 \cong (2q_e I_d + 4kT/R_b + i_{na}^2) T_s + (4kTR_s + e_{na}^2) C^2/T_s \quad (6)$$

where T_s is the shaping time. The first term includes the different current noise sources i_n^2, and the second term includes the voltage noise sources e_n^2 [28]. Equation (6) shows that noise can be reduced by minimising the spectral density of input noise of the preamplifier e_{na}^2 and i_{na}^2, and by reducing the input capacitance C (e.g. decreasing C_f, C_d, capacitance of the connectors). This can be achieved by reducing the diode bias, reducing R_s, increasing R_B, lowering the temperature T, or optimizing T_s that determines the bandwidth, and therefore the maximum speed of the circuit and the SNR.

Fig. 4 shows the relation between total noise, physical and electrical properties of the sensor, and noise of the preamplifier. The software outputs four curves (Fig. 4) of the dependence of noise with shaping time (a) and sensor capacitance (b), and capacitance of the sensor (c) and

noise of the sensor (d) for optimum T_S. T_S is optimum when current and noise contributions are equal, what corresponds to the minimum of curve (c). For the geometry and electrical characteristics of the sensor that we are using, the DSSD used here adds 1.070 e⁻ to the ENC, a value that is typical for this type of sensors. When the noise of the preamplifier is included, ENC reaches around 3300 e⁻ for an optimum shaping time (minimum noise) of 40 ns.

But this optimum time does not take into account the collection time of charge carriers that is a function of bias voltage. If the sensor operates at full depletion the collection time of electron and holes can be estimated as

$$t_c \approx \frac{\bar{z}}{v} = \frac{\bar{z}}{\mu \overline{\mathrm{E}}} = \frac{\bar{z}\,d}{\mu V_b} \qquad (7)$$

where $\bar{z}$ is the average distance that an electron will go across the bulk before being absorbed (approximately 250 μm, see Fig. 1B), v is the average speed of the electrons (or holes) generated in the sensor, μ is the mobility of electrons or holes in silicon, d the thickness (1 mm) of the sensor, $\overline{\mathrm{E}}$ the average electric field and V_b the bias voltage applied (we have employed 140 V). Substituting these values in equation (7) the average collection time for electron and holes will be 13 ns and 40 ns, respectively.

Summarising, we are interested in using a DSSD detector that operates with high-counting rate. Noise is minimum for $T_S \approx 40$ ns (see Fig. 4), counting rate must be slower than collection time for holes ($T_S > 40$ ns), and the electronics must be fast enough to measure the electron events without pile-up of pulses, i.e., $T_S < 400$ ns (see section 2.3). Taking into account all these considerations the front-end was designed with a high-pass CR filter (see Fig. 3) having a characteristic time $T_S = R \cdot C = 1\,k\Omega \cdot 100\,pF = 100$ ns.

4. Electric simulation

Before fabricating the circuits we simulated the transient behaviour of the CSA, the shaper and the comparator using *Tina* and *MultiSIM* software programs. These are *spice-like* simulators supplied by the electronic component manufacturers *Texas Instruments* and *Analog Devices* respectively. Each strip of the SSD sensor was modelled as a diode with a capacitance of 15 pF and a reverse bias current of 5 nA.

Fig. 5a shows a Bode plot of the output of the preamplifier, and the band pass characteristic seen at the outputs of the 1st and 2nd amplifiers of the shaper. One of the big advantages of the CSA configuration is the relatively simple scheme that is required for testing the response of the circuit; in fact it only requires the use of a voltage source and a capacitor (C_T in the Fig. 3). Transient simulations have been done applying voltage squared pulses with a leading edge of 30 ns, an amplitude ΔV =10 mV and a width of 300 ns to the test capacitor C_T of 0.5 pF, which is equivalent to injecting a charge Q_i=5 fC at the input of the preamplifier. Fig. 5b and 7b shows the waveforms resulting of transient simulation at the output of the shaper. Analogue pulses with 100 ns width are measured as expected at the output. The digital output (output of the comparator) is also shown, and it is high whenever the analogue pulse crosses over the selected threshold.

5. Experimental tests of the front-end with 200 keV electrons

Prototypes were built soldering surface mount (SMD) components and using a four-layer printed circuit board (PCB) (Fig. 3c). It is essential in this application to reduce the capacitance introduced by wiring, and also to minimise acoustic pickup noise, ground loops, and radio frequency pickup. One of the layers was exclusively dedicated to grounding and another for the low-voltage positive supply. Parasitic capacitance was minimised with careful PCB layout,

reducing connector distances and placing decoupling capacitors close to the power supply pins of the preamplifier, which must be located as close as possible to the detector.

The DSSD detector was connected to a block of eight front-end circuits (Fig. 6a). Because the electronics will operate in high-vacuum, copper stubs were contacted with thermal conductive glue to the integrated circuits of the electronics to help dissipating heat. The electronic circuit operates with a symmetrical supply of ± 5 V. For biasing the DSSD at the operating plateau of 200 V, we built a high-voltage power supply of ± 70 V using linear transformers to avoid the noise typical in switched power supplies. The complete system including power supplies is shown in Fig. 6b. The system was tested inside a Philips CM200 TEM operated at 200 keV using a case of steel with high-vacuum seels high-vacuum (see Fig. 6c) and thick enough to shield the circuit from X-rays.

Fig. 7 shows experimental results of the analogue signal at the output of the shaper. Figs. 7a-b compare simulation and experimental pulses respectively. The experimental pulses correspond to an electric charge of about 5 fC and a temporal width of 150 ns, a value that is larger than the 100 ns used as design specification.

We can calculate the expected amplitude of pulses produced by one electron at the analogue output of the front-end. The amplitude of the output voltage of the CSA preamplifier V_o, is given by

$$V_o = \frac{Q_i}{C_f} \qquad (8)$$

where Q_i is the charge (number of e-h pairs) released in the sensor and C_f the feeback capacitor. Using the value of Q_d calculated from Eq. (3) the amplifier sensitivity at room temperature with C_f = 0.5 pF will be 17.5 mV/electron. The analogue signal at the output of

the shaper is amplified 74 (8.6 x 8.6) times, therefore the pulse generated by an electron of 200 keV absorbed completely should have a maximum amplitude of 1.3 V.

Electrons of the TEM can be considered approximately mono-energetic but most experimental pulses (Fig. 7c-d) have amplitudes between 0.3 and 1.3 V. Smaller peaks below the 1.3 V reference level can be explained considering that a fraction of the electrons will be backscattered generating less charge in the sensor. Moreover, imperfect biasing and capacitive matching between sensor and electronics can result in cross-coupling between neighbouring strips that would degrade collection efficiency of the electrodes and charge redistribution, resulting in peaks with much lower amplitudes. In fact, Fig. 7c shows that when the electron dose changes, the baseline of the output signal shifts $\cong 150$ mV, which indicates that the design of coupling between sensor and electronics was imperfect. Moreover, peaks with amplitude up to 1.9 V were sporadically observed.

Fig. 7b also shows the presence of a sine wave oscillation of the baseline with a frequency of approximately 1 MHz and $V_{RMS} = 50$ mV. Shaping time of the electronic circuit determines at which frequency the amplifier gain peaks and it is given by $f \approx 1/2\pi T_s$. The circuit has a shaping time $T_{s,experimental} = 150$ ns (Fig. 7b), meaning that the noise gain will be maximum at 1.06 Mhz, and which is in the range of radio-frequency, RF. Therefore RF pickup is the most probable source of this noise, most likely because of unsatisfactory metallic shielding of the system or coupling through cables interconnecting the detector output to the oscilloscope and power supplies outside the TEM.

Conclusions

We have designed and tested a prototype of electronic circuit connected to a DSSD, with the goal of detecting single electron events of 200 keV in a TEM. As we were interested in high-

speed counting, i.e. not in energy measurements, we have designed a high-bandwidth circuit at the expense of electronic noise. We have measured individual peaks with amplitude and duration very close to the specifications, well within expectations of individual electrons impacting the sensor. The electric charge generated by the impact of individual electrons was amplified, shaped and digitized with a low-cost electronic circuit fabricated with discrete electronic components and operating at a frequency of f=1/150 ns or 6.6 MHz.

Whilst the results shown here demonstrates DSSD feasibility for detecting energetic electrons we measured also cross-coupling between first-neighbour strips and the geometry of the sensor (thickness and pitch) must be optimised for its application to TEM. In fact, for a given electron energy and carefully designing pixel pitch and sensor thickness the efficiency of DSSDs imagers can be very high [8]. For example, at 200 keV a value of DQE of 75% can be obtained with a 50 μm thick DSSD and a pixel pitch of 100 μm, which is well above that of the imagers currently used in TEM (approximately 30% for direct CMOS pixelated detectors like FEI Falcon and Gatan K2). But the design of DSSD as imaging device with high pixel resolution is challenging if high electron doses are used. In this case and because the strips extend all the length of the sensor readout electronics has to operate at very high speed in order to cope with ghost counts. Nevertheless, DSSDs could be advantageous in terms of design flexibility, easiness of fabrication and cost of the sensor for applications requiring low spatial resolution (≤ 1k x 1k) and using ASICs for the electronic readout.

Nowadays, there is a great interest in segmented detectors for scanning TEM (STEM) with potential application in techniques like differential phase contrast (DPC), strain analysis by nano beam electron diffraction (SANBED) or annular bright-field (ABF) [47-49]. STEM detectors available in the market use a single crystal Yttrium Aluminum Perovskite (YAP) or Yttrium Aluminum Garnet (YAG) scintillator and a solid quartz light pipe extending from the scintillator (inside the vacuum) to the entrance of a photomultiplier and achieve >90% DQE [50]. SSD

technology could be used instead with high DQE with the advantage of being more compact because does not requires optical conversion neither photomultiplication.

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Figures
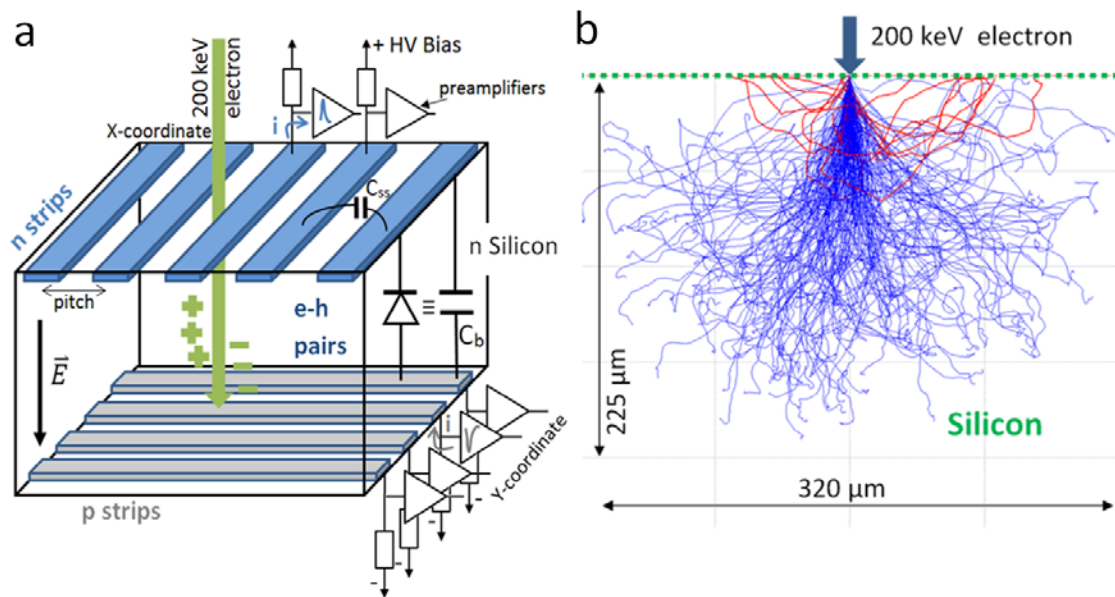
Fig. 1. (a) Schematic diagram of a DSSD with orthogonal p and n-doped strip diodes at opposite sides of the device. With the reverse bias applied, strip diodes have a deep depletion zone and act similar to capacitors C_b. As an 200 keV electron impacts the sensor, it generates electron-hole pairs along its trajectory and induces a current pulse in the nearest strip and respective amplifier. (b) Monte Carlo simulation of 10 trajectories of 200 keV electrons in silicon, illustrating that the interaction volume occupies several 100 μm. A fraction of electrons are backscattered and do not deposit all of their energy in the sensor.
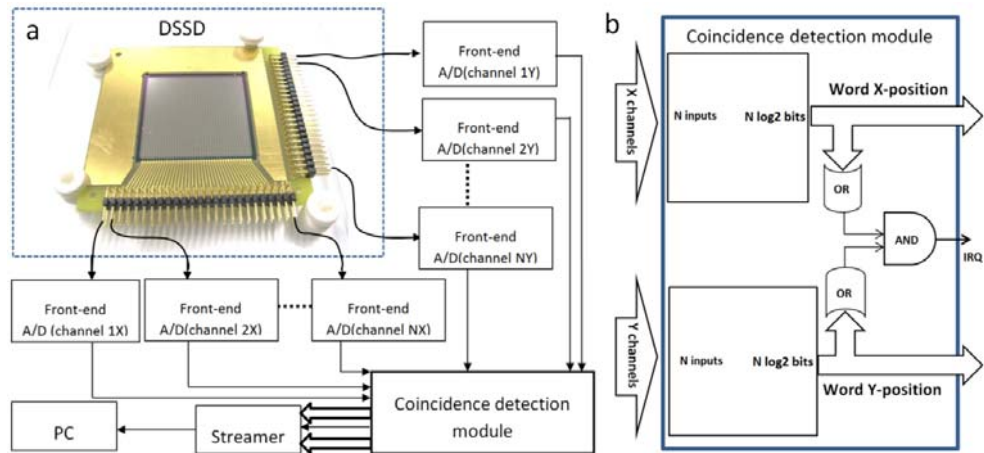
Fig. 2. (a) Block diagram of system architecture for a position-sensitive counting detector using a DSSD. Each strip is connected to one front-end circuit like the one shown in Fig. 3. The strips at each side of the detector are connected to respective X and Y modules that encode position of triggered strip to a binary word. (b) A coincidence detection module filters simultaneous triggers on the X and Y channels, and signals IRQ high when a particle is detected. IRQ output signals to an external communication module (e.g. a streamer) that the two-dimensional position of a detected electron is available for readout.
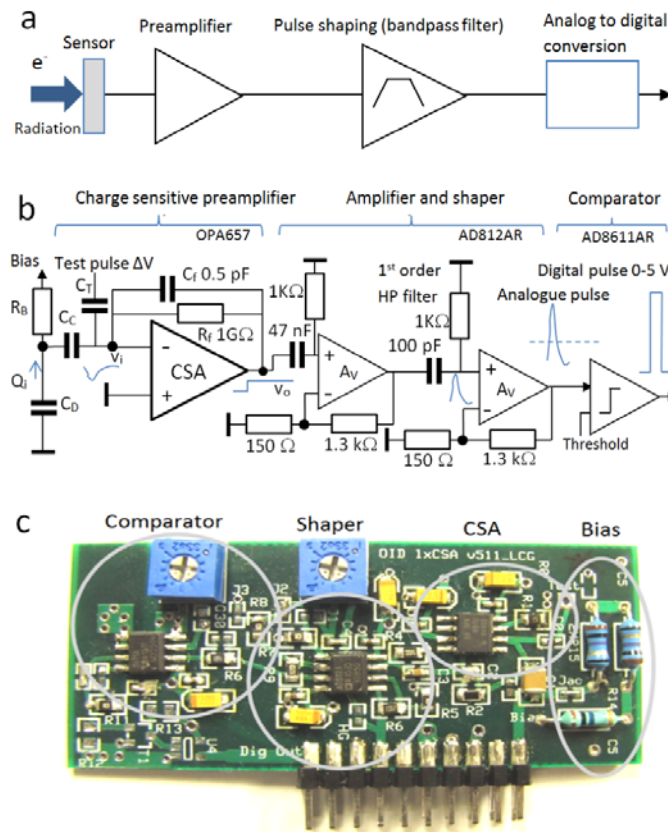
Fig. 3. (a) Functional blocks of a generic semiconductor detector front-end. Bandpass filtering is generally obtained by combining the low-pass characteristic of the transfer function of preamplifier with a high-pass filter at the second stage. (b) Electronic circuit of the front-end module used to sense, amplify and digitalise pulses at the strips of the DSSD. The main blocks are the charge-sensitive preamplifier, the shaper and the analogue-to-digital converter. Details of the biasing of the sensor, passive filters, and feedback networks of the amplifiers are drawn. (c) Photograph of the mounted PCB of the front-end circuit fabricated with low-cost discrete electronic components.
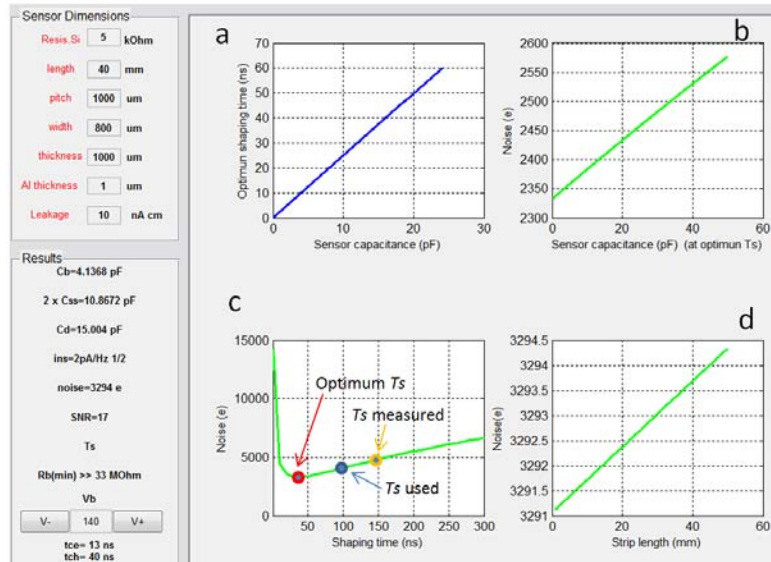
Fig. 4. Graphical user interface of software developed to model a range of design parameters as a function of the sensor specifications.
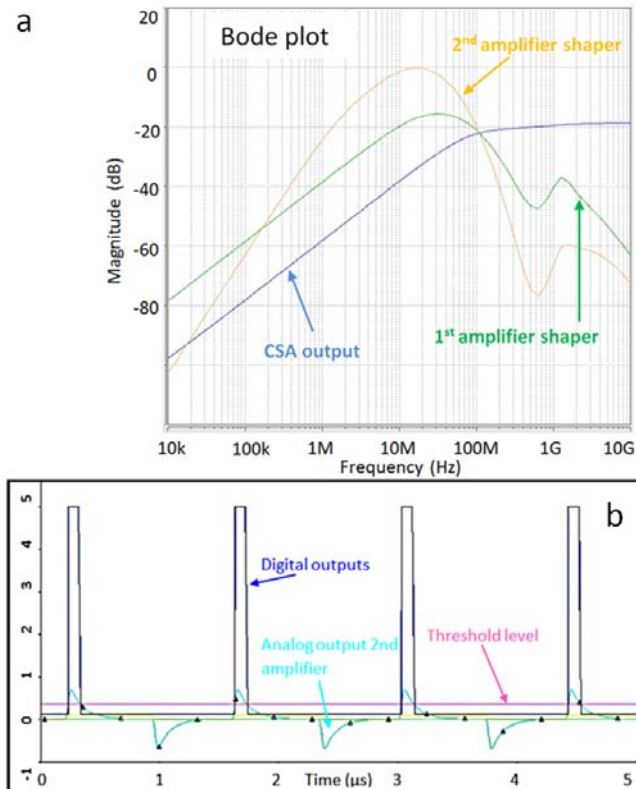
Fig. 5. (a) Bode plot of the analogue part of the electronic circuit shown in Fig. 3. The signal at the output of the second amplifier of the shaper is filtered at low frequencies by the low-pass characteristic of the CSA amplifier and at high frequencies by the CR circuits of the amplifiers. (b) Transient simulation of the analogue and digital outputs of the frontend circuit shown in Fig. 3.
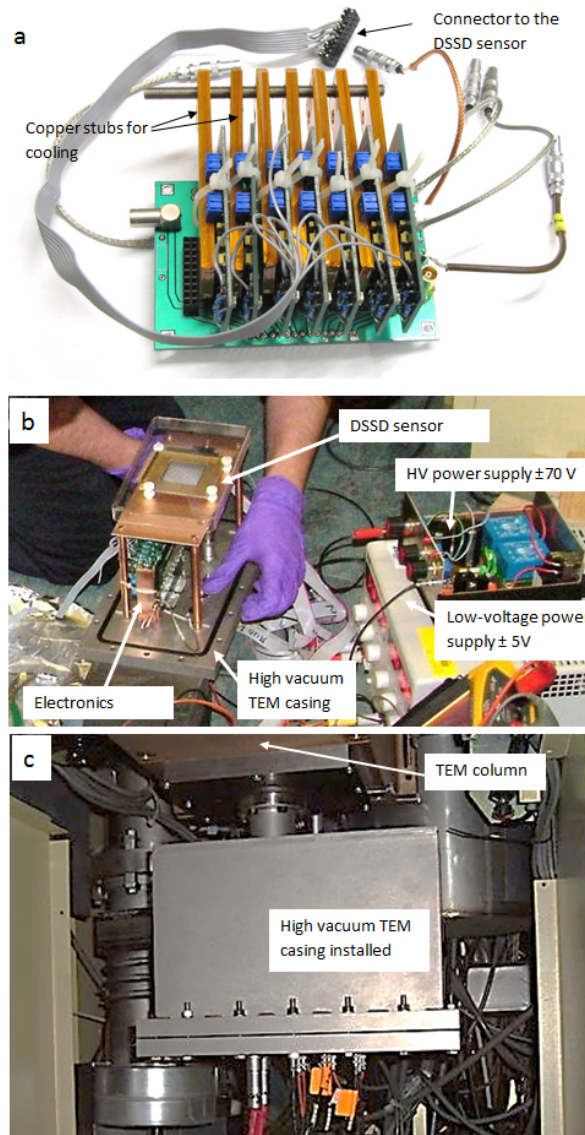
Fig. 6. (a) Block with seven identical frontend circuits, as shown in Fig. 3b, ready for test. Image shows the cables and copper stubs added for dissipating heat from the integrated circuits inside the vacuum of the TEM column. (b) Electronic equipment for test including the voltage power supplies. (c) The electronics and the DSSD sensor installed inside a vacuum chamber, and mounted to the base of the TEM column.
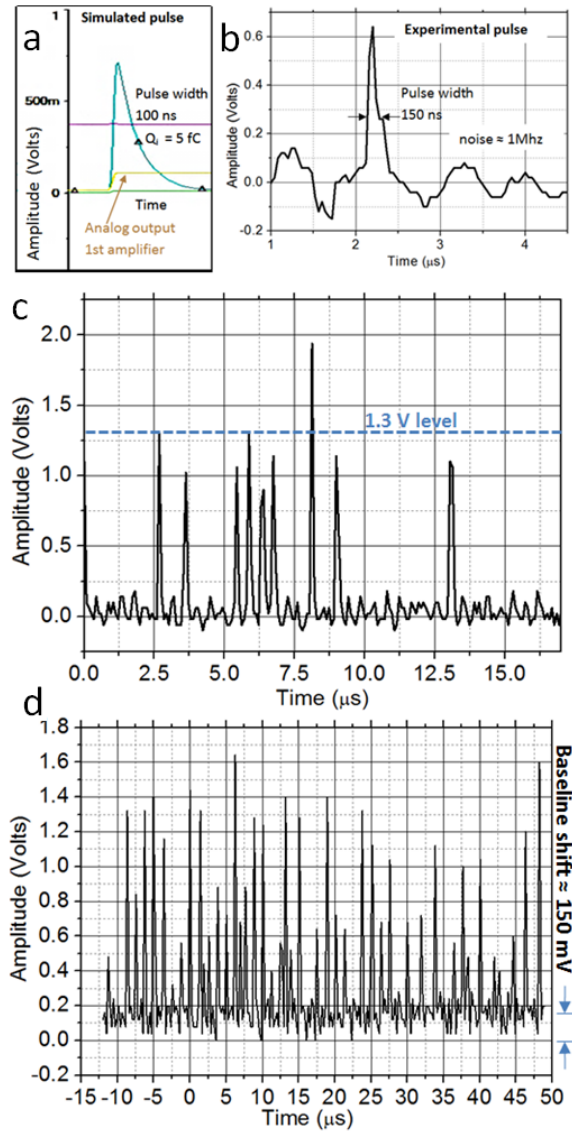
Fig. 7. (a) Detail of the simulated analogue output of the first amplifier and the analogue output after the second amplifier for a pulse of charge of 5 fC. (b) Experimental pulse measured with the DSSD detector inside a TEM for one electron accelerated at 200 keV. The pulse has a width of 150 ns and amplitude that fits well the simulated pulse. RF noise is also present as 1 MHz oscillations with $V_{RMS} = 50$ mV. The 1.3 V reference level corresponds to the theoretical amplitude expected for an electron event of 200 keV fully absorbed inside the DSSD. (c) Experimental measurement of the analogue output of the front-end circuit shown in Fig. 3. (d) Changing the dose an upwards shift of the baseline of 150 mV is observed.

MINI ABSTRACT

Here we investigate feasibility of employing a Silicon Strip Detector (SSD) as a direct imaging detector for TEM. We detail design and tests of the frontend electronics and discuss the limitations and applications of this technology for TEM.