# Simplified single-phase clock scheme for MOBILE networks

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MOBILE networks can be operated in a gate-level pipelined fashion allowing high throught-output. If MOBILE gates are directly chained, a four-phase clock scheme is requiered for this. A single phase scheme is possible adding latches to the MOBILE gates. This paper proposes and experimentally validates a new single-phase interconnection scheme that simplifies the inter-stage element, which translates in power, area and clock load advantages with respect to using latches.

*Introduction*: It has long been recognized that area, power and speed advantages can be obtained incorporating Negative Differential Resistance (NDR) devices in circuit design. Resonant Tunnelling Diodes (RTD) exhibit such an NDR characteristic and many circuits taking advantage of it have been reported covering different applications (memories, logic, oscillators, A/D converters, ...) and with different goals (high speed, low power, ...). In particular, their NDR current-voltage (*I*-*V*) characteristic can be exploited in logic design to significantly increase the functionality implemented by a single gate (in comparison to CMOS and bipolar technologies) [1].

Logic circuit applications of RTDs are mainly based on the MOnostable-BIstable Logic Element (MOBILE) [2] which exploits the negative differential resistance of their *I*-*V* characteristic (Fig. 1a). The MOBILE in Fig. 1b is an edge-triggered current controlled gate which consists of two RTDs connected in series and driven by a switching bias voltage, $V_{CK}$. When $V_{CK}$ is low, both RTDs are in the on-state and the circuit is monostable. Increasing to an appropriate maximum value ensures that only the device with the lowest peak current switches (*quenches*) from the on-state to the

off-state. Output is high if the driver RTD switches and it is low if the load does. Logic functionality can be achieved if the peak current of one of the RTDs is controlled by an input. In the configuration of the rising edge-triggered inverter MOBILE shown in Fig. 1c, the peak current of the driver RTD can be modulated using the external input signal. RTD peak currents are selected such that the value of the output depends on whether the external input signal is “1” or “0”.

*Interconnection of MOBILE logic gates*: Rising (falling) edge-triggered MOBILE logic gates evaluate the inputs with the rising (falling) edge of the bias voltage and hold the logic level of the output while the bias voltage is high (low), even though the inputs change (self-latching operation). The output returns to zero (to one) with the falling (rising) edge of the clock until the next evaluation. The self-latching operation allows the implementation of gate-level pipelined architectures without extra memory elements [1,3]. The return of the output to a reset value implies that each stage must evaluate when the previous stages are in the hold phase. A multi-phase clock scheme is necessary to operate MOBILE networks. Each clock cycle is divided into four phases of the same length, $T_R$, (evaluation, hold, reset and wait) and each consecutive clock signals are also delayed by $T_R$. Therefore, each stage evaluates during the hold phase of the previous stages and before they return to the reset value. Four clock signals are enough, since $V_{CK,1}$ can be used for the fifth level and so on. Thus, the clock signal distribution is critical for a correct operation of the MOBILE network, with constraints between rising and falling times and the delays between two consecutives signals.

In order to increase the robustness, it is desirable to replace the four-phase clock scheme by a simpler one. A network of MOBILE gates can be operated with a single clock phase [4] by alternating “non-return-to-reset” rising and falling edge-triggered stages. A “non-return-to-reset” rising (falling) edge-triggered stage is formed adding a

latch enabled with high (low) level. This interconnection scheme resembles TSPC, the well-known CMOS gate level pipelined design style.

*Proposed interconnection scheme*: A detailed analysis of the operation of this architecture shows that the 'non-return-to-reset' is not necessary to ensure a correct operation. Moreover, it is enough to maintain the output of each MOBILE stage until the next one has evaluated. Thus, the latches reported in [4], which exhibit a large static consumption that limits their practical usage, can be substituted by a simpler circuit. Moreover, simulations of alternating rising and falling edge-triggered MOBILE gates without inter-stage elements show correct operation. This is explained because the decision on which output the MOBILE will give is taken when $V_{CK}$ is approximately equal to $2V_P$. For this value of the clock voltage, the output of the previous MOBILE stage has not reached the reset value yet and, thus, it can be properly evaluated. In spite of this, since the MOBILE operating principle is very sensitive to load, an inter-stage element is advantageous to increase robustness and to ease design. This element takes care of fan-out and isolates MOBILE gates. Fig. 2a depicts the proposed architecture.

Fig. 2b shows HSPICE simulated waveforms corresponding to an interconnection of rising and falling edge-triggered MOBILE inverters with static inverters as inter-stage elements. Evaluation problems could occur for those cases in which the output of the previous MOBILE stage differs from its corresponding reset value. In these situations, the active edge of the clock signal forces a change in the output of previous stage which is, at the same time, being evaluated. In the shown waveforms, this happens for the falling edge-triggered MOBILE (the one with $V_{OUT,2}$ as input and $V_{OUT,3}$ as output) in the marked clock transition. Note that the right input value (zero) is taken in spite of $V_{OUT,1}$ being reset to zero (and so $V_{OUT,2}$ reset to one) by that transition. Note that in addition to the already mentioned advantages of including an

inter-stage element, the small delay introduced by the inverter favors correct operation.

*Experimental results*: The operation of the proposed interconnection scheme of MOBILE gates has been experimentally validated. Up to our knowledge it is the first time a working single phase MOBILE network is reported. A three-stage chain of MOBILE inverters have been fabricated. The first and the third follower are falling edge-triggered, whereas the second one is rising edge-triggered. They have been implemented with MOS-NDR devices (circuit made up of transistors that emulate the RTD *I-V* characteristic) and the MOBILE gate topology from [5] in a 1.2V 130nm CMOS commercial technology.

Fig. 3 depicts experimental waveforms in which the clock (a sinusoidal clock of 100MHz) and the input have been captured using an oscilloscope. They have been represented along with the digital version of the output in the logic analyzer Agilent 16902B. Note that the same sequence of the input is observed on the output as expected (there are six inverting stages in total since we are using inverters after each MOBILE inverter), with a delay between them, corresponding to three semi periods of the clock signal. This delay is associated to the consecutive evaluation of the three MOBILE stages. Moreover, the return to the reset value is observed. In order to validate circuit operation for faster clock transitions, and since increasing the frequency of the sinusoidal clock was not possible due to dynamic limitations of the pads, we have used a pulse generator. We have checked that the circuit also operates correctly for these much faster (smaller rising and falling times) clock transitions. In this experiment, the clock has been generated by a HP81134A pulse generator, with an operation frequency of 20MHz and rising and falling times, measured using low capacitance probe in our experimental set up, of 800ps.

*Conclusions:* A new single-phase interconnection scheme between MOBILE stages has been proposed and experimentally validated. It simplifies the inter-stage element reported in previous single-phase architectures which translates in power, area and clock load advantages. The operation of the structure has been shown using static inverter as inter-stage element. Experimental results exhibit a correct operation for different clock transition times.

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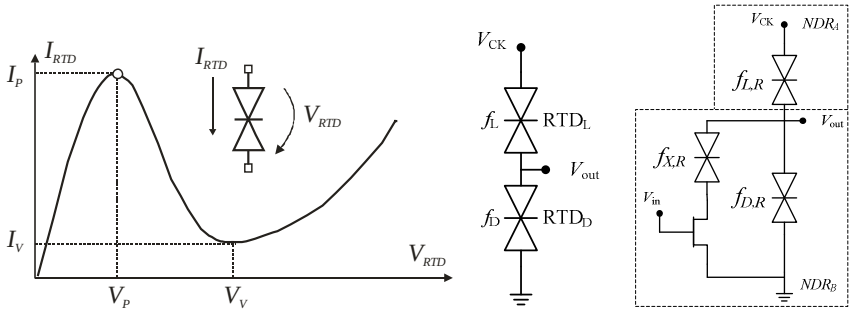
**Figure captions**

Fig. 1 (a) RTD current-voltage characteristic and symbol. (b) MOBILE. (c) Rising edge-triggered MOBILE inverter.

Fig. 2 (a) Block diagram of the proposed single-phase connection. (b) Waveforms used to explain the operation of the circuit of Fig. 2a.

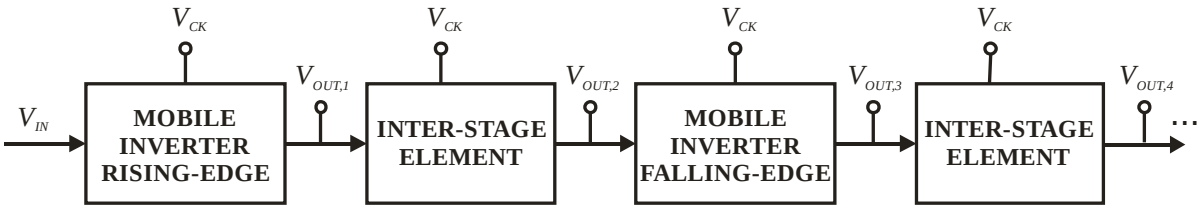
Fig. 3 Experimental results of the fabricated MOS-NDR MOBILE chain.

**Figure 1**

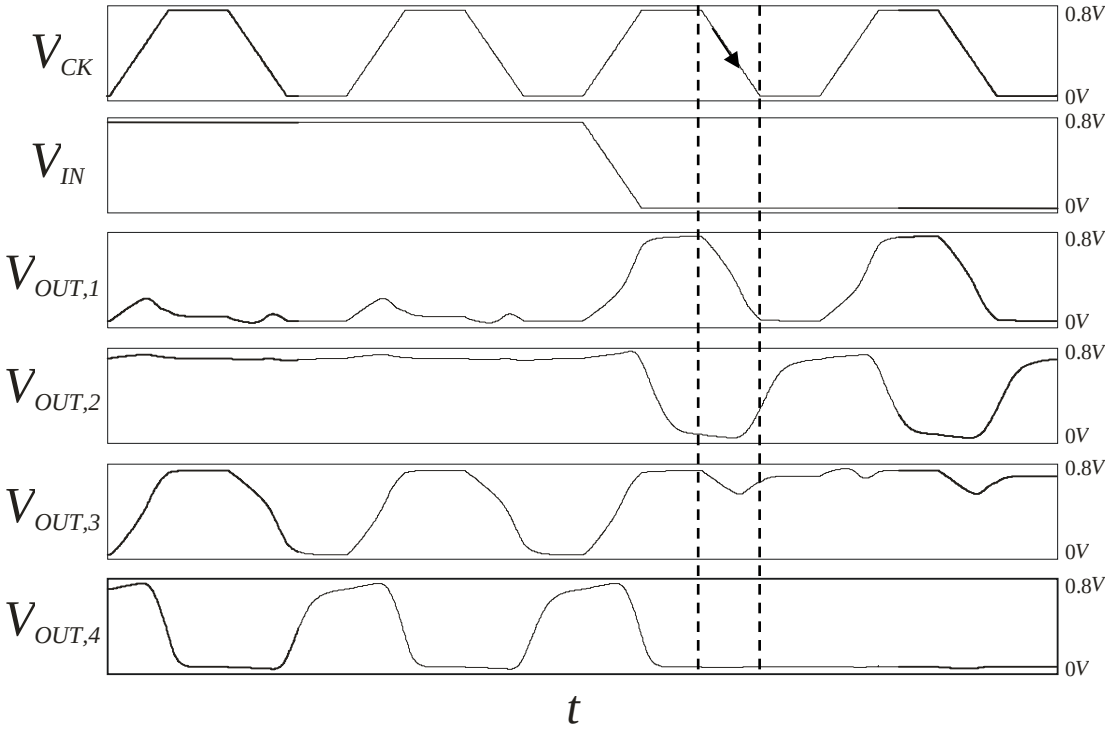

$I_{RTD}$
$I_P$
$I_V$
$V_P$
$V_V$
$V_{RTD}$
$I_{RTD}$
$V_{RTD}$
$V_{CK}$
$f_L$
RTD$_L$
$V_{out}$
$f_D$
RTD$_D$
$V_{CK}$
$NDR_A$
$f_{L,R}$
$V_{out}$
$f_{X,R}$
$V_{in}$
$f_{D,R}$
$NDR_B$

(a) (b) (c)

**Figure 2**

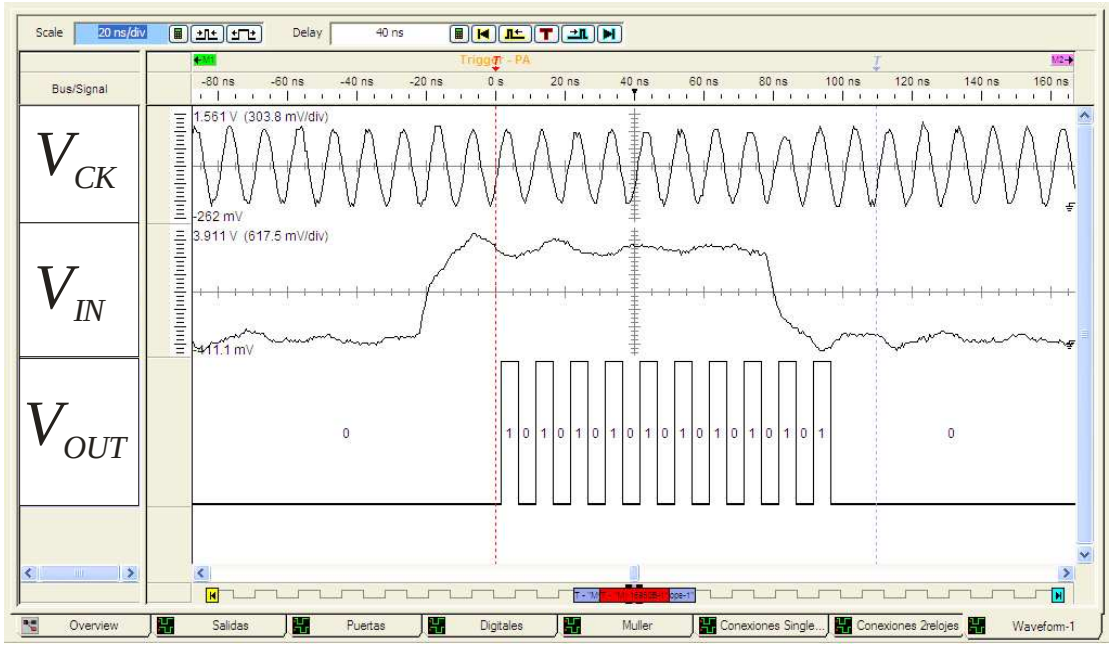

$V_{CK}$
$V_{CK}$
$V_{CK}$
$V_{CK}$
$V_{IN}$
$V_{OUT,1}$
$V_{OUT,2}$
$V_{OUT,3}$
$V_{OUT,4}$
MOBILE INVERTER RISING-EDGE
INTER-STAGE ELEMENT
MOBILE INVERTER FALLING-EDGE
INTER-STAGE ELEMENT
…

(a)


$V_{CK}$
$V_{IN}$
$V_{OUT,1}$
$V_{OUT,2}$
$V_{OUT,3}$
$V_{OUT,4}$
0.8V
0V
$t$

(b)

**Figure 3**


Scale
20 ns/div
Delay
40 ns
Bus/Signal
$V_{CK}$
$V_{IN}$
$V_{OUT}$
-80 ns
-60 ns
-40 ns
-20 ns
0 s
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns
160 ns
1.561 V (303.8 mV/div)
-262 mV
3.911 V (617.5 mV/div)
-411.1 mV
0
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
0
Overview
Salidas
Puertas
Digitales
Muller
Conexiones Single...
Conexiones 2relojes
Waveform-1