JETTA manuscript No.
(will be inserted by the editor)

Alternate test of LNAs through ensemble learning of on-chip digital envelope signatures

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Received: date / Accepted: date

Abstract This paper presents a novel and low-cost methodology for testing embedded Low Noise Amplifiers (LNAs). It is based on the detection and analysis of the response envelope of the Device Under Test (DUT) to a two-tone input signal. The envelope signal is processed to obtain a digital signature sensitive to key specifications of the DUT. An optimized regression model based on ensemble learning is used to relate the digital signatures to the target specifications. The proposed test procedure is studied from an analytical point of view, and a demonstrator has been developed to prove the feasibility of the approach. This demonstrator features a 2.445GHz low-power LNA and a simple envelope detector, and has been

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developed in a 90 nm CMOS technology. Post-layout simulations are provided to verify the functionality of the proposed test technique.

Keywords RF test · RF BIST · Signature test · Ensemble learning

1 Introduction

Nowadays complete and very complex systems are integrated on one single die. By far the largest portion of that is in the digital part of the system, which usually contains Multi-core GHz Processors, multiple Mbytes of memory, Media Access Controllers (MAC) and several dedicated Digital Signal Processors (DSP). Examples can be found in consumer applications like cellular phones, DVD players, multi-media players and so on. A general conceptual scheme for the architectures of these present and future systems can be that in Figure 1, where any wireless-based application is conceptually covered. As shown in the typical example of Figure 1, these systems usually contain one or multiple Analog Front-Ends (AFE), Analog Back-Ends (ABE), as well as RF Receive and Transmit functions.

From a test engineer point of view, testing RF subsystems embedded in a complex, tightly-integrated SoC represents a challenging task. The difficulty stems from the fact that each RF block has a specific set of diverse specifications that usually require a custom test strategy. It can be said that RF testing has inherited all the difficulties of analog testing, but adding also the problem of handling high frequency signals. This framework leads to the same fundamental problem for analog and RF testing: these blocks are tested based on the functional measurement of a set of specifications, while fault-model-based test, very successful in the digital test domain, are impossible to standardize in the RF field, since each circuit type demands its own custom fault model.

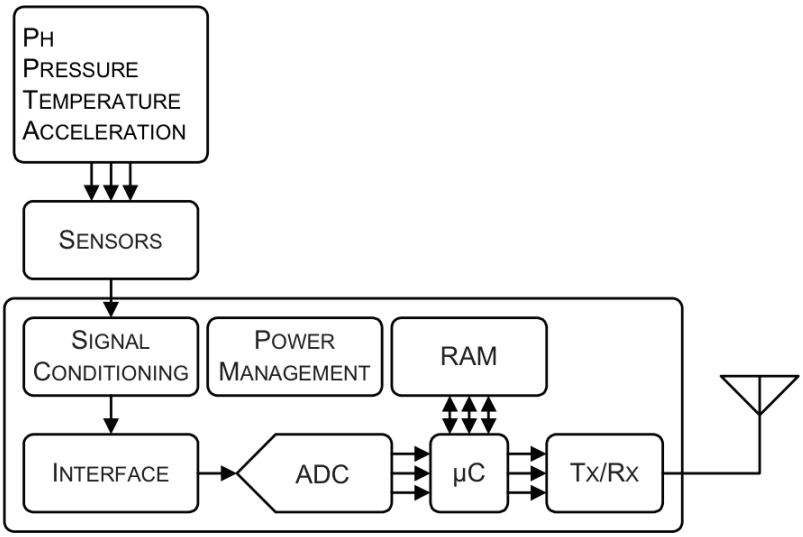

Fig. 1 Generic SoC view

The diverse specifications and high operating frequency of RF blocks, as well as the large impact of process variations in current deep sub-micron technologies, make necessary extensive tests that are complex and expensive to perform. Reducing RF test complexity and cost is still an open research topic that has been addressed in a number of different approaches. Recent work in this area includes defect modeling and failure diagnosis [1–4], alternate test [4, 5], DfT and BIST techniques [6–14], etc.

In particular, BIST techniques have been identified as a solution to mitigate RF test drawbacks for several reasons [10]:

- The test cost of RF systems is dominated by expensive automatic test equipment (ATE). Thence it should be desirable to move some of the testing functions to the test board or to the device under test (DUT) itself.
- There is a strong demand of known-good-die test solutions that can be implemented at wafer level, due mainly to the increasing packaging costs.

– BIST can be used to identify faulty blocks inside the system, providing a valuable information for yield enhancement and accelerating product development.

Direct approaches for testing and diagnosing an RF device are based on the application of a high-frequency stimulus to the DUT, and the observation of its response. This requires the use of high-speed external test equipment and, for embedded RF devices, the provision of an adequate test access. However, the increase in operation frequency and integration capabilities turns the latter two requirements quite difficult. Test access to internal nodes is usually impossible, and even in the case these nodes are reachable, there may be electrical losses in the transport of the signals from the chip to the external tester due to their inherent high-frequency.

Some authors [5, 15] replicate traditional RF test equipment such as spectrum analyzers on a load board. These approaches employ complex circuitry (mixers, frequency synthesizer, etc.) for up- and down-conversion of the test stimulus and its response, respectively. The need of RF testers is eliminated and multiple RF test specifications can be extracted. However, the load board circuitry is too complex for its direct BIST implementation, and hence this approach is limited to the test of discrete RF circuits.

The approach in [1, 2] focuses on failure diagnosis of RF circuits. The work in [1] considers the detection of catastrophic faults, while that in [2] also attempts to isolate parametric ones. Although behavioral simulations demonstrate high fault coverage, they lack a general fault model. Furthermore, it is necessary the use of standard RF test equipment and techniques to enable failure diagnosis.

Loop-back test and diagnosis of transceivers have also been widely explored [3, 4, 9–11]. The main advantage is that only-digital signals are involved as well as that both the receiver and the transmitter are tested at once. However, an on-chip implementation is not

so simple since, in practice, some components need to be removed for testing, namely the band-pass filter, close to the antenna, and the power amplifier in the transmission path [9], or an attenuator block has to be implemented within the loopback connection to accommodate the output of the transmitter to the input of the receiver [10].

The use of test sensors embedded into the RF system has also been proposed [6–8, 10–14]. Several built-in test schemes have been reported that use integrated peak, root-mean-square (RMS), power detectors and temperature sensors for testing discrete RF modules or complete transceivers. However, these sensors usually deliver a DC signal. To extract the test specifications from the limited information of a DC magnitude, multiple detectors and/or test configurations have to be used, thus increasing the complexity of the test as well as the required area overhead. Likewise, the design of these detectors is not always straightforward.

In this context, the approaches in [16–19] propose the use of a simple envelope detector for RF test purposes. The work in [16] demonstrates that selected specifications can be extracted from the envelope of the response of an RF block to an optimized test stimulus. The envelope signal is acquired with a conventional A/D converter and processed to carry out the demanded measurement. The work in [18] combines envelope extraction and other sensors, such us Die-Level Process Monitors (DLPM [20]), DC probes, and current sensors, and analyzes how the combined outputs of these sensors correlate to the specifications of the RF DUT.

On the other hand, the work reported by the authors in [19] takes advantage of analytical results to define a digital signature from the response envelope of the DUT to a two-tone at-speed test stimulus. It is shown that this digital signature can be easily discriminated when the circuit is performing within specifications. The latter method has some benefits in terms of simplicity. Thus, compared to [16], there is no need of complex stimulus optimization,

processing the envelope is greatly simplified, and the use of a complete A/D converter for signal acquisition is avoided. Also, compared to [18] a single envelope detector is used instead of multiple sensors, test access to internal nodes of the DUT is not required, and there is no transport of analog DC signals to the outside world, being the test output a simple digital word. However, compared to [16] and [18], reference [19] has the important disadvantage of not providing functional measurements.

The proposal to be described herein aims to extend our previous idea of a signature-based test by a two-tone response envelope characterization. This work will demonstrate how the information contained in the digital signatures can be easily related to the functional specifications of the DUT, while keeping the simplicity of the approach reported in [19]. The paper is organized as follows. Section 2 recalls the analytical basis of [17, 19] and presents the proposed test technique. Then, section 3 discusses its on-chip implementation and presents the design of an integrated demonstrator. After that, Section 4 provides some relevant experimental results to validate the proposal. Finally, Section 5 summarizes the main contributions of this work.

2 Proposed approach

2.1 Theoretical basis

Figure 2-a shows a standard two-tone test set-up that is traditionally used to characterize RF systems. In this test scheme, two high-frequency close tones are used as test stimuli and fed to the DUT. The system response is then acquired and conveniently processed to characterize the DUT. Important performance parameters such as forward gain, third-order intercept, inter-modulation products, 1dB compression point, etc, can be measured using this traditional set-up. However, the direct acquisition and processing of the test response

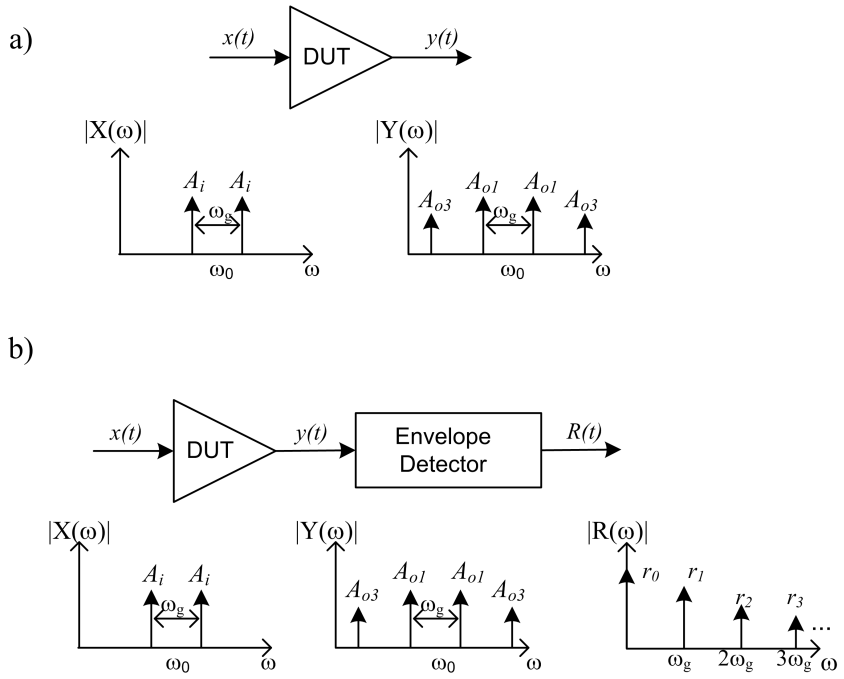

Fig. 2 a) Traditional two-tone test; b) Two-tone response envelope detection.

is a challenging task, since this response is a high-frequency signal that has to be handled by expensive RF test equipment. Our approach, represented in Figure 2-b, is in fact similar to the traditional scheme, but in this case the DUT response is driving an envelope detector. The extracted envelope has relevant information about the test response at much lower frequencies, this information being easily extracted by simplified processing.

Let us consider the typical two-tone test (see 2-a), in which a non-linear RF device is driven by a signal $x(t)$ composed of two equal-magnitude tones at different, but very close, frequencies, in the form,

$$x(t) = A_i cos\left(\left(\omega_0 - \frac{\omega_g}{2}\right)t\right) + A_i cos\left(\left(\omega_0 + \frac{\omega_g}{2}\right)t\right) \quad (1)$$

where A_i is the amplitude of each test tone, and ω_g is the frequency difference between them ($\omega_g << \omega_0$). In order to make an analytical study, a third-order non-linear model has been assumed for the RF block. That is, the response $y(t)$ of the system can be written as,

$$y(t) = \alpha_1 x(t) + \alpha_3 x^3(t) \tag{2}$$

Expanding (2), and discarding the out-of-band components, the response $y(t)$ can be expressed as,

$$\begin{aligned} y(t) =& A_{o1} cos\left(\left(\omega_0 - \frac{\omega_g}{2}\right)t\right) + A_{o1} cos\left(\left(\omega_0 + \frac{\omega_g}{2}\right)t\right) \\ &+ A_{o3} cos\left(\left(\omega_0 - \frac{3\omega_g}{2}\right)t\right) + A_{o3} cos\left(\left(\omega_0 + \frac{3\omega_g}{2}\right)t\right) \end{aligned} \tag{3}$$

Using the Rice formulation [21], the envelope, $R(t)$, of a real waveform, $u(t)$, can be expressed as,

$$R(t) = \left\| u(t) + i\, u^H(t) \right\| \tag{4}$$

where, i is the imaginary unit, and $u^H(t)$ is the Hilbert transform of $u(t)$. In our case, the envelope of the response signal $y(t)$, can be thus computed as,

$$R(t) = \left| 2A_{o1} cos\left(\frac{\omega_g}{2}t\right) + 2A_{o3} cos\left(\frac{3\omega_g}{2}t\right) \right| \tag{5}$$

Signal $R(t)$ results to be a periodic function with period $T_g = 2\pi/\omega_g$. Given that $\omega_g << \omega_0$, then signal $R(t)$ results to be a low frequency signal that still contain information about the magnitude of the spectral components, A_{o1} and A_{o3}, of the high-frequency DUT response. We take advantage of this information to define a simple signature that can be used for testing purposes.

2.2 Signature definition and efficient implementation of the signature extractor

In order to extract a meaningful test signature from the response envelope $R(t)$, some considerations have to be made. The target signature has to keep the information about the DUT

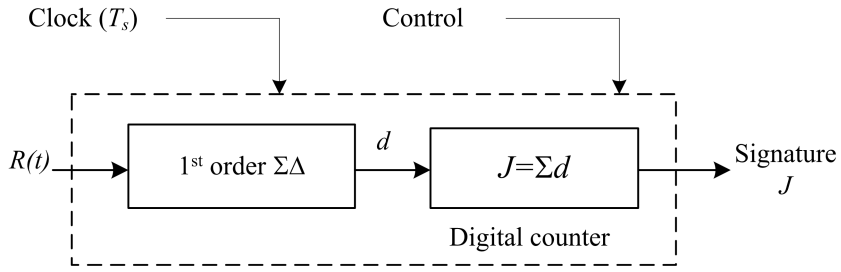

Fig. 3 Block diagram of the proposed signature extractor.

response contained in the envelope, that is, magnitudes A_{o1} and A_{o3}, but also the computation of the signature itself has to be as simple as possible to reduce the overhead due to the signature extractor. In this line, we propose the computation of the area under the $R(t)$ curve as a simple test signature, that, as it will be shown, can be efficiently computed on-chip while keeping the desired information.

The area, $\hat{J}$, under M periods of the response envelope $R(t)$ can be easily computed as the integral,

$$\hat{J} = \int_0^{MT_g} R(t)dt = M\frac{8}{\omega_g}\left(A_{o1} - \frac{A_{o3}}{3}\right) \tag{6}$$

Signature $\hat{J}$ results to be a linear combination of the high-frequency response spectral components A_{o1}, and A_{o3}. Consequently, it should be clear that signature $\hat{J}$ is sensitive to changes in gain and non-linearity specifications, so any deviation affecting those characteristics would affect also its value.

A direct approach for computing signature $\hat{J}$ in the digital domain would require a precise A/D converter to acquire the response envelope, and an arithmetic DSP. Instead of that, since the response envelope is a low-frequency periodic signal, the computation of signature $\hat{J}$ can be made using an alternative method; in our proposal, by using a simplification of the efficient test core for periodic analog signal analysis in [22]. Figure 3 shows the block diagram of our proposed signature extractor. It takes advantage of the noise-shaping char-

acteristics of first-order $\Sigma\Delta$-modulators to accurately compute the target signature in the digital domain. Signal $R(t)$ is directly fed to a first-order $\Sigma\Delta$-modulator, which provides a simple and robust A/D conversion without the need of a full A/D interface. The output bitstream of the $\Sigma\Delta$ modulator, $d(n)$, can be expressed as a function of the input signal samples, $R(n)$, and the quantization error in the modulator, $e(n)$, as,

$$d(n) = R(n-1) + e(n) - e(n-1) \tag{7}$$

This output bit-stream, $d(n)$, is then integrated using a simple digital counter to get a digital signature J. This signature is given by,

$$J = \sum_{n=1}^{MN} d(n) = \sum_{n=0}^{MN-1} R(n) + \sum_{n=1}^{MN} \{e(n) - e(n-1)\} = \frac{8MN}{\pi}\left(A_{o1} - \frac{A_{o3}}{3}\right) \pm 2 \tag{8}$$

where N is the oversampling ratio in the modulator defined as $N = T_g/T_s$ (T_s is the sampling period in the modulator), the integration has been extended to M response envelope periods, and magnitudes A_{o1} and A_{o3} are in this case normalized with respect to the full-scale range of the $\Sigma\Delta$ modulator. It is important to notice that the error term ± 2, due to the quantization error in the modulator, does not scale with the number of evaluated samples because this error is naturally compensated in the discrete integration.

Signature J is a digital measurement of the area under the envelope signal, $\hat{J}$, and the resources needed to calculate it are reduced to a first-order $\Sigma\Delta$ modulator and a simple digital counter.

In a first approximation, the analytical expression (8) could be used to directly compute magnitudes A_{o1} and A_{o3}, and hence, provide a functional characterization of the DUT. However, let us recall that this analysis has been performed under the assumption of a third-order polynomial model for the RF block. Actual DUT behavior may deviate from this idealization, and consequently the analysis becomes more complex, or impossible to complete. In

spite of that, the previous analysis is important because we have demonstrated that there is a relation between the proposed signature and performance figures. In this work we extract functional information about the DUT from the proposed signature by building a blind regression model, without assuming any analytical model for the DUT.

2.3 Ensemble Learning

Machine-learning, regression modeling, function approximation, data mining, all this terminology belongs to the vast mathematical field of statistics. Researchers have been struggling to develop the best modeling approach from more than a hundred years. Unfortunately, the idea of best model is always relative to the application and nobody has come out with the definitive approach. Some models perform better on low-dimension spaces, other require few training samples, etc.

As a matter of fact most papers that apply machine-learning algorithms to circuit testing do not explain the choice of their statistical tool. For potential users, it is difficult to assess if a given tool will perform well in another case. Actually, the task of model selection has already been investigated (see Chapter 7 in [23]), and a number of criteria have been developed to assess model quality, usually in terms of expected prediction error. Anyhow, managing these concepts is not an easy task to the profane.

From the end-user perspective, the concept of ensemble learning is very appealing because it builds a mosaic model from a collection of statistical tools. It implements a routine that trains different models using cross-validation principles to deduce the expected prediction error. The final model is a weighted average of a subset of all the trained models, being the weights a function of the calculated prediction error. The task of model selection is thus handled by the top-level ensemble construction in an automatic way.

As pointed out in [24], diversity is the cornerstone of ensemble approaches. The idea is that no perfect model exist but different models will likely commit errors at different places. Uncorrelated model errors can thus be averaged out.

The practical implementation of ensemble learning is greatly simplified by the ENTOOL Matlab toolbox developed by Wichard and Merkwirth [25], which itself uses elements of [26]. All the statistical data in this paper have been managed by this toolbox without ad-hoc corrections. The obtained results thus serve to validate its use in the context of Alternate Test. Let us briefly present the different model families [1] that are trained by the toolbox to form the ensemble.

- Polynomials models that expand linear ones by introducing the products of input variables as new variables. Complexity is handled by limitting the order of the polynomial and the number of variables.
- Nearest-Neighbors models parametrized by different neighborhood sizes, different averaging kernels or different distance definitions.
- Neural Networks of three different classes: Perceptrons, Radial Basis Functions, and Projection-based Radial Basis Function Nets (PRBFN, [27]) which can be seen as a combination of ridge (perceptron) and RBF neurons.
- Multivariate Adaptive Regression Splines (MARS) proposed by Friedman [28] and successfully applied in a large number of papers in the past few years [29–31]. For high-dimensional data, only low-order splines are considered (typically lower than three) in order to limit the complexity of the model. The Adaptive Multivariate part of the name comes from the recursive partitioning of the input space.

[1] Unfortunately, it is not possible to thoroughly describe the performance of each model in a single journal article. The interested reader can refer to [23] for a deeper insight.

Within these different model families, the toolbox can generate a wide variety of models by selecting different parameters, like kernel types, roughness penalties, learning methods, number of hidden layers... Diversity is thus ensured and the resulting ensemble is likely to outperform its constituting models.

3 Demonstrator design

3.1 Goal of the demonstrator.

In order to verify the feasibility of the previously discussed test procedure we use an LNA design that complies with the IEEE 802.15.4 standard. The implemented demonstrator is depicted in Fig. 4. The signature extractor in Fig. 3 is not included in the prototype; instead, it is emulated externally to provides flexibility in the validation.

3.2 Presentation of the CUT

LNA: The single-ended LNA with inductive source degeneration is designed in a 90nm technology. Its specifications are: (i) a noise figure (NF) below 5dB, (ii) a third-order input intercept point (IIP3) higher than -6dBm and (iii) both source and load impedances equal to 50Ω and (iv) a power consumption less than 2mW for a supply voltage of 1.2V.

Transistor M_1 of Fig. 4 is designed to be under moderate inversion in order to reduce power consumption, capacitor C_{ext} is used to adjust input impedance without spoiling the NF and L_d is chosen to obtain the highest gain available. The final design consumes 1.44mW

Envelope Detector: We have developed a simple current-mode envelope detector adapted from [32]. It comprises a voltage-to-current converter (VIC) followed by an AC-coupled half-wave current-mode rectifier with a passive output low-pass filter. The selected VIC is a

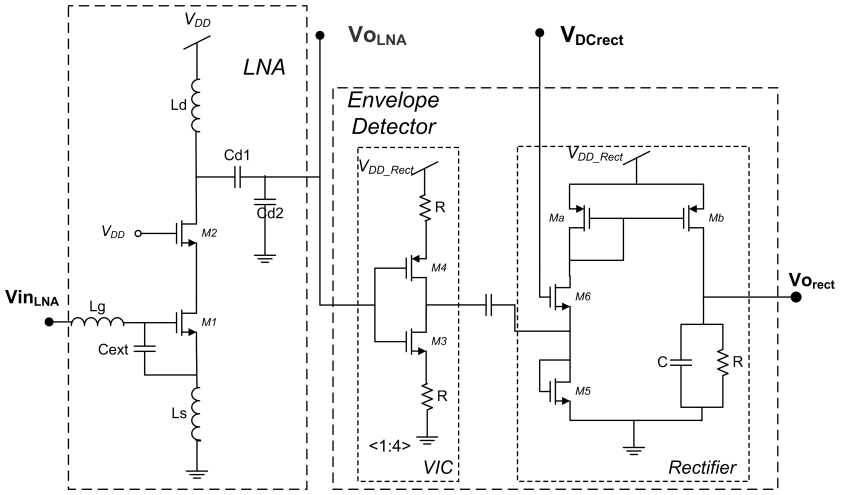

Fig. 4 Schematic of the designed LNA jointly with the envelope detector.

simple CMOS push-pull inverter with resistive source degeneration. Qualitatively, the half-wave rectifier works as follows: when the VIC output current flows into the rectifier, the diode-connected transistor M_5 is turned on and M_6 is off, so no current is drawn by M_b and V_{ORect} is zero. Oppositely, when the VIC output current leaves the rectifier, M_5 turns off while M_6 and M_a turn on, and this current is mirrored through M_b to the *RC* low pass filter. Voltage V_{DCrect} is used to bias transistor M_6 in the subthreshold region. The *RC* constant has been adjusted to reject the high frequency carrier, so the output voltage V_{ORect} follows the envelope of the input signal.

To obtain the LNA specifications when the envelope detector circuit is enclosed, a co-design is compulsory. In this particular design, a readjustment in the capacitances of the output network was needed. All designed transistors are sized with minimum length to obtain the best performance in high frequency. LNA bias circuit is not shown in Fig.4 for clarity.

The described envelope detector fulfills the following five conditions. Firstly, its input impedance is high enough to discard modifications in the output matching entailing losses

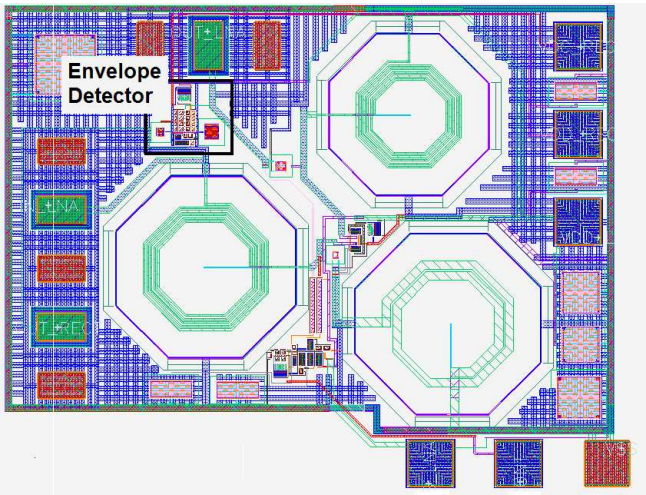

Fig. 5 Layout of the LNA with the envelope detector.

in the output power. Secondly, its power consumption is kept low to minimize temperature gradient that would adversely affect the characteristics of LNA transistors, and to allow the utilization of the BIT block under LNA normal operation without considerable current overhead (only about 300 μA_{RMS} when operating at 2.445 GHz). Also, the envelope detector has an independent power supply to be turned off when test is not performed. Finally, the area overhead is very small.

The complete layout of the prototype is depicted in Fig. 5. The total area without pads is 760 μm x 700 μm. The area of the envelope detector is 100 μm x130 μm. The area overhead is 2.4%. However this area overhead can also be considered as zero as the LNA, especially because of its three inductors, has enough free and unused area to permit the insertion of the detector.

Table 1 LNA characteristics with and without envelope detector

Specification	LNA without envelope detector	LNA with codesigned envelope detector
Gain (dB)	12.5	12.4
NF (dB)	3.66	3.66
IIP3 (dBm)	-4.4	-3.5
CP1dB (dBm) [2]	-15	-15.1
S11 (dB)	-24.8	-25.2
S22 (dB)	-9.8	-11.3
S12 (dB)	-26.4	-26.5
Zin (Ω)	46.6-13.2j	42.6-11.4j
Zout (Ω)	44.3+12.2j	42.4+8.7j

3.3 Simulated results and analysis.

Table 1 lists the typical performance figures of post-layout simulation of the designed LNA with and without the envelope detector. In both cases no substantial differences exist between the LNA characteristics.

Fig. 6 presents two large-signal transfer curves of the envelope detector obtained by post-layout simulation. These transfer curves plot the mean voltage at the output of the envelope detector when it is excited by a single tone both at 100MHz and 5GHz (the limits of its operating frequency range), as a function of the magnitude of this input tone. Voltages are normalized to the full-scale range, which corresponds, in this case, to the rail-to-rail range of the LNA. The input dynamic range is between [-45dBFS -15dBFS] at 100MHz and between [-30dBFS 0dBFS] at 5GHz.

Fig 7.a shows the output waveform of the envelope detector when it is excited with two 50 mV tones at 2.4445 GHz and 2.4455 GHz (7.b). In these plots both the input and output

[2] CP1dB: 1dB Compression point.

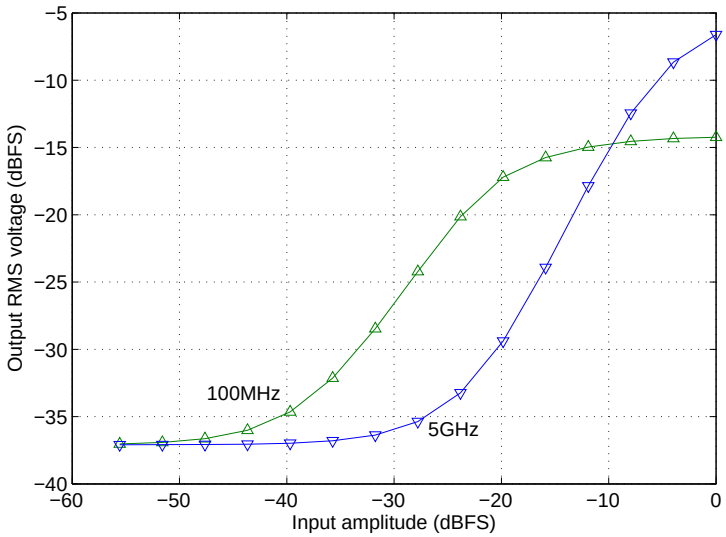

Fig. 6 Transfer function of the envelope detector injecting an input tone at 100MHz and at 5GHz.

waveforms have been normalized to their respective maximum values. As it can be clearly visualized, the output of the rectifier follows the envelope of its input signal. The envelope signal reaches a peak value of approximately 180 mV.

4 Experiment simulation

The demonstrator described in previous section has been fabricated and will be characterized soon. Unfortunately, like most academic institutions, we do not have access to industrial volumes. As a matter of fact only 100 samples were received and we do not know if they come from the same region of the wafer, the same wafer or the same lot. The closest to experimentation was thus to perform Monte-Carlo simulation on the extracted layout view.

The *J*-signature defined in Section 2 is used to predict the performance figures of the LNA using the ensemble learning paradigm previously described. For this purpose, a set of 200 instances of the demonstrator was obtained by a post-layout Monte-Carlo simulation.

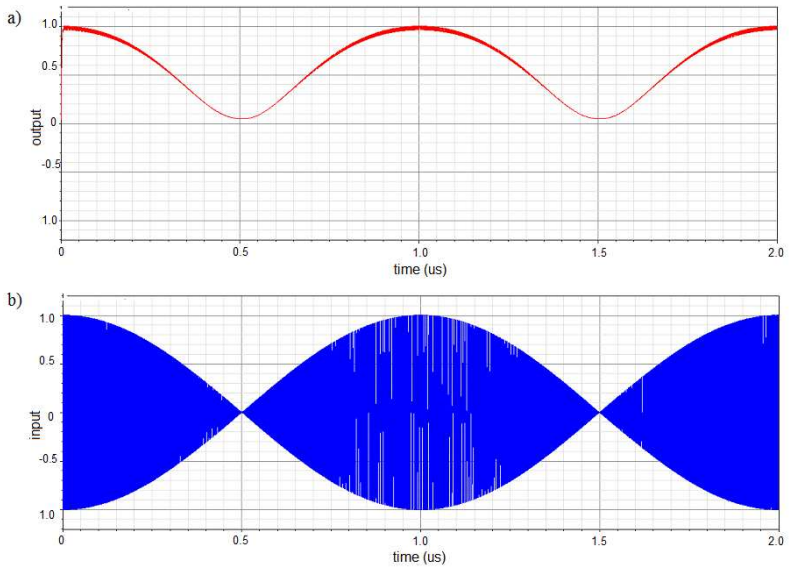

Fig. 7 a) Normalized output of the envelope detector and b) normalized input of the envelope detector.

Out of the 200 instances, 150 were used to train the ensemble, while 50 randomly chosen instances were taken apart as test set to verify the accuracy of the prediction. A set of different signatures J_{LNA} was extracted varying the magnitude of the input test tones. In addition, given that the envelope detector in the demonstrator is subject to the same variation mechanisms as the LNA, the test stimuli were bypassed to the envelope detector and signatures J_{env} were evaluated from the resulting envelope signal. Signatures J_{env} allow the ensemble model to estimate and remove the contribution of the envelope detector variations. Two different two-tone test stimuli were used in our validation, corresponding to magnitudes A_i = –26 dBm and A_i = –23 dBm. Both test stimuli were centered on f_0 = 2.445 GHz (the peak-gain frequency of the LNA) and the frequency gap between the two tones was set to f_g = 1 MHz.

Since the signature extractor was not included in this first proof-of-concept prototype, a realistic VerilogA model was used to compute the test signatures from the obtained envelope signals. The oversampling ratio and the number of evaluation periods were set to $N = 144$,

and $M = 1$, respectively. This way, we obtain a set of four independent signatures to feed the ensemble model, i.e. a pair (J_{LNA}, J_{env}) is computed for each test stimulus.

4.1 Performance estimation

An ensemble model is trained for each of the following performance specifications:

- gain
- 3^{rd} order Input-referred Intercept Point (IIP3)
- Noise Figure (NF)
- S_{11}, S_{12} and S_{21} parameters

In a production test environment, it is generally accepted that the model training phase should be preceded by a defect filter [33]. The objective of such a filter is to eliminate the circuits that do not correspond to process variations, like for instance spot defects. For such circuits, the model may not be able to find correlations between signatures and performance and in any case, these correlations would not respond to the same statistics as the ”nominal” circuits. A defect filter can be built from density estimation models to isolate outliers. In this work, all the samples are obtained through Monte-Carlo simulations of the extracted layout, using the process statistics provided by the fab. We thus know a-priori that they correspond to a unique multivariate statistic and the defect filter is thus unnecessary.

Figure 8 gathers the obtained scatterplots of the estimated versus the measured values. Dot markers stand for the complete set of samples – both training and test sets – and circle markers highlight the independent samples of the test set. The standard deviation of the estimation errors for the test set can be found in Table 2.

Presenting the performance of a regression model is not always an easy task. The standard deviation of the estimation error is actually a good metric, but it cannot be interpreted

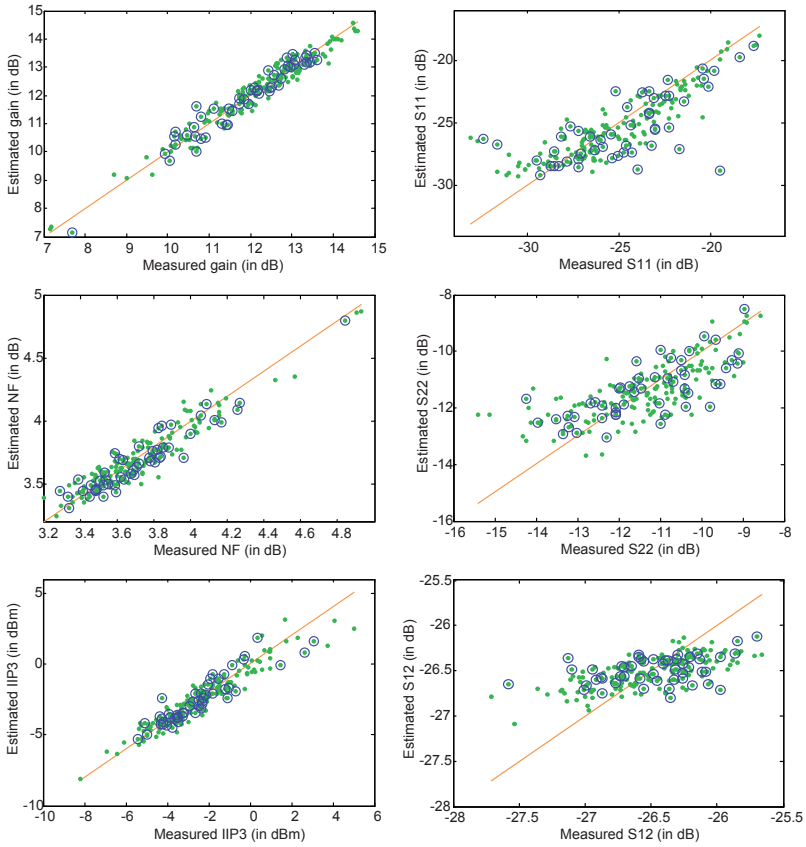

Fig. 8 Scatterplot of estimated versus measured performance specifications

Table 2 Model prediction error for the specifications

Specifications	σ_{error} on the test set	FOM
Gain	0.32 dB	3.90
NF	0.097 dB	2.98
IIP3	0.90 dBm	2.17
S11	2.09 dB	1.47
S22	0.96 dB	1.52
S12	0.31 dB	1.13

independently from the measurement. A voltage precision of, say, $3mV$ is either good or bad depending on the problem at hand. The standard deviation of the relative estimation error could be seen as a good alternative, but it is highly misleading. If the metric under consideration is close to zero in average (for instance an offset) the relative error will be high, even if the absolute precision is good. On the other extreme of the spectrum, if the metric under consideration is large in average (for instance, the DC gain of an amplifier) the relative error will appear to be small, even is the estimation is not very accurate.

For this reason, the table also boasts the following Figure Of Merit (FOM) for model-based test,

$$FOM = \sqrt{\frac{\frac{1}{N_s}\sum_{i=1}^{N_s}\left(P_{real,i} - \bar{P}_{real}\right)^2}{\frac{1}{N_s}\sum_{i=1}^{N_s}\left(P_{pred,i} - P_{MC,i}\right)^2}} \tag{9}$$

where N_s is the number of samples in the test set, $P_{pred,i}$ is the performance of circuit i predicted by the model, and $P_{real,i}$ is the real performance of circuit i. In our case, the real performance comes from the MonteCarlo simulation data, but the same definition holds for experimental data. The Hat symbol stands for the mean value, as usual.

We propose this FOM as a way to capture and evaluate the shape of the scatterplot (estimated vs measured). If the cloud of point is diffuse or clearly deviated from the diagonal, the model has brought almost no information and the FOM should be close to 1. On the other hand, if the cloud of points shrinks to the diagonal line the estimation is almost perfect and the FOM tends to the infinite.

It actually measures the improvement of the proposed model over the information inherently present in the data (in our case, the standard Monte-Carlo simulation). This inherent information is the variation range of the data. If the samples in the training set are greater than a and lower than b, you can expect that all the circuits will respect these bounds. If, for whatever reason, the variation range of the data is small, even a very good model will not

improve much the prediction. One reason may be that the training data is not sufficiently representative. For instance, if you have few silicon dies, they may come from the same region of the wafer and all give very similar results. This population is not representative of high volumes and the proposed FOM would remain close to 1, alerting that the problem is ill-conditioned. Another reason may be that the DUT was designed with large guardbands for a particular parameter. In such a case, the prediction may be accurate but the merit is not of the model.

One example of this effect is the case of S_{12} parameter in Figure 8. Roughly speaking, the measured S_{12} varies between $-27dB$ and $-26dB$: that is less than a 4% variation. Actually, the model is not able to retrieve any strong relationship between the digital signatures and the S_{12} parameter, so it outputs a value that is centered on the mean measured value. While the relative precision of this estimate is still close to 4%, the model actually brings no new information and it can be seen in Table 2 that the FOM for this parameter is only 1.13.

For the remaining parameters, it appears clearly that there is a strong correlation between the digital signatures and some parameters, namely the gain, the noise figure, and the input-referred third-order intercept point. The estimates of the S_{11} and the S_{22} parameters are also correlated to the real measurements but still not very precise. This may be due to two reasons: the four digital signatures may not be sufficient to adequately capture the underlying variation mechanisms, or the ± 2 quantization noise component on the signature (8) may dominate the model precision.

In order to test the latter assumption, we add an extra Gaussian white noise on the four digital signatures and re-train the models. As the magnitude of the Gaussian noise ($\sigma = 2$) has been made similar to the expected noise in the signature, if the model estimate is noise limited, the estimation error should significantly increase. As a matter of fact, assuming independent Gaussian errors, the estimation error should be multiplied by $\sqrt{2}$. The model

result for the LNA gain with the additional noise gives and estimation error of $\sigma_{err} = 0.49$ dB, which is clearly worse than the value quoted in Table 2 and very close to the $\sqrt{2}$ factor. It thus seems that the prediction of the LNA gain is mainly limited by noise. On the other hand, the estimation error for $IIP3$ is only increased by a factor 1.24 (from 0.9 dBm to 1.12 dBm) clearly lower than $\sqrt{2}$. Similar results are obtained for the rest of parameters. It can thus be concluded that generating the signatures for a larger number of evaluation periods (which according to (8) reduces the relative error in the signatures at the cost of increasing test time) would only improve the gain estimate.

4.2 Discussion on BIST approach

As said in the introduction, there have been several proposals of using embedded sensors to perform statistical regression. Obviously, the additional test circuitry is submitted to the same process variations as the DUT. In [18, 20], authors take advantage of this fact, implementing some replicas of the most sensitive parts of the DUT. These replicas are expected to vary in a similar way as the DUT, as far as global parametric variations are concerned. Measurements on these replicas thus offer some information on process impact on the circuit behavior, but without loading the real functional circuit in excess. This is an interesting approach but is quite different from what is proposed here. Like in [5], we propose to build a kind of on-chip instrument – in our case an envelope detector. This embedded instrument is submitted to process variations, and its performance will thus be correlated to the performance of the DUT. While for circuit replicas this performance correlation is close to 1 (neglecting the effects of local mismatch), for an independent instrument it is not known *a-priori*. As a matter of fact, fault masking may occur. One approach to circumvent this issue would be to design an on-chip instrument insensitive to Process Voltage and Temperature

Table 3 Model improvement with sensor signature

Specifications	σ_{error} for all signatures	σ_{error} for J_{LNA}	FOM for all signatures	FOM for J_{LNA}
Gain	0.32 dB	0.43 dB	3.90	2.78
NF	0.097	0.103	2.98	2.57
IIP3	0.9 dBm	1.70 dBm	2.17	1.20
S11	2.09 dB	2.87 dB	1.47	1.03
S22	0.96 dB	1.34 dB	1.52	1.01
S12	0.31 dB	0.37 dB	1.13	1.01

(PVT) variations. Unfortunately, this is usually not an easy task and would possibly lead to a test circuitry larger and more complex than the DUT. That is why we have proposed to bypass the DUT and generate a signature directly from the envelope detector. In this way, the information relative to the variation of the instrument and to the intrinsic variation of the DUT may be separated by the model. In a sense, we are performing a sort of implicit calibration of the instrument.

In order to illustrate this effect, we trained another model for the same samples using only the signatures from the LNA (J_{LNA}), Table 3 compares the FOM obtained for nominal model and the new one.

It appears that the FOM is much closer to 1 (i.e. much worse) if only the LNA signatures are considered. This is particularly true for *IIP*3 and the S parameters. The conclusion from this section is thus the direct translation of an old concern of defect-oriented BIST approaches to the realm of alternate test: you must ensure that the additional circuitry is not failing. In the case presented here, it can be said that the variation of the sensor must be measured independently in order to isolate the variation of the circuit.

An intuitive way to further improve the regression model would be to consider more inputs. Any additional measurement is likely to add a bit of information that was not present

in the original set. A brute force approach would be to consider as many measurements as possible. As most statistical training methods involve some form of overfitting limitation, feature selection is handled implicitly. The model would thus select the valuable measurements alone. However, this approach is not feasible if the additional measurements require chip modifications. For instance, the temperature sensors like those proposed in [14] are not only sensitive to the average temperature but also to the local one and thus to the local power dissipation. Such sensors would likely complement the information provided by the envelope detector, but we cannot affirm it *a-priori*. Though statistical tools are very powerful they do not solve the test problem, creativity is still needed to propose the best input space.

5 Conclusions

Alternate test is undoubtedly an interesting path to mitigate the ever increasing cost of testing embedded RF blocks. In this paper, a LNA with an envelope detector has been fully co-designed and implemented in a 90nm technology and it has been demonstrated that the parasitics introduced by the test circuitry do not significantly affect the performance. Using simple low-frequency circuitry, digital signatures can be generated from the output of the envelope detector (and thus easily routed through a hypothetical SoC). A regression model based on ensemble learning has been trained to relate these simple digital signatures to the main performance parameters of the LNA. The statistic tool has been shown to perform adequately and is particularly suited for non-expert users. In order to assess the relevance of statistical regression, we have also proposed a new Figure of Merit that measures the amount of additional information that the regression manages to extract from the original data. The results show that the proposed approach effectively measures some important performance parameters, like the LNA gain, the Noise Figure and the 3^{rd}-order Intercept

Point, and roughly estimates the S-parameters. Finally, we have shown that it is necessary to separate the variations due to the LNA itself from the variations of the embedded envelope detector.

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