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A Low-Voltage Floating-Gate MOS Biquad

ESTHER O. RODRÍGUEZ-VILLEGAS*, ALBERTO YÚFERA† and ADORACIÓN RUEDA‡

Instituto de Microelectrónica de Sevilla (IMSE), Centro Nacional de Microelectrónica (CNM), Edificio CICA, Avda. Reina Mercedes s/n, 41012-Sevilla, Spain

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A second-order g_m-C filter based on the Floating-Gate *MOS* (*FGMOS*) technique is presented. It uses a new fully differential transconductor and works at 2 *V* of voltage supply with a full differential input linear range and a *THD* below 1%. Programming and tuning are performed by means of a single voltage signal. The transconductor incorporates a novel Common-Mode Feedback Circuit (*CMFB*) based also on *FGMOS* transistors.

Keywords: Analog low-voltage low-power filters; FGMOS circuits

I. INTRODUCTION

Low Power (*LP*) and Low Voltage (*LV*) circuits are nowadays extensively demanded by the market of portable applications (computers, phones, biomedical implants) [1]. This is leading the circuit design philosophy to environments where the scaling down of the power supply is continuously decreasing, but where the circuit performance must be also retained. Filters are building blocks appearing on demanded *LP*/*LV* products. Continuous Time Filters (*CTF*) could be a good choice *versus* the sampled-data filters alternatives, because they avoid the *pre* and *post-aliasing* filters. Also, they reduce the components spread (capacitors, current gains, *etc.*) if large time constants, as in audio-frequency applications are required. One of the main drawbacks of *CTF* is that tuning processes are necessary due to technological process variations, but on the contrary clock-noise is absent.

Continuous Time Filters performance is directly related to the continuous time integrator quality measured in terms of power consumption, linearity, noise, phase response and tunability as main parameters. In the context of *LV*/*LP* circuits, some contributions have been reported. Looking at the technology capabilities, a first approximation could classify them in bipolar, *BiCMOS* or *CMOS* designs. Totally bipolar realizations can work at

*e-mail: esther@imse.cnm.es
†Corresponding author. Tel.: +34-955056666, Fax: +34-955056692, e-mail: yufera@imse.cnm.es
‡e-mail: rueda@imse.cnm.es

LV [2, 3], until 1 *V* of supply voltage [3]. The best performance in terms of power efficiency and dynamic range for *LP/LV CTFs* has been proved for these technological realizations in [4, 5]. This optimal performance is obtained with a non-linear integration method preserving linear input-output relationship (companding technique [6]). They seem to be a good candidate for low-voltage high-frequency operation [7], although good results have been also obtained in the audio frequency range [8]. *CMOS* realizations are based on biasing transistors at strong inversion, on saturation [9–11] or linear [12, 13] region, and also in weak inversion mode [14–16]. Companding realizations can be found in *CMOS* technologies, being possible to be ruled either by squared-root [11] or by logarithmic [15, 16] laws, unlike bipolar designs. This fact makes possible to distinguish between so called *log-filters* and $\sqrt{x}$-*filters*. The *BiCMOS* technologies make compatible the reduced voltage swing for bipolar transistors with *MOST* working at linear region. In Refs. [17, 18] circuit techniques are used to limit the drain-to-source voltage on *MOST*.

In this paper, a biquad based on a new transconductor realization is presented. The circuit is based on the *FGMOS* transistor principle [19–20]. The use of this technique makes easy the voltage-down process without degrading the circuit performance parameters. The specifications are focused on the audio frequency range. Large time-constants for low frequencies (some tens of *Hz*) need low g_m/C ratios, which forces to low transconductance values and large integrating capacitors as well as high output resistance. The transconductor has good programming and tuning characteristics. Fully balanced input-output operation has been used in order to reduce distortion, so the proposed transconductor includes a new common-mode feedback circuit (*CMFB*). The common-mode feedback circuit presented also exploits the processing capabilities of the *FGMOS* technique. The simulation results obtained are compared to other audio-frequency filter realizations.

II. FGMOS BASIC PRINCIPLE

In the *FGMOS* technique exposed in [19], the drain-to-source current characteristic of a *MOS* transistor is externally modified by adding a set of capacitors connected to the gate terminal as shown in Figure 1(a). Here, the *FGMOS* transistor has V_i ($i=1,2,\ldots,n$) input voltages. C_i are the input capacitors, C_{ox} the floating-gate oxide capacitance, and C_{FD}, C_{FS} and C_{FB} the overlap capacitances between the floating-gate to the drain, source and bulk respectively. The equivalent circuit and schematic are shown in Figures 1(b) and (c), respectively. The drain-to-source current in saturation if $C_{FD}, C_{FS} \ll C_T$ is given by,

$$I_D = \beta_n \left(\sum_{i=1} w_i V_i + w_B V_B - w_S V_S - w_T V_{th} \right)^2 \quad (1)$$

where β_n is the transconductance parameter, V_{th} is the nominal transistor threshold voltage, V_B and V_S the body and source voltages respectively. The weights in Eq. (1) are defined as: $w_i = C_i/C_T$, $w_B = C_{FB}/C_T$, $w_S = [1-(C_{FB}/C_T)-2/3(C_{ox}/C_T)]$, $w_T = [1-2/3(C_{ox}/C_T)]$, being C_T the total capacitance seen from the floating gate.

Let us consider the three-input *FGMOS* case, where V_1 is the input signal ($V_{in} = V_1$), and V_2 and V_3 are bias voltages ($V_{b2} = V_2$ and $V_{b3} = V_3$). For $V_S = V_B = 0$, the following expression results from Eq. (1),

$$I_D = \beta_n (w_1 V_1 + w_2 V_2 + w_3 V_3 - V_{th})^2 \quad (2)$$

in which, the drain-current is given as a quadratic dependence of input voltages' weighted sum.

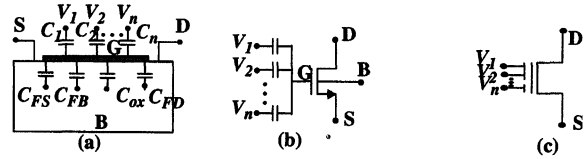


FIGURE 1 Floating-Gate MOS (FGMOS) transistor: (a) Capacitors model. (b) Equivalent circuit. (c) Schematic.

When $C_1 \gg C_{ox}$, Eq. (2) can be rewritten as,

$$I_D = \beta_n \cdot \frac{C_1^2}{C_T^2}(V_{in} - V'_{th})^2 \quad (3)$$

where,

$$V'_{th} = V_{th} + \frac{C_2}{C_1} \cdot (V_{th} - V_{b2}) + \frac{C_3}{C_1} \cdot (V_{th} - V_{b3}) \quad (4)$$

This expression enables the reduction of the threshold voltage seen from the input terminal (V_1). In order to obtain this, it must be fulfilled that $V_{b2} > V_{th}$ and/or $V_{b3} > V_{th}$. The magnitude of the reduction is controlled by the input capacitor ratios C_i/C_1 ($i = 2, 3$). As consequence, the requirements for voltage-down are less restrictive. If $C_1 = C_2 = C_3$ and $V_2 = V_3 = 1.5\,V_{th}$, a $V'_{th} = 0$ is obtained.

Equation (2) can be also interpreted as follows: the *FGMOS* transistor has two inputs, $V_{in+} = V_1$ and $V_{in-} = V_2$, and a bias signal, $V_{b3} = V_3$. The inputs are symmetrical with respect to the common mode level ($V_{cm} \pm V_{id}/2$), and its weights are equals, $C_1 = C_2$. The result for this selection is,

$$I_D = \beta_n \cdot \frac{C_1^2}{C_T^2}(V_{cm} - V'_{th})^2 \quad (5)$$

where the a threshold voltage,

$$V'_{th} = V_{th} + \frac{C_3}{C_1} \cdot (V_{th} - V_{b3}) \quad (6)$$

smaller than V_{th} can be obtained if $V_{b3} > V_{th}$. The operation expressed in (5) represents the calculus of the mean value of the two input signals through the gate-to-source voltage of a *MOST*. This gate-to-source voltage is equal to the voltage common-mode value, with a threshold voltage controlled by V_{b3}. This sensing method for the V_{cm} voltage can be used for common-mode correction *via* feedback or feedforward circuits. In the following section, these two basics interpretations of the floating-gate *MOS* transistor operation are applied to build the transconductor used in the biquad filter we propose to show the feasibility of *FGMOS*-based implementations.

III. FILTER IMPLEMENTATION

The proposed g_m-C integrator is shown in Figure 2 [21]. The transconductor is a pseudo-differential pair composed of $M1-M4$, with $M9-M10$ as active load and a *CMFB* circuit which will be described later on. The $M1-M4$ three-input *FGMOS* transistors work as a two cross-coupled pair, giving a current defined by $(I_B - I_2)$ or $(I_1 - I_B)$, being $I_1 + I_2 = 2I_B$, and I_B the bias current. The aspect ratios and input capacitors for these transistors are the same, being different the bias voltages, V_{b1} and V_{b2}. When transistors are in saturation region, the output current is calculated as,

$$I_L = \frac{2\beta_n C_{in} C_c (V_{b2} - V_{b1})}{C_T^2} \cdot (V_{in1} - V_{in2}) \quad (7)$$

where β_n is the transconductor parameter $\mu_n C_{ox} W/L$, C_{in} is the input capacitance connected to $V_{in1,2}$, and C_c the control capacitor connected to V_{b1} and V_{b2} respectively. C_T is the total capacitance seen from a floating gate. The large signal transconductance,

$$G_m = \frac{2\beta_n C_{in} C_c (V_{b2} - V_{b1})}{C_T^2} \quad (8)$$

can be easily tuned through the $(V_{b2} - V_{b1})$ factor. Values of negative resistances can be also obtained

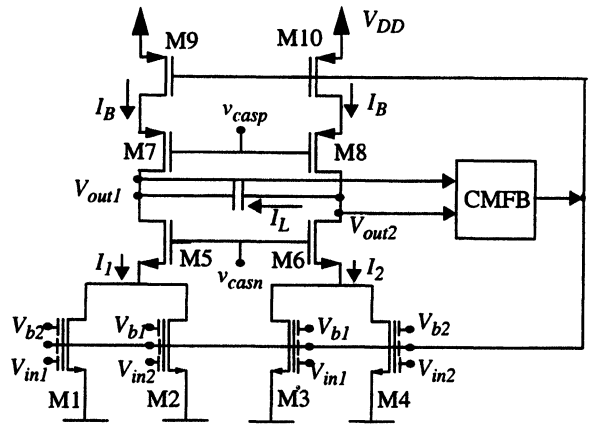


FIGURE 2 Fully-differential FGMOS integrator.

if necessary. Capacitor and voltage biasing value are selected in agreement with Eq. (4) in order to reduce the input voltage levels and maintaining *MOST* on saturation and strong inversion.

The schematic of the *CMFB* circuit used is represented in Figure 3. It is composed of a differential pair ($M12, M13$) with diode-connected transistors as loads ($M14, M15$). The *FGMOS* pair has the same total input capacitance ($C_{T,12} = C_{T,13}$), and all the capacitors have the same value. The constant reference voltage ($V_{DD}/2$) is obtained from the mean value of V_{DD} and ground. According with Eq. (5), the current through $M13$ is,

$$I_{D13} = \beta_n \left(\frac{V_{dd}}{2} - V'_{th} \right)^2 \tag{9}$$

where the new threshold voltage, for equal input capacitors at V_{DD} and *gnd* inputs is,

$$V'_{th} = V_{th} + V_s \tag{10}$$

which is compared with the equivalent gate voltage at $M12$. The V_s is the common source voltage of the differential pair. The drain current in this case is,

$$I_{D12} = \beta_n (V_{cm} - V'_{th})^2 \tag{11}$$

where the new threshold voltage is the same as $M13$ given in Eq. (10). The differential pair will be unbalanced when the common-mode level is not zero (for symmetrical power supplies), sensing the common-mode voltage level. The output of this circuit is connected to the transconductor bias current and a capacitor input of the cross-coupled input pair to obtain a negative feedback. The common-mode voltage level can be easily defined by the capacitor ratios at the *CMFB* circuit.

The transconductor has been used as basic block for a second order Tow-Thomas filter. The schematic of this block is shown in Figure 4. The equations describing filter operation are:

$$\frac{V_{BP}(s)}{V_{in}(s)} = -\frac{s \cdot (g_{m1}/C_1)}{s^2 + s \cdot (g_{m2}/C_1) + (g_{m3}g_{m4}/C_1C_2)} \tag{12}$$

$$\frac{V_{LP}(s)}{V_{in}(s)} = \frac{(g_{m1}g_{m3})/(C_1C_2)}{s^2 + s \cdot (g_{m2}/C_1) + (g_{m3}g_{m4}/C_1C_2)} \tag{13}$$

where the typical filter parameters of a second order section are,

$$\omega_o = \sqrt{\frac{g_{m3}g_{m4}}{C_1C_2}} \tag{14}$$

$$Q = \frac{\sqrt{g_{m3}g_{m4} \cdot C_1/C_2}}{g_{m2}} \tag{15}$$

being ω_o and Q the cut-off frequency and the quality factor, respectively. Using Eqs. (14)–(15), the ω_o and Q tuning can be performed through control voltages V_{b1} and V_{b2} as shows Eq. (8).

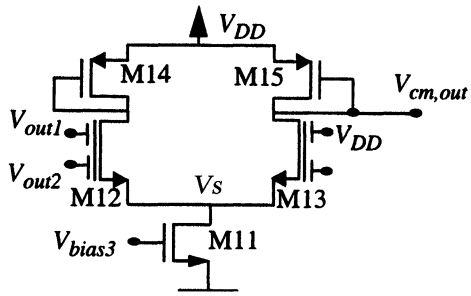


FIGURE 3 Common-mode feedback circuit.

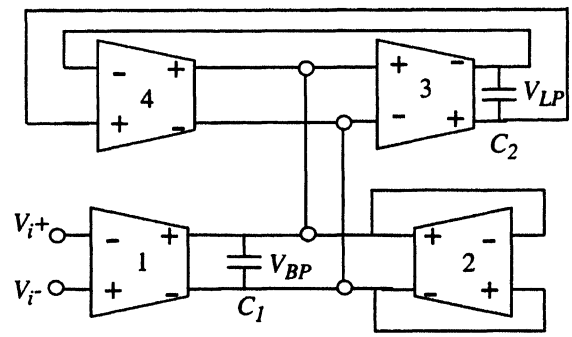


FIGURE 4 Tow-Thomas biquad.

IV. RESULTS

The design of a filter illustrating the circuits described before has been focused for low-voltage audio applications. The time constant required are in the range of [10 ms, 25 μs] for frequencies between 100 Hz to 40 KHz respectively. These time constants can be implemented by choosing the adequate transconductance to capacitance ratio ($g_m/2\pi C_{i=1,2}$) in Eqs. (12)–(13). The lowest time constant imposes large capacitor values, so a trade-off between capacitor area and G_m value is necessary. For $C_i = 5$ pF and a frequency range between 100 Hz and 10 KHz g_m is located between 0.3 μS and 3 nS. Cascode transistor structures were used at the outputs to increase the output resistance. The $M1-M4$ transistors are $W/L = 2.5\,\mu m/10\,\mu m$, with capacitance values of 150 fF, 250 fF and 600 fF for the inputs. The $M12$ and $M13$ aspect ratio is 2.5 μm/17 μm, with input capacitances of 133 fF, and the total capacitance is 0.533 fF.

Electrical simulations have been performed in a 0.8 μm CMOS technology, with nominal threshold voltages of $V_{tn} = 0.85$ V and $V_{tp} = -0.75$ V. BSIM3v2 models have been used for MOST. Figure 5 shows simulation results for the output current (I_L) *versus* the differential input voltage for several values of the control voltage ($V_{b2} - V_{b1}$). In both, the high linearity of the transconductor and

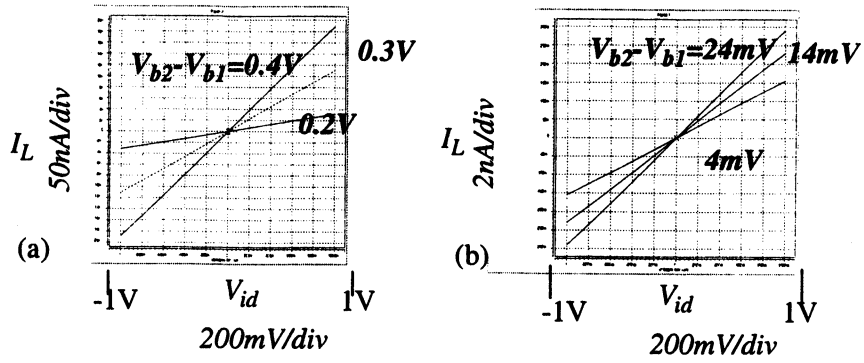


FIGURE 5 G_m-tuning: (a) for $(V_{b2} - V_{b1}) \sim 0.2$, 0.3 and 0.4 V and (b) for $(V_{b2} - V_{b1}) \sim 4$, 14 and 24 mV.

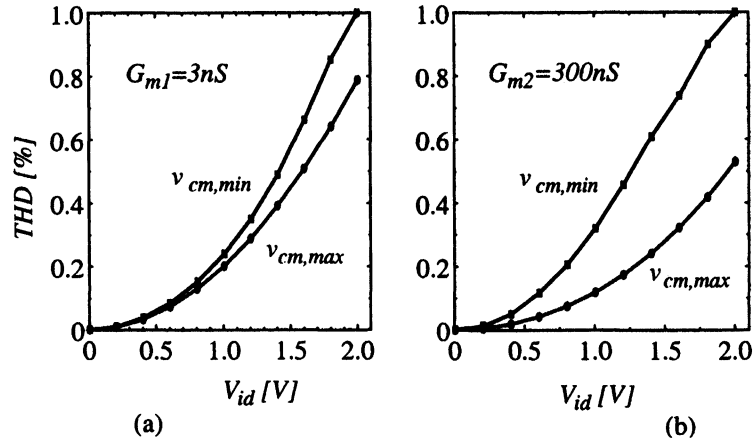
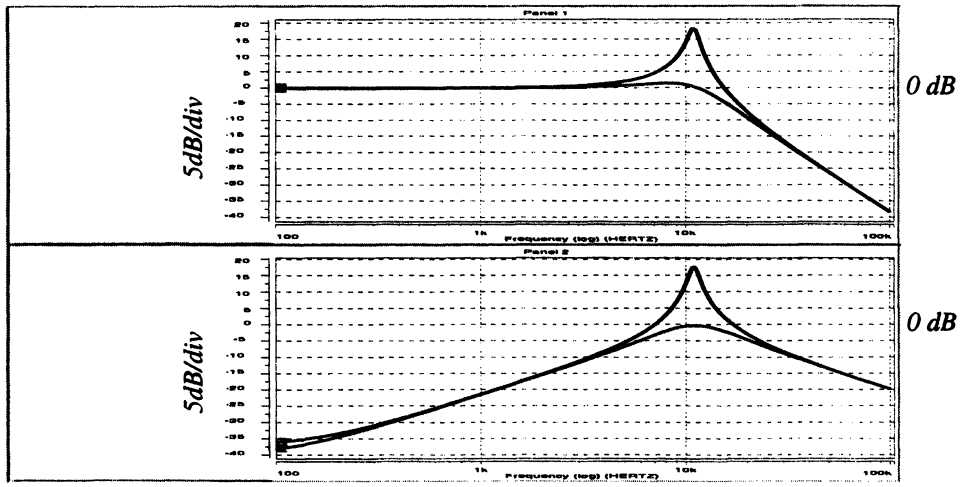


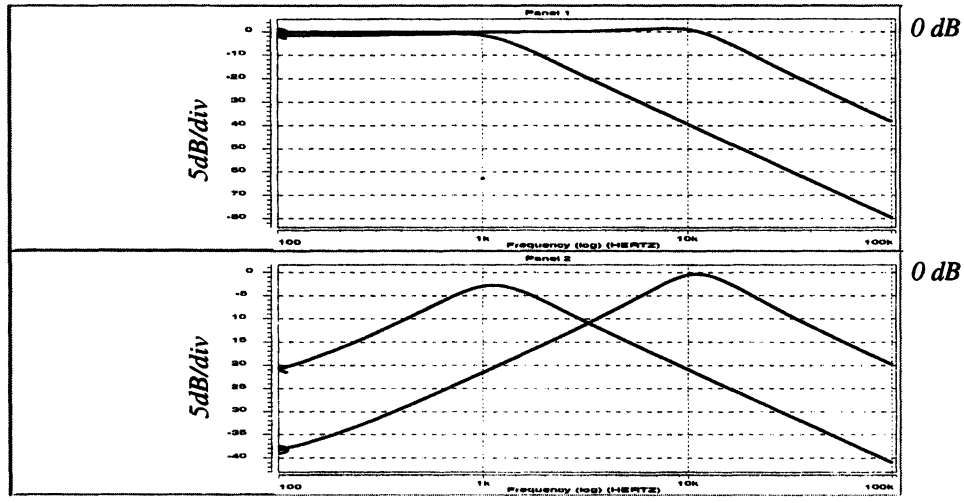
FIGURE 6 THD *versus* peak-to-peak input range: (a) for $G_m = 3$ nS and (b) for $G_m = 300$ nS.

the extremely wide input voltage range can be observed. The results obtained with this graphic agree with Eq. (8). The low distortion has been confirmed by transient analysis. The *THD* obtained for $g_{m1} = 3\,\text{nS}$ and $g_{m2} = 300\,\text{nS}$ are shown in Figures 6(a) and (b) respectively. Both have been calculated at the edges of the input Common-Mode Range ($V_{cm,min} \sim 0\,\text{V}$, $V_{cm,max} \sim 0.8\,\text{V}$). The total *THD* is always below 1%.

Finally, in Figure 7, the bandpass and lowpass filter transfer function have been obtained for two values of the cut-off frequency and the quality



(a)



.1KHz 1KHz 10KHz 100KHz

(b) Frequency

FIGURE 7 (a) Q-tuning and (b) ω_o-tuning for both band-pass and low-pass filter transfer-functions.

TABLE I Summary of transconductor HSPICE simulations

	$g_{m1}=3\,nS$		$g_{m2}=300\,nS$
V_{supply}		$2\,V$	
I_B		$1.6\,\mu A$	
$V_{id}(V_{pp})$	$2\,V$		$2\,V$
CMR	$0.8\,V$		$0.8\,V$
$THD@2\,V$		$<1\%$	
$Power$		$10\,\mu W$	

factor. Table I summarize the performance of the transconductor for the maximum and the minimum transconductance values.

V. CONCLUSIONS

A *LV/LP* filter implementation based on a new *FGMOS* transconductor has been presented. The transconductor uses *FGMOS* to decrease the supply requirements as well as to tune the filter cut-off frequency, obtaining a full range differential input voltage and two decades for frequency tuning. Harmonic distortion is always below one per cent for all input values. The voltage common-mode correction is performed also by calculating its possible swing by means an *FGMOS* differential pair. The feasibility of the block has been illustrated with a second order Tow-Thomas biquad. The obtained results agree with expectations, and propose a close solution for low voltage, low frequency applications with the *FGMOS* technique.

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Authors' Biographies

Esther Rodríguez-Villegas received the B.S. degree in Electronics from the University of Sevilla, Spain in 1996. Since 1997 she is in the Institute of Microelectronics at Seville (IMSE) where is currently working toward the Ph.D. degree. Her main research interests are the design of Floating-Gate circuits for both digital and analog applications.

Alberto Yúfera joined the Department of Electronics and Electromagnetism at the University of Seville in 1988 as Assistant Professor, and obtained the Ph.D. degree in 1994. Since 1991 he is Associate Professor in the Department of Electronic Technology at the University of Seville. In 1989 he became researcher at the Department of Analog Design of the National Microelectronics Center (CNM), now Institute of Microelectronics at Seville (IMSE). He has participated in several research projects financed by the Spanish CICYT and in ESPRIT Projects. He has published several technical papers in main international journals and conferences. His current research interests include analysis and design of analog integrated circuits and systems for signal processing, and development CAD tools for analog circuits.

Adoración Rueda joined the Department of Electronics and Electromagnetism at the University of Seville in 1976 as Assistant Professor, and obtained the Ph.D. degree in 1982. From 1984 to 1996 she was Associate Professor in that Department, where now holds the position of Professor in Electronics. In 1989 she became researcher at the Department of Analog Design of the National Microelectronics Center (CNM), now Institute of Microelectronics at Seville (IMSE). She has participated in several research projects financed by the Spanish CICYT or by the European Community. She has also published several technical papers in main international journals and conferences, and she won the Best Paper Award of the 10th IEEE VLSI Test Symposium in 1992. Her current research interests are design and test of analog and mixed analog/digital circuits, and development of CAD tools. She is member of the Institute of Electrical and Electronic Engineers.