CMOS Design of a Current-Mode Multiplier/Divider Circuit with Applications to Fuzzy Controllers

Abstract

Multiplier and divider circuits are usually required in the fields of analog signal processing and parallel-computing neural or fuzzy systems. In particular, this paper focuses on the hardware implementation of fuzzy controllers, where the divider circuit is usually the bottleneck. Multiplier/divider circuits can be implemented with a combination of A/D-D/A converters. An efficient design based on current-mode data converters is presented herein. Continuous-time algorithmic converters are chosen to reduce the control circuitry and to obtain a modular design based on a cascade of bit cells. Several circuit structures to implement these cells are presented and discussed. The one that is selected enables a better trade-off speed/power than others previously reported in the literature while maintaining a low area occupation. The resulting multiplier/divider circuit offers a low voltage operation, provides the division result in both analog and digital formats, and it is suitable for applications of low or middle resolution (up to 9 bits) like applications to fuzzy controllers. The analysis is illustrated with Hspice simulations and experimental results from a CMOS multiplier/divider prototype with 5-bit resolution. Experimental results from a CMOS current-mode fuzzy controller chip that contains the proposed design are also included.

I.- Introduction.

Multiplier/divider circuits are usually required in the fields of analog signal processing and parallel-computing neural or fuzzy systems [1-19]. In this paper, we will focus on the application to fuzzy controllers, which are currently drawing a great attention. Typical fuzzy systems like Mamdani's or Takagi-Sugeno's types infer a crisp (not fuzzy) output by aggregating all the rules' conclusions and performing a division. One of the main problems that appears when implementing a fuzzy system in hardware is the selection of an adequate divider circuit. The divider is usually the circuit that limits the speed, precision and interface capabilities (it is the output block) of the resulting fuzzy chip [1-9].

Several techniques to design multiplier/divider circuits have been proposed in the literature. Conventional log-antilog or bipolar translinear techniques have been employed in the analog fuzzy

chips described in [1-2]. These structures can be realized with CMOS technology by using MOS transistors working in subthreshold region. However, the low current levels make them operate slowly [10]. Low operating speed is also the main limitation of multiplier/dividers based on the time-division technique [11]. The MOS translinear principle is another approach. In this case, the main limitation is a low resolution because the performance of the resulting circuits is very sensitive to deviations from the simple square-law model of the transistors in saturation, caused by length-channel modulation, mobility reduction or mismatching [3][12][13]. Another technique widely employed is to invert the behavior of a multiplier by using local feedback or by inserting it in the feedback path of an inverting amplifier. Performance of these multiplier/dividers depends primarily on the performance of the multiplier and the amplifier employed. Precision is mainly limited by offsets associated with the input and output variables [3][14][15]. The analog fuzzy chips reported in [4-7] contain this type of multiplier/dividers.

An alternative solution is the successive-approximation technique that employs two accumulators, as shown in Figure 1 [16]. The master accumulator approximates the value of the input signal, x_{num}, after N steps:

$$x_{num} \cong x_{den} \cdot \sum_{i=1}^{N} 2^{-i} \cdot b_i \tag{1}$$

where x_{den} is a reference signal and b_i is a digital output whose value is "1" ("0") if the output of the master accumulator at the i-th step is smaller (bigger) than x_{num}.

The slave accumulator takes the set $\{b_i\}$ and another reference signal, x_p, as inputs and provides the following output:

$$x_{out} = x_p \cdot \sum_{i=1}^{N} 2^{-i} \cdot b_i \tag{2}$$

Solving equations (1) and (2), it follows that:

$$x_{out} \cong x_p \cdot \frac{x_{num}}{x_{den}} \tag{3}$$

with a quantization error of $\pm\, x_{den} / 2^{(N+1)}$.

Hence, the output $\{b_i\}$ is the digital code of the division x_{num}/x_{den} while x_{out} is the analog discrete signal that represents the multiplication/division $x_p \cdot x_{num}/x_{den}$.

This technique has been employed in [17] to implement a voltage-mode multiplier/divider circuit, using A/D and D/A switched-capacitor (SC) cyclic converters as master and slave accumu-

lators, respectively. In that proposal, the analog output is provided after two stages. The first of them consists of N steps in which the N bits of the digital output are obtained. The digital code is converted to analog format during the next stage which again consists of N steps. SC successive-approximation multiplier/dividers have been employed in the fuzzy controllers described in [8-9].

The CMOS multiplier/divider circuit proposed in this paper implements the successive-approximation technique with current-mode algorithmic converters that occupy smaller area and are capable of working at lower voltage supplies than their voltage-mode counterparts. The A/D and D/A converters employed are coupled in the sense that they begin conversion by the same bit (the most significant bit, MSB) so that the analog and digital outputs are provided after only one stage. Besides, the response time can be smaller than N times the duration of the slowest operation because continuous-time data converters are employed. Several circuit structures to design these current-mode continuous-time algorithmic converters are proposed in this paper, following the work in [20]-[24]. They are discussed and compared in terms of static and dynamic features in Section II. The most efficient of these structures enables realization of small and fast multiplier/divider circuits suitable for applications of low or middle resolution (below 9 bits, which is higher than the resolution obtained by many of the above commented proposals). Performance of the proposed multiplier/divider circuit is illustrated with Hspice simulation and has been verified with a 2.4-μm CMOS prototype with 5-bit resolution. These results are included in Section III. Section IV illustrates with experimental results the application of the proposed design to implement the divider in a current-mode CMOS fuzzy controller chip. Finally, Section V provides some conclusions of the work.

II.- Circuit design.

Among the different designs of current-mode converters, algorithmic types are widely used because they are very simple and modular. If switched-current techniques are employed, an iterative cyclic or a pipeline design can be implemented. In the first case, a cell performs the conversion of all the N bits sequentially so that the response time and throughput of the converter is N clock cycles. In the second case, an extreme realization is to employ a cascade of N bit cells that provide a bit every clock cycle so that the response time is also N clock cycles but the throughput is only one [23][24]. If continuous-time techniques are employed, the data converter also consists of a cascade of N bit cells but no control circuitry is required to govern the signal transmission from one cell to another [20]. Besides, the response time can be smaller than N times the duration of the slowest operation. A disadvantage is that the converters are sensitive to mismatching among the

cells, so that resolution is limited typically to 9 bits [25].

Considering applications of low or middle resolution like IC realizations of fuzzy controllers, we have selected continuous-time algorithmic converters to reduce the control circuitry and the response time. The resulting multiplier/divider circuit has the modular structure shown in Figure 2. Each bit cell contains an A/D and a D/A bit cell that provide, respectively, a bit of the digital output, $\{b_i\}$, and a contribution to the analog output, I_{out}. As described in Section I, the output $\{b_i\}$ is the digital code of the current-mode division I_{num}/I_{den} while I_{out} is the discrete current that represents the multiplication/division $I_p \cdot I_{num}/I_{den}$. Design considerations for the A/D and D/A bit cells are given in the following.

II.a Design considerations for the A/D bit cells.

Most reported algorithmic A/D converters [18-22] implement the multiplying algorithmic conversion. However, the dividing algorithmic conversion (illustrated in Figure 3) is more suitable for a divider circuit in order to have I_{den} as the full-scale current of the A/D converter (master accumulator) and $I_{den}/2^N$ as the quantization step (refer to Equation (1)). Focused on this case, the input range for I_{num} is $I_{num} \leq I_{den}$.

Using a current-mode approach, the operations required by an algorithmic A/D conversion are performed by current mirrors and current comparators. Regarding accuracy, the limit is imposed by mismatching in the current mirrors due to systematic and random errors. Random errors are caused mainly by threshold voltage variations between ideally identical transistors, and can be reduced by employing large devices (with a typical limit of 9 bits) [25]. Systematic errors may decrease this potential resolution. On one hand, they are caused by a difference between the input and output voltages of the current mirrors, and on the other, by their finite output resistance. Regarding operation speed, this is limited by the transient response of the current mirrors and by the settling time of the current comparators.

In the following, we propose and discuss three structures of A/D bit cells that combine different circuit techniques to improve resolution and speed. The starting point is the dividing version of the original multiplying-type A/D bit cell proposed in [20]. This cell, which will be named type_0 cell, is illustrated in Figure 4. Its resolution is limited mainly by the systematic errors that appear at the subtraction operation, $R(I_i) - R(I_{den}/2^i)$, where $R(.)$ represents the replication operation implemented by a current-mirror. To reduce this problem, which is caused by the high voltage swing at node *x*, the proposal in [20] is to use active current mirrors, at the cost of more area and power consumption. On the other side, the speed of this type_0 cell is limited mainly by the re-

sponse time of the current comparator, which is based on a cascade of inverters like that described in [26].

Type 1 cells: The first modification we propose to improve the performance of the type_0 cell is the type_1 cell which is illustrated in Figure 5. It implements the flow chart of Figure 3, so that its output current I_{oi} is given by:

$$I_{oi} = b_i \cdot \left[\Re(I_i) - \Re\left(\frac{I_{den}}{2^i} \right) \right] + \overline{b_i} \cdot \Re(I_i) \tag{4}$$

where the bit b_i is obtained from the comparison of $R(I_i)$ with $R(I_{den}/2^i)$.

The most important systematic errors, which appear at the subtraction operation, $R(I_i)$ - $R(I_{den}/2^i)$, are reduced with the regulated output stage of the mirrors that replicate I_i and $I_{den}/2^i$. This output stage is also exploited to perform as a fast current comparator like that proposed in [27][28]. Since the input to this comparator is capacitive like in the type_0 cells, the offset is virtually zero and resolution is not degraded. Hence, an A/D converter based on these cells can occupy less area than another based on type_0 cells for a given resolution and range of operation.

Another advantage of type_1 cells is that their speed is higher since the comparator employed is faster. The cost to pay for it is a higher power consumption because one of the inverters in the current comparator acts as an amplifier and consequently, the quiescent current through it is not null. As usual, the higher the quiescent current the higher the speed. The fast response of the comparator and the capacitive coupling between nodes *z* and *x* may cause glitches in the digital output. Let us analyze this problem in the bit cell shown in Figure 5. When b_i is "1", the pmos transistor M_p that acts as a switch is off, the voltage at node *x* is high (M_3 is off) and the voltage at node *y* is low. When b_i changes to "0", ($R(I_i) < R(I_{den}/2^i)$), the pmos switch begins to conduct and the voltage at the high-impedance node *x* decreases rapidly following the voltage at the low impedance node *y*. The drain-to-gate capacitance, C_{gd}, of transistor M_3 and the gate-to-source capacitance of transistors M_1, M_2, and M_3, C_{gs}, cause a capacitive coupling between nodes *z* and *x* so that:

$$\Delta V_z \cong \Delta V_x \cdot \frac{C_{gd}}{C_{gd} + 3C_{gs}} \tag{5}$$

The voltage decrease induced at node *z* can make $R(I_i)$ be momentarily superior to $R(I_{den}/2^i)$. Hence, b_i can return to "1" if the comparator is too fast. In this sense, the type_0 cells can be seen as a conservative design because they employ slow comparators.

Glitches have to be reduced if high-speed operation is required. A solution is to include the

transistor shown with grey lines in Figure 5. This transistor is conducting when b_i is "1", making low the voltage at node *x*. Therefore, a change of b_i from "1" to "0" causes a momentary increment in the voltage at *x* and, indirectly, at *z*. Opposite to the above commented situation, this affirms the "0" value of b_i. Figure 6 illustrates how glitches are reduced with this solution. It corresponds to the Hspice transient simulation of an A/D converter of 5 bits when the digital code changes from 10000 to 01111 (I_{den} is 16μA and I_{num} is a square pulse between 8.25μA and 7.75μA). Figures 6a and b show, respectively, the voltage of the least significant bit, b_5, and the output current, I_{o5}, of the 5^{th} bit cell, when the bit cells contain (black line) or do not contain (grey line) the additional transistors to reduce glitches.

Type 2 cells: The multiplying bit cells of the A/D converter proposed in [21] employ a current injection technique (addition of a bias current, I_b) to increase the speed of the current mirrors and to decrease the voltage swings at the nodes, thus reducing systematic errors. We have applied this technique to dividing-algorithmic converters. The resulting flow chart and, consequently, the resulting bit cells, which will be named type_2 cells, are simpler than that obtained for multiplying converters, as can be seen in Figure 7. The schematic of this type_2 cell, which also employs a fast current comparator, is shown in Figure 8. Its output current I_{oi} is given by:

$$I_{oi} = \Re(I_i) - b_i \cdot \Re\left(\frac{I_{den}}{2^i}\right) \tag{6}$$

where the bit b_i is obtained by comparing $R(I_i)$ with $R(I_{den}/2^i) + R(I_b)$.

The design of these cells has to be more careful than that of type_1 cells to achieve the same resolution. The reason is that the bits b_i are obtained by comparing currents that suffer more replicas and, hence, they are susceptible of more errors.

The most significant glitches of these cells appear when the nmos transistor that acts as a switch (M_n in Figure 8) begins to conduct. However, they are not so important as they were in the not improved type_1 cells because the difference between the voltages at nodes *x* and *y* when the switch is open are not so high. Consequently, the operation speed of these cells can be similar (slightly inferior) to that of type_1 cells.

Type 3 cells: Another way to increase the speed of the current mirrors in the bit cells is to always ensure a not zero current through them by modifying the conversion algorithm. The flow chart illustrated in Figure 9a is the proposal in [22] for multiplying A/D converters. Applying this idea to a dividing A/D converter, we have obtained a simpler flow chart which is shown in Figure

9b. It ensures that the output current I_{oi} of each cell is always bigger or equal to I_{den}-$I_{den}/2^i$. Figure 10 illustrates the type_3 cell that implements this algorithm. The expression of I_{oi} is the following:

$$I_{oi} = \Re(I_i) + \overline{b}_i \cdot \Re\left(\frac{I_{den}}{2^i}\right) \tag{7}$$

where b_i results from comparing R (I_i) with R (I_{den}) - R ($I_{den}/2^i$)

The additional transistor drawn with grey lines in Figure 10 is included to reduce glitches that can be very important in these cells because the currents involved are high.

Comparison: To perform a quantitative comparison of the four bit cells commented, they have been employed to design four A/D converters of 5 bits using the transistor parameters provided by a 2.4-μm CMOS technology. Their response time and average power consumption have been obtained from Hspice simulation. The results shown in Figure 11 reflect the worst case: the slowest transition (10000 to 01111) and the slow model parameters for the transistors. The left and right bars correspond to a full-scale current (I_{den}) of 16μA and 64μA, respectively (with $I_b=I_{den}/4$ and a 5-V power supply). The best trade-off power/speed is achieved by the type_1 cells (response time of 260ns-140ns and power consumption of 0.62mW-1.49mW). They also offer a good trade-off between silicon area occupation and resolution. Therefore, they have been selected as the A/D bit cells of the proposed multiplier/divider circuit.

II.b Design considerations for the D/A bit cells.

The basic structure for an algorithmic D/A bit cell is a digitally controlled current mirror, as shown in Figure 12 with black lines. The bits b_i generated by the A/D part vary during the circuit operation as I_{num} or I_{den} change. Hence, the features of the analog output I_{out} provided by the multiplier/divider circuit greatly depends on the dynamic behavior of the D/A bit cells. An important condition that should be met to reduce glitches at the output is to ensure synchronization of all the switches of the D/A cells. This is achieved by using a master-slave scheme for the latches that store the digital output $\{b_i\}$ of the digital part. Figure 13 illustrates the inclusion of this latch in the bit cell schematic of an A/D- D/A multiplier/divider that employs type_1 A/D bit cells. When H is "1" the digital word that represents the quotient I_{num}/I_{den} is calculated. When S is equal to "1" (H is "0"), the bits $\{b_i\}$ that control the D/A part are updated at the same time. The bits $\{b_i\}$ do not change when H is "1", thus maintaining both the analog (I_{out}) and the digital ($\{b_i\}$) outputs while performing a new division.

The longest delay of the D/A converter appears when the digital code changes from 00...0 to 11...1 because all the nodes *a* (in Figure 12) have to be loaded starting from V_{ss}. The typical solution to reduce this delay is to replace the single switches by differential switches that always offer a conducting path for the current [29]-[33]. In our case, we have introduced the transistor M_a shown with grey lines in Figure 12. It reduces the voltage swing at node *a* because when b_i is "0" the voltage at *a* is not V_{ss} but a bigger value close to a reference voltage, V_{ref} (which is V_{dd} in Figure 13). Figure 14 shows the Hspice transient simulation of a 5-bit D/A converter when the digital code changes from 00000 to 11111 (the reference current I_p is 16μA). The grey and black lines correspond, respectively, to a converter that uses simple and differential switches.

When b_i increases from "0" to "1", the additional pmos transistor (M_a in Figure 12) switches off once b_i becomes equal to $V_q = V_{ref} - |V_{Tp}|$, where V_{Tp} is its threshold voltage. At this value, the transistor M_1, which is on, begins to discharge the node *a* so that the nmos switch rapidly begins to conduct. Nonsymmetrical switching of these nmos transistors is the cause of the glitches that remain at the output. A simple solution to reduce this problem is to employ all the D/A bit cells identical. Another solution more costly is to choose the value of V_q as the value where the bits b_i that change to "0" and to "1" meet together, as illustrated in Figure 15. This can be achieved by tuning the value of V_{ref} externally, as proposed in [31].

III.- Experimental results.

To validate our approach, a 5-bit A/D-D/A multiplier/divider circuit has been implemented in a 2.4-μm CMOS process. It employs type_1 A/D bit cells, like that shown in Figure 5 but without additional transistors for glitch reduction, and D/A bit cells, like that shown in Figure 12 (with V_{ref} equal to V_{dd}). We estimated that by using type_1 A/D bit cells instead of type_0 cells the silicon area occupation was smaller and the operation speed was 5.7 times higher, with a power consumption that was 1.5 times higher. This prototype consists of a cascade of alternating odd and even cells which provide, respectively, the odd and even bits. This solution eliminates the pmos current mirrors between cells (shown in Figures 5 and 12), thus saving area but increasing glitches, as commented above (because the bit cells are not identical). The ratio between channel width and length of the nmos transistors is W/L=10μm/10μm. The geometry of the pmos transistors is W/L=20μm/10μm for those in the first and second bit cells and 10μm/10μm for the others. This design allows working at voltage supplies as low as 3V with input and output current ranges of 18μA. Figure 16 shows the die photograph of the circuit, whose active area is 528μm x 145μm ($0.077mm^2$). It is worth pointing out that the area occupied by this current-mode A/D-D/A design

of 5 bits is more than 4 times smaller than a 4-bit successive approximation SC A/D converter that was designed with the same technology.

Figure 17 illustrates the behavior of the circuit obtained experimentally by varying the numerator current, $I_i=I_{num}$, with the denominator current, I_{den}, equal to 12μA and the reference current, I_p, taken the values 9, 12, 15 and 18μA. Figure 18 shows the transfer function measured when sweeping the denominator current, $I_{AD}=I_{den}$, with the numerator current, I_{num}, taken the values 0, 0.25, 0.5, 0.75, and 1μA, and the reference current, I_p, fixed to 12μA. The function I_R, represented by the hyperbolic and continuous line, is the ideal division for the last case, I_{num}=1μA. The prototype was tested at a 2-V output voltage and a 3-V power supply. Since these circuits contain A/D and D/A cells, we have chosen the total error as a global figure to evaluate their precision. The total error contains the inherent quantization error as well as the gain, offset and non-linearity errors of both the A/D and D/A parts. The total error measured in this prototype is ± 2.47% with an offset of 1.82% of the full-scale current, I_{den}=12μA (the inherent quantization error is ± 1.56% with an offset of 1.56%). The 5-bit resolution (32 discrete output levels) was experimentally confirmed.

The performance of the circuit is not affected by variation of parameters due to temperature variation. Another advantage is the monotonic behavior of the converters employed. The static power consumption measured for the full scale currents, $I_{den}=I_p$=12μA, is 318μW. The response time measured for a full scale step at the input I_{num} and with I_{den} equal to 12μA is 1.23μs. The design of this prototype was not optimized regarding glitches, as commented above. Hence, the response time can be faster if applying the solutions discussed in Section II. If this is done, Hspice simulations give a response time of 120ns and a static power consumption of 409μW for the same conditions as in the experiments. Obviously, better results can be achieved with modern submicron technologies.

IV.- Application to a current-mode fuzzy controller chip.

Zero-order Takagi-Sugeno's fuzzy controllers are widely employed by their simplicity and control efficiency. They implement a set of rules like the following:

Rule i: IF x_1 is A_1^i and ... and x_u is A_u^i THEN y is c_i

where x_j (j=1,..., u) are controller input signals, y is the output, A_j^i are linguistic values defined by fuzzy sets on the input universes of discourse, and c_i are crisp values (i=1,...,R).

The control output is obtained from an average in which each consequent value, c_i, is weighted by the activation degree, h_i, of its corresponding rule:

$$y = \frac{\Sigma_i h_i \cdot c_i}{\Sigma_i h_i} \tag{8}$$

When implementing these fuzzy controllers as VLSI circuits, the signals that represent the numerator and denominator of the above expression are usually currents because currents can be added by simply connecting wires. The proposed multiplier/divider circuit is very well suited to implement equation (8) because it accepts directly the current-mode signals $\Sigma_i h_i c_i$ and $\Sigma_i h_i$. They are the input currents to the A/D part, so that $\Sigma_i h_i c_i \leq \Sigma_i h_i$ since $\Sigma_i h_i$ is the reference current of the A/D converter. The digital output of the A/D part, $Q(\Sigma_i h_i c_i / \Sigma_i h_i)$, is the control output given in digital format. The D/A part takes this digital word and a reference current, I_p, as inputs and provides the following output current:

$$I_o = I_p \cdot Q\left(\frac{\Sigma_i h_i \cdot c_i}{\Sigma_i h_i}\right) \tag{9}$$

The current I_o is the control output in analog format. Hence, the proposed multiplier/divider circuit enables IC realizations of fuzzy controllers that can interact directly with analog actuators and subsequent digital processing systems.

The A/D-D/A circuit of 5 bits described in Section III was included as a divider (hence, as the output block) in a two-input one-output fuzzy controller that was integrated in a 2.4-μm CMOS technology [34]. This fuzzy controller chip accepts inputs represented by voltages or currents and provides the control output in analog and digital format. Figure 19a shows the control output in analog format provided by the D/A part of the divider when sweeping one input variable and changing the other input as shown in Figure 19b (the inputs to the controller are represented by voltages, V_x and V_y). The output is given as a voltage because the output current of the divider was converted externally through a resistance of 10KΩ. In this case, the output is quantized into 30 values because the measured transitions cover from 00000 to 11101 (the maximum value of the c_i's was 0.875 ± 0.03125, since the consequents are programmed with 4 bits). Figure 19c shows a complete control surface provided by the fuzzy chip (the inputs to the controller are represented by currents, I_x and I_y). This surface contains 19 quantization steps because the transitions cover from 00000 to 10010 (the maximum value of the c_i's was 0.5625 ± 0.03125 in these measures). The error between the measured and the ideal quantization values is ± 0.22 LSB, thus confirming the 5 bit resolution of the A/D-D/A multiplier/divider of the fuzzy chip.

Figure 19d shows several step responses of the discrete analog output of the chip. The response time showed to be less than 2μs, which means an inference speed above 0.5 MFLIPS (Mega

Fuzzy Logic Inferences Per Second). This is a high inference speed considering that the multiplier/ divider circuit was not optimized regarding speed, as commented in Section III.

V.- Conclusions.

A current-mode multiplier/divider based on the successive approximation technique has been proposed and its static and dynamic behavior has been analyzed. It employs continuous-time algorithmic data converters whose bit cells enable a better trade-off speed/power than others previously reported while maintaining a low area occupation. Simulation and experimental results from a 2.4-μm CMOS prototype of 5-bit resolution verify these features: small silicon area (0.077 mm^2), capability of working at low voltage supply (3 V), and high speed (response time of a few hundreds of nanoseconds for a power consumption below the milliwatt). The proposal is suitable for applications of low or middle resolution (up to 9 bits) and offers the flexibility of providing the division value in both digital and analog formats. In particular, it has been applied to implement the output divider block of a fuzzy controller chip that can interact directly with analog actuators and digital processing environments.

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FIGURE CAPTIONS

Figure 1. Structure of a successive-approximator multiplier/divider.

Figure 2. Modular structure of the multiplier/divider proposed.

Figure 3. Flow chart of the dividing algorithmic conversion method.

Figure 4. Schematic of the type_0 cell.

Figure 5. Schematic of the type_1 cell.

Figure 6. Comparison of the dynamic behavior of a 5-bit A/D converter based on the type_1 cells with additional transistors (black lines) and without them (grey lines): (a) Transition of the least significant bit, b_5. (b) Output current I_{o5} of the last bit cell.

Figure 7. Flow chart of the algorithmic conversion method with current injection: (a) Multiplying type [21]. (b) Dividing type.

Figure 8. Schematic of the type_2 cell.

Figure 9. Flow chart of the algorithmic conversion method with algorithmic restriction: (a) Multiplying type [22]. (b) Dividing type.

Figure 10. Schematic of the type_3 cell.

Figure 11. Comparison of the different A/D bit cells considered.

Figure 12. Dividing algorithmic D/A bit cell.

Figure 13. Schematic of the selected A/D-D/A bit cell.

Figure 14. Output current of a 5-bit D/A converter for a full-scale step when simple switches (grey line) and differential switches (black line) are employed.

Figure 15. Value of V_q to reduce nonsymmetrical switching of the D/A part.

Figure 16. Die photograph of a 5-bit multiplier/divider prototype.

Figure 17. Experimental results of the circuit operating as a multiplier.

Figure 18. Experimental results of the circuit operating as a divider.

Figure 19. Experimental results of the proposed circuit integrated within a fuzzy controller chip: (a) Analog control output provided by the divider corresponding to the sweeping depicted in the control surface of (b). (c) An experimentally obtained control surface. (d) Several step responses of the discrete analog control output.

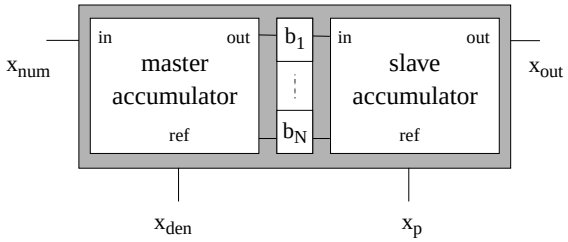


Fig 1: Structure of a successive-approximator multiplier/divider.

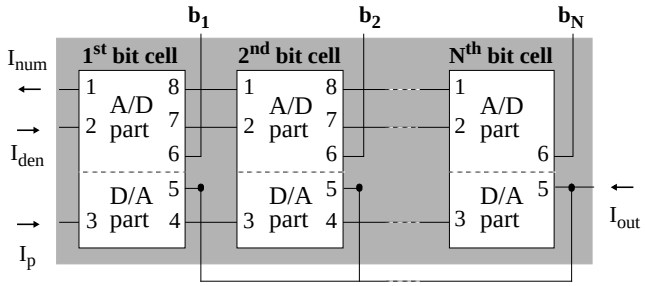


Fig 2: Modular structure of the multiplier/divider proposed.

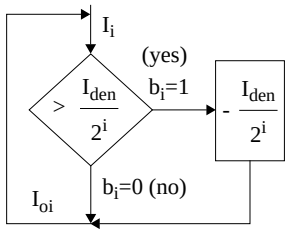


Fig. 3: Flow chart of the dividing algorithmic conversion method.

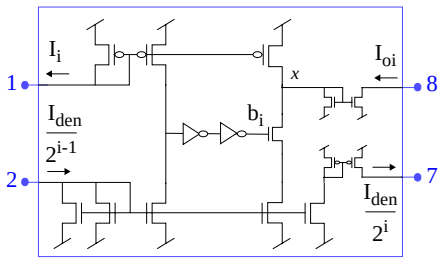


Fig 4: Schematic of the type_0 cell.

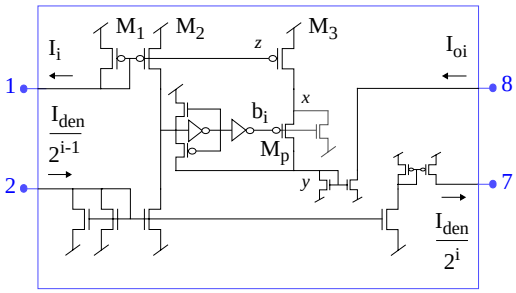
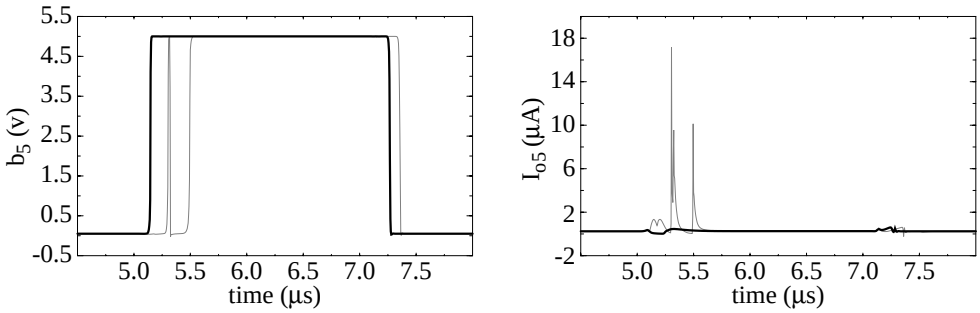
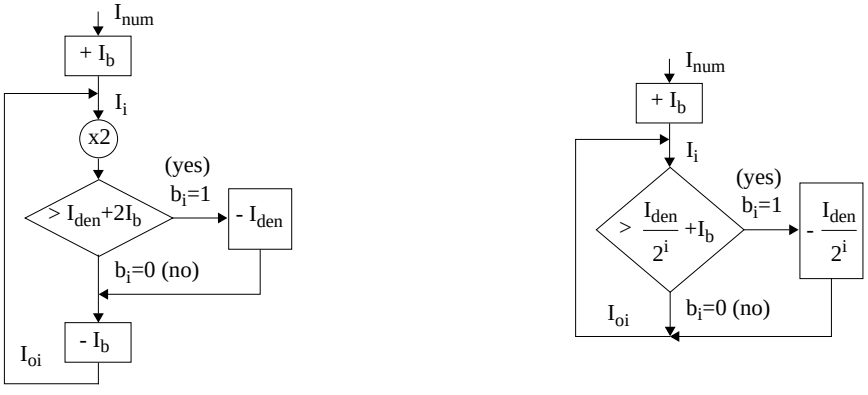


Fig 5: Schematic of the type_1 cell.



(a) (b)

Fig. 6: Comparison of the dynamic behavior of a 5-bit A/D converter based on the type_1 cells with additional transistors (black lines) and without them (grey lines): (a) Transition of the least significant bit, b_5. (b) Output current I_{o5} of the last bit cell.



(a) (b)

Fig. 7: Flow chart of the algorithmic conversion method with current injection: (a) Multiplying type [21]. (b) Dividing type.

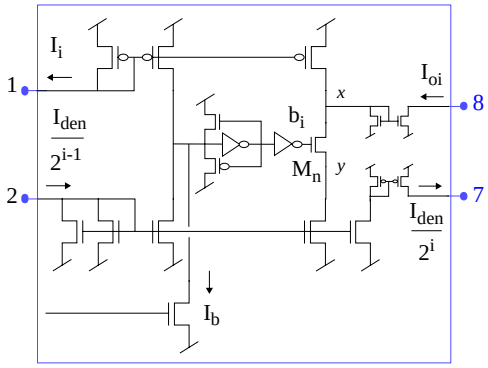
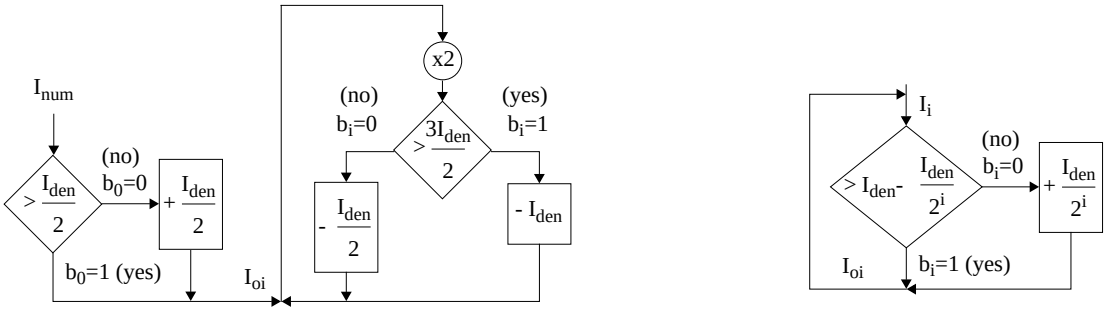


Fig 8: Schematic of the type_2 cell.



(a) (b)

Fig. 9: Flow chart of the algorithmic conversion method with algorithmic restriction: (a) Multiplying type [22]. (b) Dividing type.

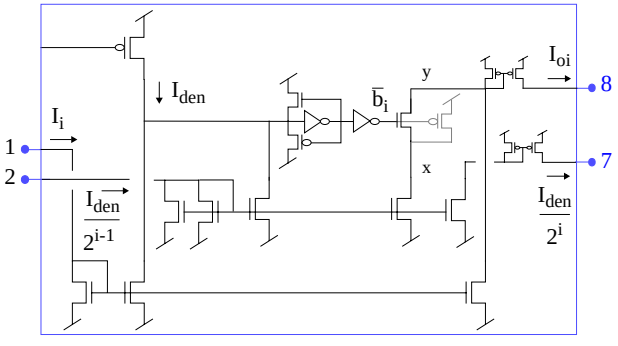


Fig 10: Schematic of the type_3 cell.

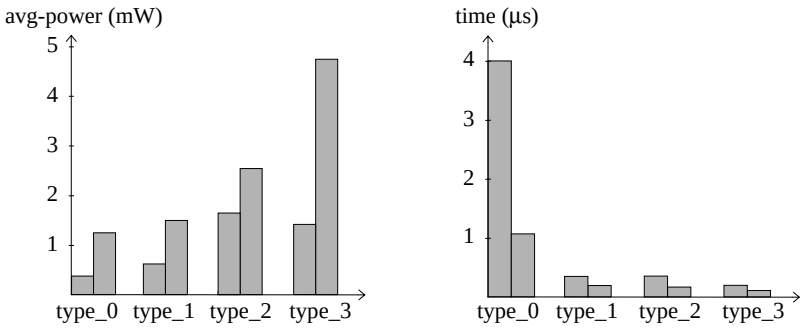


Fig. 11: Comparison of the different A/D bit cells considered.

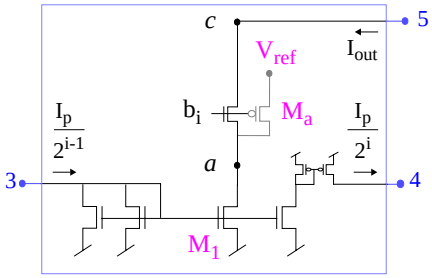


Fig. 12: Dividing algorithmic D/A bit cell.

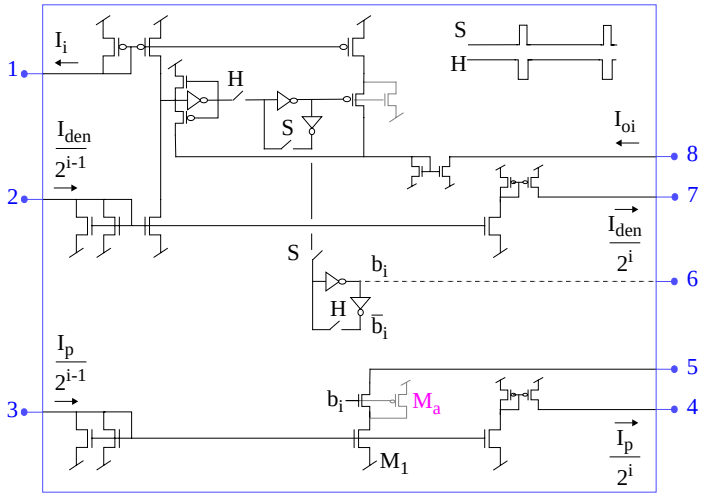


Fig. 13: Schematic of the selected A/D-D/A bit cell.

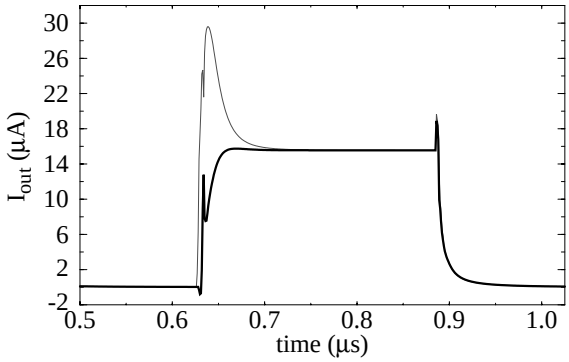


Fig. 14: Output current of a 5-bit D/A converter for a full-scale step when simple switches (grey line) and differential switches (black line) are employed.

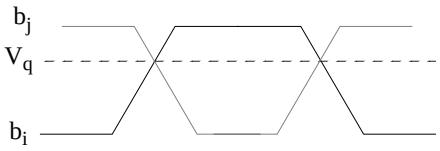


Fig. 15: Value of V_q to reduce nonsymmetrical switching of the D/A part.

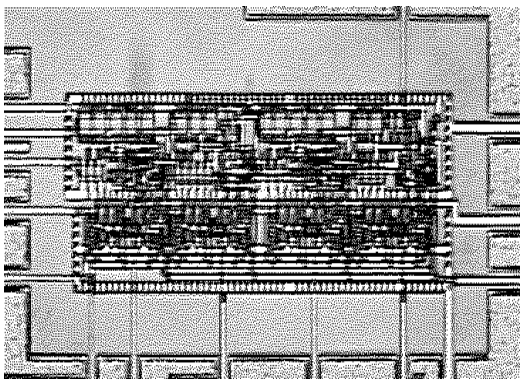


Fig. 16: Die photograph of a 5-bit multiplier/divider prototype.

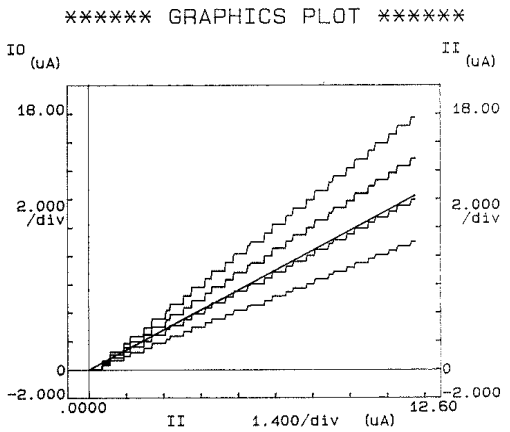


Fig. 17: Experimental results of the circuit operating as a multiplier.

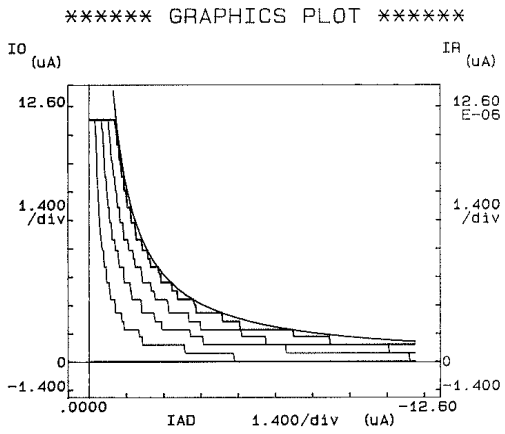
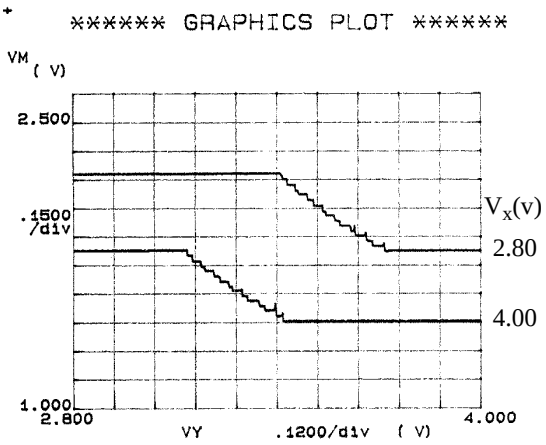
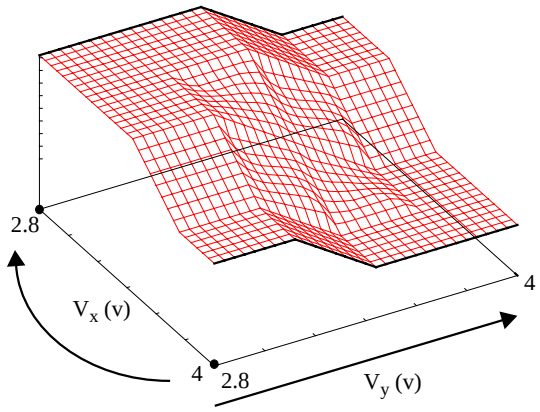


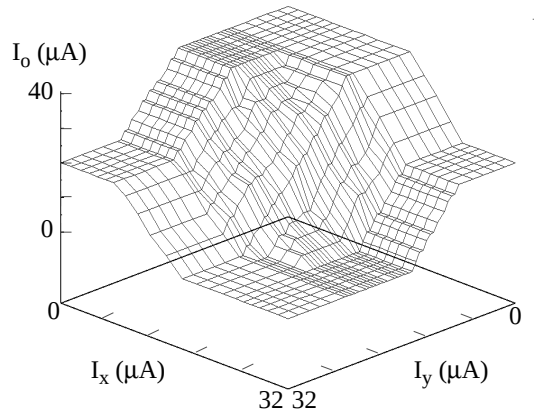
Fig. 18: Experimental results of the circuit operating as a divider.



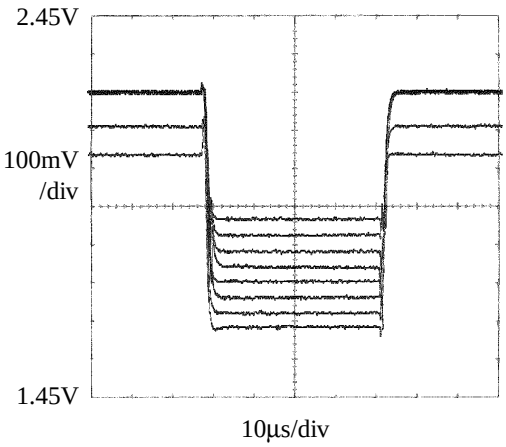
(a)



(b)



(c)



(d)

Fig. 19: Experimental results of the proposed circuit integrated within a fuzzy controller chip: (a) Analog control output provided by the divider corresponding to the sweeping depicted in the control surface of (b). (c) An experimentally obtained control surface. (d) Several step responses of the discrete analog control output.