CURRENT-MODE SINGLETON FUZZY CONTROLLER

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Abstract.-- This paper describes the realization of a fuzzy controller which implements the simplified inference mechanism. CMOS analog circuits where signals are represented as currents are employed. However, the whole system is externally communicated through voltages, thus enabling simple interface with conventional control circuitry.

I. Introduction

The efficient realization of microelectronic systems for fuzzy logic-based control applications requires a careful choice of both the inference mechanisms and the circuit structures which implement each controller block. Among the various inference methods, the singleton or simplified method is the most adequate for hardware implementation, as well as offering enough freedom in the choice of antecedents and consequents to ensure efficient control. Concerning circuit design methodologies, current-mode techniques are especially suited for direct implementation of the basic fuzzy operators. Working in current-mode, dynamic range problems can be handled with enough flexibility and a high-speed operation can be attained. Another important feature worth considering is the controller's compatibility with existing devices. The electrical variable (either voltage or current) that sensors (actuators) provide (accept) imposes a limitation to the design technique to be chosen. In this sense the proposed controller works with voltages at input and output to maintain compatibility with conventional voltage control circuits. Finally, controller programmability is essential since it limits the controller adaptability to solve different control problems without demanding complex adjustment procedures.

II. Controller architecture

The simplified inference mechanism can be considered as a particular case of those which are proposed in [1]. However, its implementation cost is much less as can be deduced from Fig. 1. The only building blocks are membership function generating circuits to describe the antecedents of the different rules, Min or Max operators to implement the connectives between these antecedents, and a rule pondering block (consisting of a current mirror and a divider circuit) to fulfill the expression:

$$y_o = \frac{\Sigma_i h_i c_i}{\Sigma_i h_i} \qquad (1)$$

In what follows the realization of each block in Fig. 1 is presented.

A. Membership Function Circuit (MFC)

The MFC blocks of Fig. 1 generate the membership functions of the different antecedents. The form and location of these functions are determined by a series of parameters, which allow choosing triangular or trapezoidal functions with different slopes. A voltage to current convertor provides the current I_{xi} proportional to the input voltage. The group formed by the transistors M_1, M_2 and the block cN acts as an absolute value operator. The block cP performs the bounded difference with I_{sat} and fixes the slope value of membership function. The output current of the MFC represents the complementary value of the membership level of the signal V_{in}.

Circuits based on this technique are more precise than other approximations reported in literature, since they do not depend on a combination of two or three functions [2-3]. They are also more efficient regarding area, power consumption, and operation speed. In addition, programmability is easily included [4].

B. Multi-input MAX Circuit

The multi-input MAX circuit which is shown in Fig. 1 performs a double function. On one hand, through I_{ref} it fixes the maximum membership degree. On the other, it implements a connective MIN between the rules antecedents, using the De Morgan's law:

$$\mathrm{Min}(I_i) = \overline{\mathrm{Max}}\,(\bar{I}_i) = I_{ref} - \mathrm{Max}(\bar{I}_i)$$

The circuit is a modification of the proposal in [5] and uses only 3n+1 transistors, yet achieving the same precision with less area and power consumption. As shown in Fig. 1, it consists of a combination of Wilson current mirrors which share a diode-connected transistor. The T_i transistors not only act as voltage followers but also conduct the current from a low impedance to a high impedance node, avoiding charge errors without additional cascode or regulated stages [6].

C. Divider

From a MOS analog circuit point of view, division has always been a costly operation in terms of time and area. Consequently, many of the reported fuzzy controllers impose the condition that the denominator in expression (1) assumes the value 1, or recur to the use of global normalization loops [5, 7] which limit the

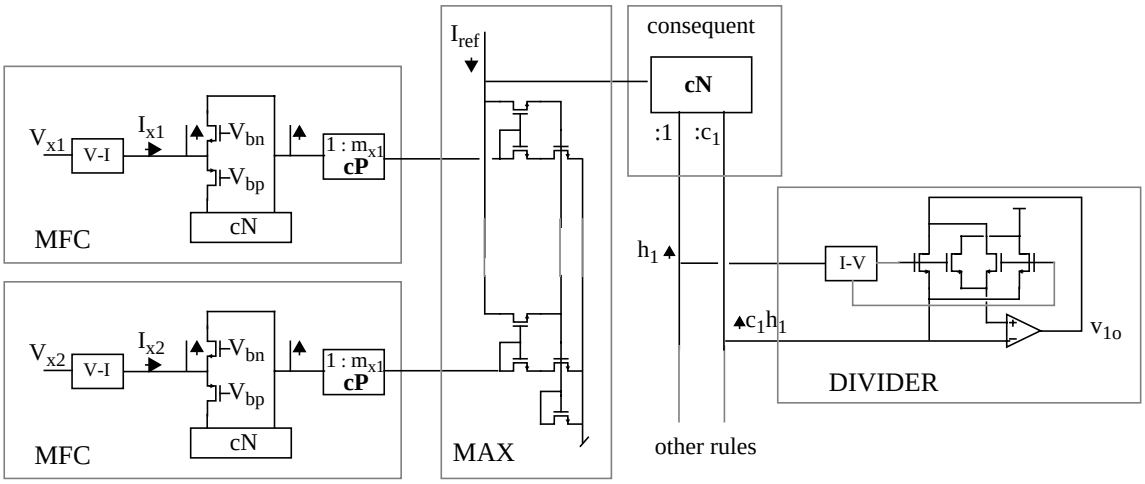

Fig. 1.- Schematic of the proposed controller.

inference speed of the controller and implement an approximation of expression (1).

The strategy followed here is the use of a simple continuous-time divider circuit which accepts currents as inputs and gives a voltage as output. For this, we follow a variable transresistance technique. This means the use of an element which allows a relation $V_o=I_n \cdot R$, with a resistance value R being controlled by a current I_d, so that $V_o=I_n \cdot V_a/I_d$.

The structure of this circuit is shown in Fig. 1. The four transistors which form the variable transresistance element operate in the ohmic region. This allows a larger dynamic range than that reached with square-law structures, and requires less power and area consumption (their geometries can be minimal). It also permits a high frequency operation, since this structure is self-compensated to intrinsic parasitic capacitances [9]. Finally, it is also more robust to transistor mismatching.

III. Results and Conclusions

The operation speed of the MFC and MIN/MAX blocks is restricted by the time invested in performing the bounded difference because this involves changing transistors from being OFF to conduct. Generally, these times are less than 300 ns. Regarding the divider block, its dynamics is governed by a dominant pole whose magnitude is proportional to the bandwidth of the amplifier and the value of I_d (which corresponds to Σh_i). For typical values, the response time of this block is also some hundred nanoseconds. Thus, the proposed controller can reach the range of MFLIPS.

The use of a simplified inference method and the adequate choice of the circuits which implement the different operators eases the hardware realization of fuzzy logic-based control systems. The main characteristics of the proposed architecture are reduced area costs, high operation capacity, simple interface with conventional control circuitry, and the possibility to include digital programming techniques.

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