Power Dissipation Associated to Internal Effect Transitions in Static CMOS Gates

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Abstract. Power modeling techniques have traditionally neglected the main part of the energy consumed in the internal nodes of static CMOS gates: the power dissipated by input transitions that do not produce output switching. In this work, we present an experimental set-up that shows that this power component may contribute up to 59% of the total power consumption of a gate in modern technologies. This fact makes very important to include it into any accurate power model.[1]

1 Introduction

Power consumption has become a key issue in UDSM technologies (0.25 μm and lower [1][2]) due to an increasing demand for portable battery-powered appliances and the durability and reliability problems associated with the high power densities, which need to be evacuated from the chip. From the point of view of VLSI circuits designers, it is necessary to know the sources of power dissipation in order to carry out designs which reduce this consumption as much as possible. In this way, logic level power estimation tools are a fast alternative to electrical level (SPICE-like) simulations because they can handle much bigger circuits and provide results in a fraction of the time by using event-driven techniques. At this level, the power consumed by a specific gate typically derives from the dynamic power caused by the switching activity. For each gate of a synchronous system controlled by a global clock, it can be expressed as [3]

$$P_{dyn} = C_L V_{DD}^2 f \alpha,$$

where P is the consumed power, C_L is the total capacitance, V_{DD} is the supply voltage, f is the clock frequency, and α is the switching activity (pulses per cycle).

Although dynamic power is the major contributor to power consumption, other mechanisms also contribute to it in a significant extent (Fig. 1): mainly

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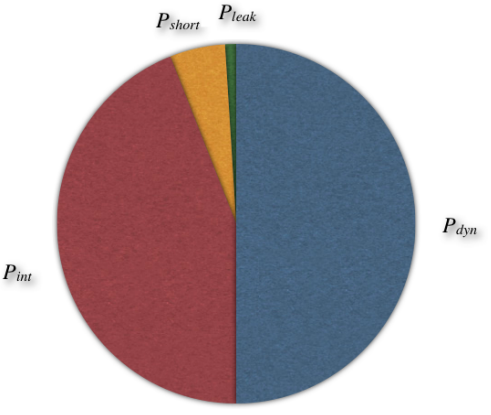

Fig. 1. Approximate contribution of the power sources to the total energy in a logic gate working at 50 MHz (0.18 μm technology)

the short-circuit power (P_{short}), leakage power (P_{leak}), and internal power (P_{int}) consumed by loading and unloading internal gate capacitances; even if the output of the gate is not switching (Fig. 2). On the one hand, short-circuit power can be modeled in a similar way to dynamic power by introducing an equivalent capacitance [4]. On the other hand, leakage power is no longer negligible in current technologies and is being extensively studied by the scientific community [5]. However, only partial progress has been made in modeling and estimating internal power consumption by proposing approximate statistical analyses [6] or generalist behavioral models for the internal states of the gate [7], and no quantitative analysis has yet been found to demonstrate the relevance of this internal power consumption with respect to the total power consumption of a gate.

Thus, the main objective of this work is to analyze the impact of the internal power associated to input transitions that do not produce output switching so, in order to differenciate the power types properly, we have assumed the next definitions (Table 1):

- Δ-power: power associated to dynamic outputs (switching outputs). We define such dissipation as the one produced in the gate when an input transition exist that generates an output transition (input transitions with external effect). Δ-power includes dynamic power, internal power and a minor short-circuit power component.
- Σ-power: power associated to static outputs (non-switching outputs). We define such dissipation as the one produced in the gate when an input transition exist that does not generate an output transition (input transitions with internal effect). Σ-power includes only internal power and a minor short-circuit power component.

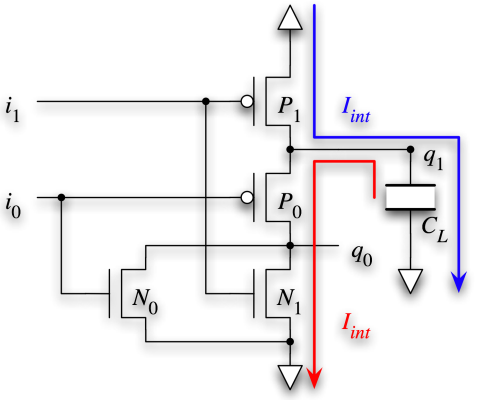

Fig. 2. Internal current flow in the NOR-2 gate: raising transition (flowing from V_{DD} to q_1) and falling transition (flowing from q_1 to GND) at node q_1

Table 1. Power sources associated to each type of consumption

Source	Δ-power	Σ-power
P_{dyn}	×	
P_{int}	×	×
P_{short}	×	×
P_{leak}		

Table 2. Amount of possible input transitions in each gate

Gate	Possible transitions	External effect transitions (Δ)	Internal effect transitions (Σ)
NOR-2/NAND-2	12	6	6
NOR-3/NAND-3	56	14	42
NOR-4/NAND-4	240	30	210

We must denote that, although both types of dissipation (Σ and Δ) include internal power, the main part of such power corresponds to the Σ component in most gates because there are much more internal effect transitions than external effect ones (Table 2).

In previous works [8][9] we have just carried out such analysis on cells from the libraries provided by the foundry. However, the electric models of those cells are very inaccurate because they do not include the corresponding parasitic elements. For this work, we have designed a set of custom cells at layout level (Fig. 3) in order to take into account those parasitic elements in our analysis. The design has been realized according to the λ-rules provided by MOSIS [10] and covers both NOR and NAND gates of up to three inputs in UMC 0.25 μm and UMC 0.18 μm technologies. Thus, the purpose of this work is to perform a quantitative analysis of the internal power consumption of static CMOS gates in

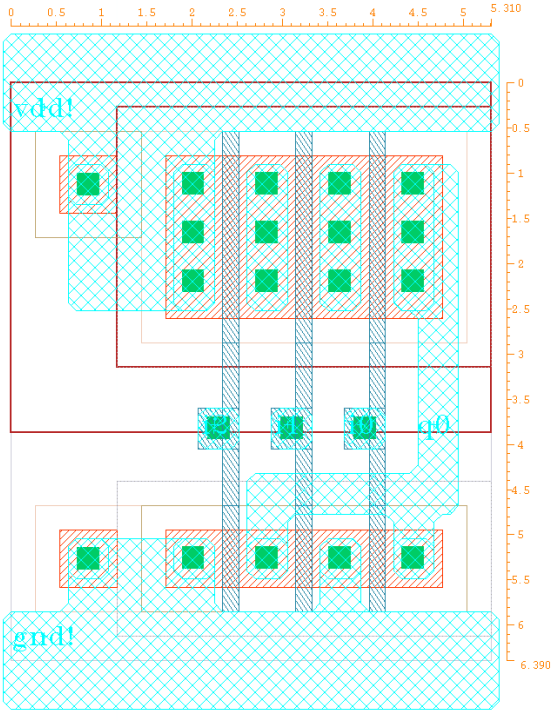

Fig. 3. Layout of the NOR-3 gate (UMC 0.18 μm)

a comprehensive way and evaluate the contribution of the Σ-power component (traditionally neglected by logic simulators) to the total dissipation.

The rest of the paper is organized as follows: in section 2 the experimental set-up used is described, in section 3 the simulation results are presented, and in section 4 we include a short discussion about the data obtained.

2 Experimental Design

The objective of the design was to measure the energy consumed in a gate for all possible input changes. Two CMOS technologies were analyzed: UMC 0.25 μm and UMC 0.18 μm. The circuit used in the study is the one shown in Fig. 4.

This structure allows us to analyze the gate under test (marked in gray) in conditions similar to those of a real circuit since it places the gate in a realistic input/output environment. Both NOR and NAND set-ups were analyzed (2-input and 3-input configurations). Each gate was equipped with its own power supply in order to measure the exact consumption taking place in it. For each case, the geometry of the transistors was chosen specifically to obtain the same ratio that the one used in the foundry library. Finally, the test circuit was powered at the nominal supply voltage for each technology: 2.5 V for 0.25 μm and 1.8 V for 0.18 μm.

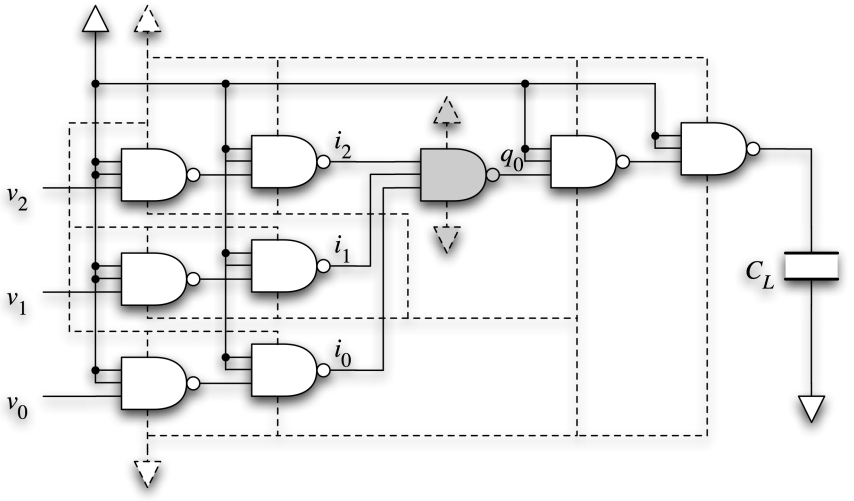

Fig. 4. Test circuit for the NAND-3 gate. The are two different power supplies (dashed): one for the device under test (shaded in gray) and another one for the rest of the gates.

This circuit was simulated at electrical level using HSPICE v2001.2. For each combination of technology and gate type, a simulation was performed with an input pattern producing all the possible input transitions. Thus, for each of these transitions we measured the power dissipated in the gate under test, distinguishing between Δ-power (produced by external effect transitions) and Σ-power (produced by internal effect transitions). These simulations allowed us to measure the last one with respect to the total consumption for each type of gate.

3 Results

Firstly, Fig. 5 and Fig. 6 show the study of the NAND-2 gate. This figure is just illustrative: actually, all possible transitions, number of inputs, and technologies for both NOR and NAND gates have been analyzed. Secondly, Table 3 and Table 4 show the energy consumed by the NOR-2 and NAND-2 gates respectively under different conditions of input transitions for each technology. Finally, Table 5 presents the total power consumption measured for each case separating Σ-power and Δ-power.

Σ-power is calculated as the sum of the energy dissipated when the output does not change and, similarly, Δ-power is calculated as the sum of the energy dissipated when the output changes. As all possible input transitions were covered, the results in this table are a measure of the energy dissipated by the gates when they are driven by random inputs.

In addition, we also calculated the percentage of the total consumption represented by Σ-power in each case (Fig. 7).

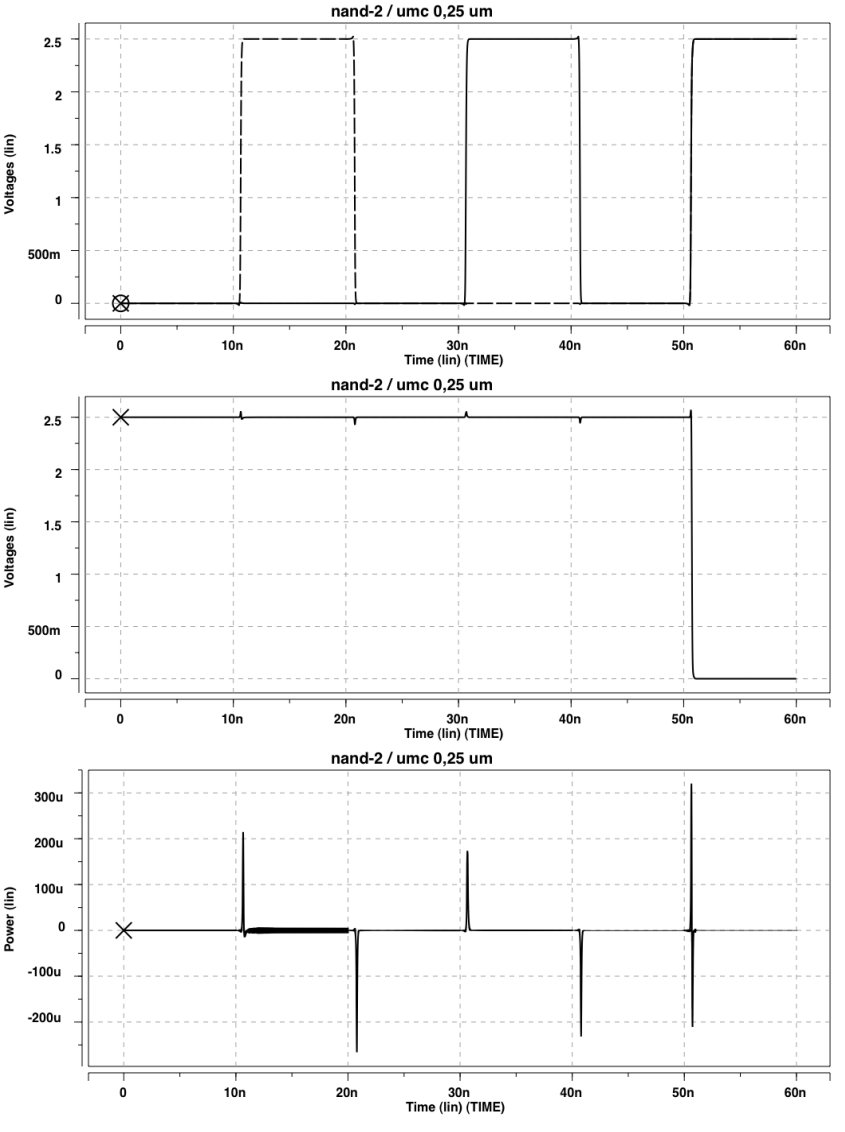

Fig. 5. Simulation detail of the NAND-2 gate (UMC 0.25 μm): input signals (top), output signal (middle), and power dissipation (bottom)

4 Discussion

Firstly, there is an enormous similarity in the power curves resulting from the simulations between the two technologies (Fig. 5 and Fig. 6). The power peaks that have been measured are very similar and differ only in their size (although they maintain a similar proportion among them). Note that the positive peaks of

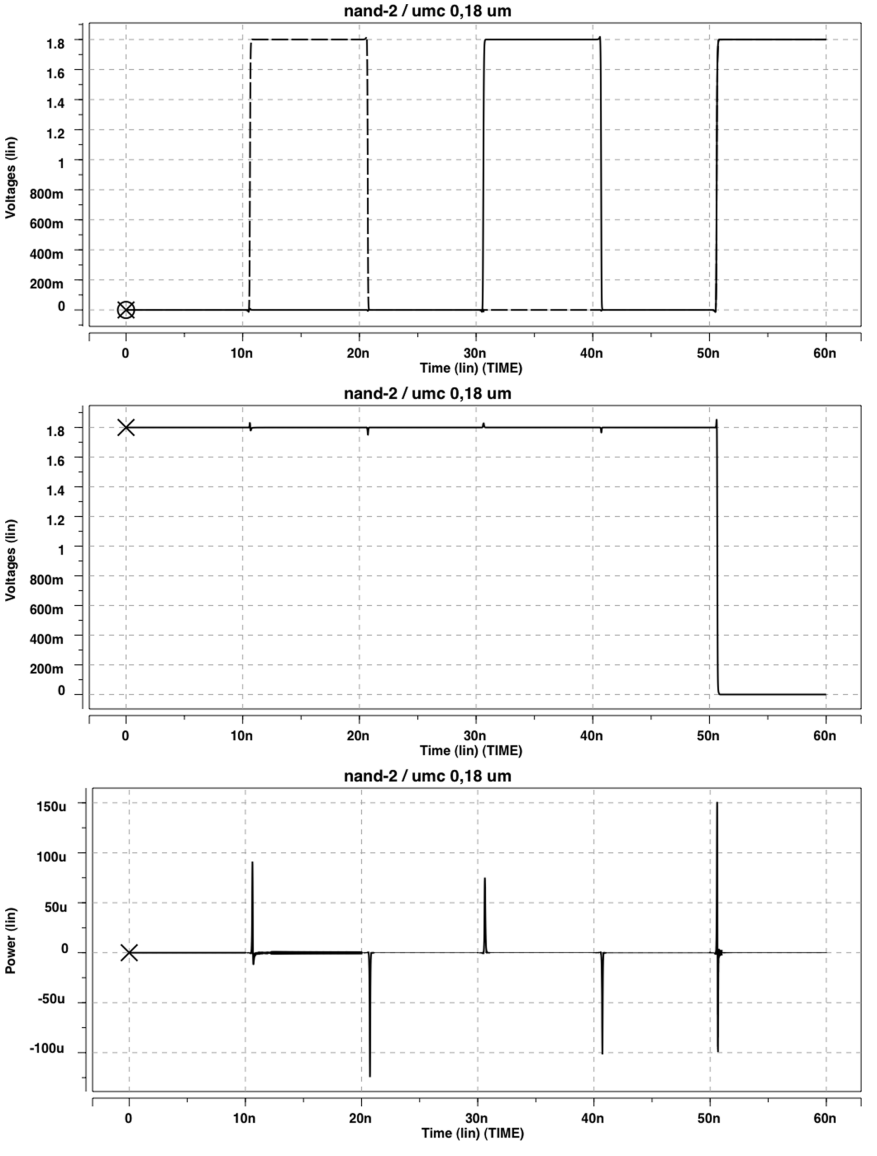

Fig. 6. Simulation detail of the NAND-2 gate (UMC 0.18 μm): input signals (top), output signal (middle), and power dissipation (bottom)

intensity (representing return to the power supply) are produced by the effect of the couple capacitances existing between the gate inputs and the output node.

Secondly, we must emphasize the enormous importance of Σ-power: according to the data, it can represent up to 58-59% of the total consumption (in the case of the NAND-3 gate) and it is always higher than 12% (Fig. 7). In addition, the

Table 3. Consumption measured in the NOR-2 gate

Input transition	Type	UMC 0,25 μm (fJ)	UMC 0,18 μm (fJ)
$00 \rightarrow 01$	Δ	-9.12	-2.30
$00 \rightarrow 10$	Δ	-32.38	-9.84
$00 \rightarrow 11$	Δ	9.84	4.46
$01 \rightarrow 00$	Δ	-113.00	-41.16
$01 \rightarrow 10$	Σ	-2.23	-0.10
$01 \rightarrow 11$	Σ	31.11	9.79
$10 \rightarrow 00$	Δ	-136.90	-49.24
$10 \rightarrow 01$	Σ	-33.63	-11.06
$10 \rightarrow 11$	Σ	6.63	2.55
$11 \rightarrow 00$	Δ	-145.80	-52.36
$11 \rightarrow 01$	Σ	-30.57	-10.61
$11 \rightarrow 10$	Σ	-32.12	-10.35

Table 4. Consumption measured in the NAND-2 gate

Input transition	Type	UMC 0,25 μm (fJ)	UMC 0,18 μm (fJ)
$00 \rightarrow 01$	Σ	14.52	3.57
$00 \rightarrow 10$	Σ	20.52	6.86
$00 \rightarrow 11$	Δ	3.76	2.25
$01 \rightarrow 00$	Σ	-25.46	-8.89
$01 \rightarrow 10$	Σ	-88.88	-31.68
$01 \rightarrow 11$	Δ	-11.43	-2.79
$10 \rightarrow 00$	Σ	-22.54	-7.38
$10 \rightarrow 01$	Σ	-114.10	-41.47
$10 \rightarrow 11$	Δ	-11.00	-3.16
$11 \rightarrow 00$	Δ	-124.90	-43.82
$11 \rightarrow 01$	Δ	-120.50	-44.04
$11 \rightarrow 10$	Δ	-100.30	-36.17

Σ-power percentage remains very consistent for both technologies yielding very similar values for each of the gates.

Thirdly, it can be seen that internal consumption becomes more important in gates with more inputs. This is due to two main reasons: (a) a greater number of transistors produce a greater amount of parasitic elements in the gate (Fig. 2) and (b) a greater number of inputs produces a higher proportion of transitions with internal effect (Table 2). Furthermore, it can be observed that the relevance of such effect varies greatly between the NOR and NAND gates. In both types of gates we have measured similar values for the parasitic capacitances, and their total consumptions are of the same order too (Table 5). However, as both gates implement different logic functions, the internal effect transitions are not the

Table 5. Global consumption results

Gate	Type	UMC 0,25 μm (fJ)	UMC 0,18 μm (fJ)
NOR-2	Δ	−427.37	−150.43
NOR-2	Σ	−60.81	−19.78
NOR-3	Δ	−1160.00	−402.44
NOR-3	Σ	−362.76	−119.62
NAND-2	Δ	−364.37	−127.72
NAND-2	Σ	−215.94	−79.00
NAND-3	Δ	−981.80	−348.03
NAND-3	Σ	−1339.79	−507.23

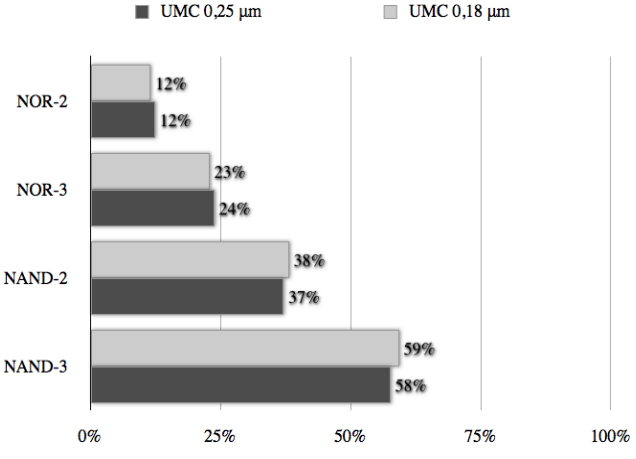

Fig. 7. Σ-power percentage with respect to the total one

same for each type of gate (Table 3 and Table 4) which makes this consumption to be more divided in the NAND case and to loose relevance, with respect to the external one, in the NOR case.

5 Conclusion

This study has shown the enormous contribution that internal consumption represents in the total energy consumed in a specific logic gate. For that, we have analyzed, in a comprehensive way, a total of four gates (corresponding to two different technologies) and we can conclude that the internal consumption associated to static outputs (named Σ-power in this paper) has shown as a very important effect (surpassing in some cases the one associated to dynamic outputs). However, such effect has been traditionally neglected by logic simulators so we consider mandatory to include it in any accurate power model.

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