Logic-Level Fast Current Simulation for Digital CMOS Circuits*

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Abstract. Nowadays, verification of digital integrated circuit has been focused more and more from the timing and area field to current and power estimations. The main problem with this kind of verification is on the lack of precision of current estimations when working at higher levels (logic, RT, architectural levels). To solve this problem it is not only necessary to use good current models for switching activity but, also, it is necessary to calculate this switching activity with high accuracy. In this paper we present an alternative to estimate current consumption using logic-level simulation. To do that, we use a simple but accurate enough current model to calculate the current consumption for each signal transition, and a delay model that obtains high accuracy when it is used to measure the switching activity (the Degradation Delay Model -DDM-). In the paper we present the current model for CMOS inverter, the characterization process and the model implementation in the logic simulator HALOTIS that includes the DDM. Results show a high accuracy in the estimation of current curves when compared to HSPICE, and a potentially large improvement over conventional approaches.

1 Introduction

Verification of digital integrated circuits is a key point during the design process. Verification tasks take place at the different design level: layout, logic-level, architectural and system levels. Due to the increasing scale of integration developed during the last two decades, more and more interest is devoted to verification at higher levels, including system and software levels [1–4].

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On the other hand, verification interest has been moving more and more from the timing and area field to current and power estimations, the main motivations being switching noise and energy consumption calculations. The first one is an important factor limiting the accuracy of the analog part in mixed-signal circuits [5], while the second is becoming a major design condition due to the increasing difficulties to dissipate the power generated by high performance processors and the need to operate low-power devices on batteries [6].

In this scenario, electrical simulation and verification is mainly limited to the optimization of basic building blocks. Filling the gap between electrical and system verification is logic-level simulation. While whole system simulation is not feasible at the logic level any more, major system parts, up to several millions of transistors, are still manageable at the logic-level. That makes logic-level simulation the more accurate alternative available in many practical cases when the rough system-level estimations are not useful.

Facing the new challenges cited above, EDA (Electronic Design Automation) vendors have been incorporating current and power estimation facilities to their logic-level simulation tools (PRIMEPOWER [7], XPOWER [8], POWERTOOL [9]). Current/power estimations at the logic level are generally obtained in a two-phase procedure: first, logic-level simulation takes place and switching activity at every node is computed. Then, power consumed at every node is computed by using charge-based power models. On the other hand, current curves may be generated during logic-level simulation by using current models in a event-driven basis [10, 11].

Since these approaches are basically correct, switching activity estimations at the logic level has been traditionally largely overestimated [12, 13], mainly due to the fact that conventional behavioural models are not able to accurately handle the propagation of glitches and input collisions [14, 15]. This way, well implanted commercial tools may easily overestimate switching activity (then current and power) from 30% to 100% [12, 16].

On the contrary, it has been shown in [17] that it is possible to develop behavioural models that catch the dynamic nature of the switching process at the logic level (e.g. Degradation Delay Model -DDM- [17]). The immediate consequence of this is a natural ability to accurately handling the generation, propagation and filtering of glitches.

The objective of this paper is to show that using this kind of dynamic behavioural modelling, the accuracy of logic-level estimations of the supplied current is largely improved. To do that, current estimation capabilities have been incorporated to a previously developed logic-level simulation tool named HALOTIS [18]. Since the tool already incorporates the DDM, switching activity is accurately handled. Current estimation is computed during the simulation process by applying a current model to every signal transition in the internal nodes of the circuit, generating a set of partial current curves. These current curves are summed up after simulation to generate the global current profile of the circuit.

Although this work is still in its early stages, results are very promising if we consider that, in our opinion, there is still plenty room to improve the process,

specially the current modelling. In the next section, we introduce the current model that is incorporated in the simulator in order to obtain current curves. Model characterization and validation is done in section 3. Implementation issues are discussed in section 4, while preliminary results are presented in section 5. Finally, we will summarize the main conclusions.

2 Current Model

Global current calculation is obtained by summing up the current driven by each circuit cell individually from the power supply. For a given cell we assume that the current only circulates during the logic switching of the cell's output. Fig. 1 shows the currents involved in a CMOS inverter structure when a raising output transition takes place. The main currents taken from V_{cc} during the inverter's switching process are I_{cl} and I_{SC}. I_{cl} is the current that charges the inverter output node, and I_{SC} is the short-circuit current which goes directly from V_{cc} to GND while the NMOS part is still conducting. When we deal with raising output transitions, the total current driven from the power supply is the sum of I_{cl} and I_{SC}. For falling output transitions, the capacity C_L is discharged, and the only component taken from the power supply is I_{SC}.

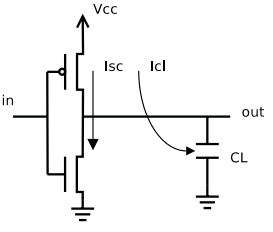


Fig. 1. CMOS Inverter currents during logic switching

The actual current curve in the gate, as obtained with HSPICE [19] electrical simulator, is shown in Fig. 2-b. Our model proposes to fit the actual current curve by a triangle-shaped, two-pieces linear curve. The triangle approximation can be seen in Fig. 2-a.

This approach is similar to that proposed by other authors [10, 11], but using a simpler characterization method. The triangular shape is defined by three points: the triangle starting point instant (T_b), the current maximum value and the instant when it takes place (T_{max},I_{max}), and the instant time where the triangle ends (T_e).

These points can be approximated as follows: T_b is the instant when the input transition starts and the point T_e is the instant when the output transition ends, which are both known. To calculate I_{max} and T_{max} we use the model proposed in [20]. In that work, the authors obtain the following equations:

$$I_{max} = \sqrt{\frac{K_p \times W_p \times V_{DD}^2 (C_L + C_{SC})}{\tau_{in}}} \tag{1}$$

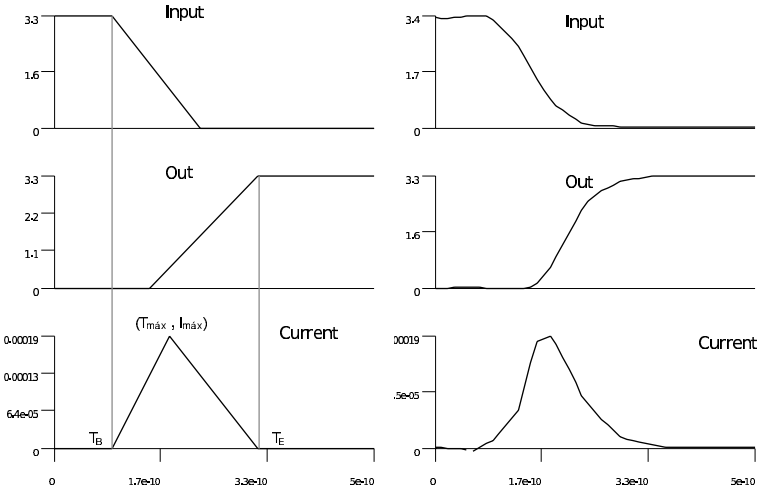


Fig. 2. Inverter switching curves. a) Triangle current model. b) HSPICE simulation

$$T_{max} = \frac{(C_L + C_{SC})V_{DD}}{I_{max}} \tag{2}$$

where K_p and W_p are respectively the transconductance factor and width of the PMOS transistor, V_{DD} is the supply voltage, C_{SC} is the short-circuit capacitance as defined in [20] and τ_{in} is the transition time of the input.

On the other hand, for falling output transitions we only have to consider the short-circuit current I_{SC}, so that:

$$I_{max} = \sqrt{\frac{K_n \times W_n \times V_{DD}^2 \times C_{SC}}{\tau_{in}}} \tag{3}$$

In this case, T_{max} is the time when input transition crosses the inverter input threshold.

The proposed model allows the calculation of an approximated, triangle-shaped current curve for every output transition of a cell, only based on cell parameters and timing data provided during logic simulation.

3 Current Model Validation and Characterization

To validate the model proposed in the previous section, we have simulated the behavior of CMOS inverter built using a $0.35\mu m$ technology. This simulation has been carried out with HSPICE. The objective is to check the I_{max} dependence with respect to τ_{in} and C_L. For this reason, we will express the equation1 as follow:

$$I_{max}^2 = \frac{V_{DD}^2}{\tau_{in}}(QC_L + R) \tag{4}$$

In this equation we can see the linear dependence of I^2_{max} with C_L and $1/\tau_{in}$, where Q and R are gate-level model parameters that hides the internals of the cell. This dependence has been checked by plotting I^2_{max} values versus C_L for different τ_{in}, and also, I^2_{max} values versus τ_{in} for different C_L. Fig. 3 shows the circuit configuration used to obtain simulation data. The first and second inverter in the chain are used to achieve realistic input transition waveforms at the input of *inv3*, which is the cell under study. The interest of working with realistic transitions in *inv3* is in the high variation of I_{max} values observed when linear (artificial) input transitions are used. On realistic transitions, τ_{in} is measured taking the 30% and 70% reference points with respect to the full supply rail.

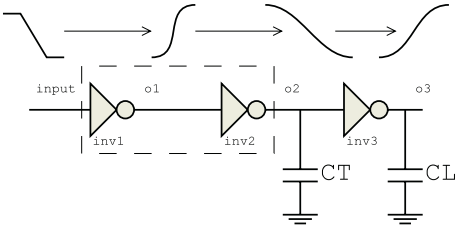


Fig. 3. Inverter characterization circuit

The simulations have been carried out for a range of typical values of τ_{in} and C_L. τ_{in} is altered in a realistic way by modifying C_T in the circuit. The design space explored includes fast and slow input transitions and light and heavy loads. To get this, C_T and C_L values take the inverter input capacity (C_{in}) as a reference, where C_{in} is:

$$C_{in} = (W_n + W_p) \times L \times C_{ox} \tag{5}$$

where W_n and W_p are the NMOS and PMOS widths respectively, L is the MOS length and C_{ox} is the oxide capacitance by unit area.

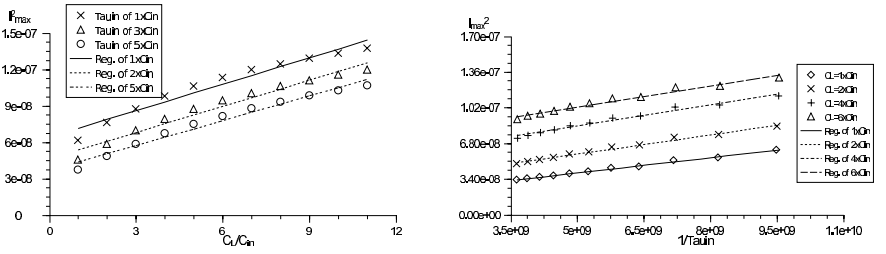
In Fig. 4-a we show the curves representing I^2_{max} versus C_L/C_{in} for different τ_{in} and its linear regressions. The Fig. 4-b shows I^2_{max} the curves I^2_{max} versus τ_{in} for different C_L/C_{in} and its linear regressions.

Based on these linear regressions it is possible to extract values for Q and R parameters of equation 4. Q and R values are mostly independent of loading and input transition time conditions. Moderate input ramps and typical loading conditions are used to compute Q and R values. As an example, inverter parameters for a raising output under conditions given by $C_T = 2 \times C_{in}$ and $C_L = 2 \times C_{in}$ gives:

$$Q = (4.67 \pm 0.28) \times 10^{-5} A/V^2, R = (5.94 \pm 0.46) \times 10^{-19} A^2 s/V^2 \tag{6}$$

4 Model Implementation in HALOTIS

HALOTIS [18] is a logic-level simulator that is being developed in our research group. It's main feature is the inclusion of the Degradation Delay Model (DDM).



(a) (b)

Fig. 4. (a) I^2_{max} vs. C_L for different τ_{in}. **(b)** I^2_{max} vs. τ_{in} for different C_L

HALOTIS, through the use of the DDM, has demonstrated a drastic accuracy improvement over conventional simulation tools thanks to the novel and precise treatment of glitch generation and propagation. HALOTIS also implements a Conventional Delay Model (CDM), that it is a delay model without the degradation effect. This facility makes it possible to easily evaluate how the DDM improves simulation results. It is also interesting to note that accounting for the degradation effect introduces a negligible overhead in the logic simulation process. Currently, HALOTIS is able to read digital circuit netlists in VERILOG [21] format and read patterns in MACHTA [22] format. It is designed in a modular way to enable for new functionality to be easily added as research on models and algorithm improves.

The current model described in section 2 has been included in the simulation engine through a new source code module that implements equations (2) and (4) corresponding to T_{max} and I_{max} respectively. The rest of the necessary parameters to compute the current waveform associated to each transition (T_e and T_b in Fig. 2-a) are already available during the simulation process. Additionally, the set of parameters for each gate now also includes Q and R parameters measured using the characterization process described in section 3.

When a new output transition is generated during simulation process, the new module processes this transition and calculates the points of the triangle that defines the current waveform associated with that output transition. All triangles are stored in a data type which is processed after simulation to generate the general current profile of the circuits, i.e. the current generated by the power supply as a function of time. The data available can also be used to locate hot spots or noisy nodes, although these applications have not been explored yet.

5 Simulation Results

The effect of summing up individual current components for every signal transition is better appreciated in multi-level digital circuits, where transitions and current waveforms overlap for a period of time. Also, glitch conditions, evolution and eventual filtering will more likely take place as logic depth increases. Thus, a simple but adequate circuit to demonstrate the possibilities of the proposed

model and its combination with the degradation effect is a chain of gates like that depicted in Fig. 5. The quality of the results is measured by comparing to circuit-level simulation using HSPICE.

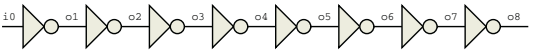


Fig. 5. Inverter chain

Two types of input patterns are simulated. The first example is intended to show the current model accuracy in the absence of degradation effect. The second pattern will make degradation effect to take place and will rise up the benefits of using a dynamic behavioural model like the DDM.

The first case is a wide pulse applied to the first inverter in the chain. This pulse is fully propagated through the inverter chain and no degradation effect takes place since the input pulse is wide enough to avoid that. The voltage waveforms obtained at selected internal nodes of the chain with HSPICE and HALOTIS are shown in Fig. 6-a and Fig. 6-b respectively. Logic-level simulation with HALOTIS matches HSPICE results quite well, and it can be seen how HALOTIS takes input transition times into account and reflects that in the plot. We note here that logic simulation results using the Degradation Delay Model (DDM) or a Conventional Delay Model (CDM) without degradation are the same since degradation effect does not take place for these stimuli.

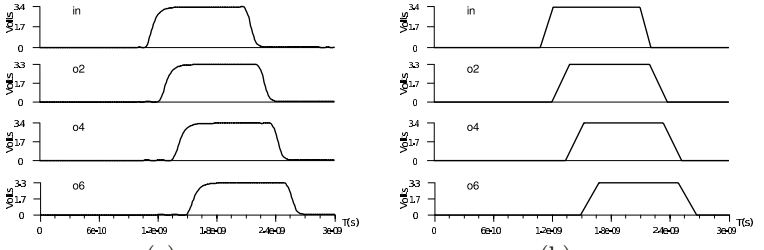


Fig. 6. Single input pulse voltage waveforms. (a) HSPICE (b) HALOTIS

As it has already be explained, current components for every transition is computed during simulation. The complete current waveform obtained by summing up these components is plotted in Fig. 7, besides the current curve generated by HSPICE. It can be easily observed how the current curve generated by HALOTIS quite well matches HSPICE results. Specially, current peaks are quite accurately reproduced.

The second example simulates a pulse train applied at the input of the chain. In this case, the pulses are narrow enough to degrade from logic level to logic. Some of the pulses will be filtered at some point in the chain. Simulated voltage

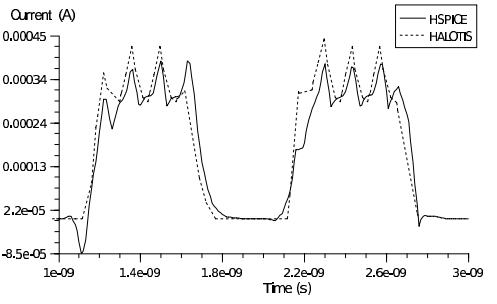


Fig. 7. Single input pulse current waveform

waveforms at even nodes using HSPICE are depicted in Fig. 8, while logic simulation considering the degradation effect (DDM) is in Fig. 9. It can be seen that the initial pulse train is degraded through the chain and some pulses are filtered until a single wide pulse is propagated to the output of the chain. This effect is reproduced both by HSPICE and HALOTIS when using the DDM. However, a conventional delay model (CDM) would propagate the full pulse train unaltered

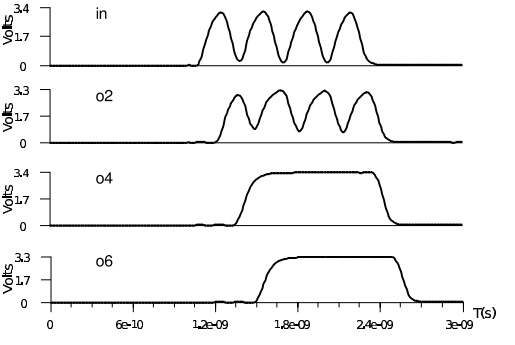


Fig. 8. Pulse train HSPICE voltage waveforms

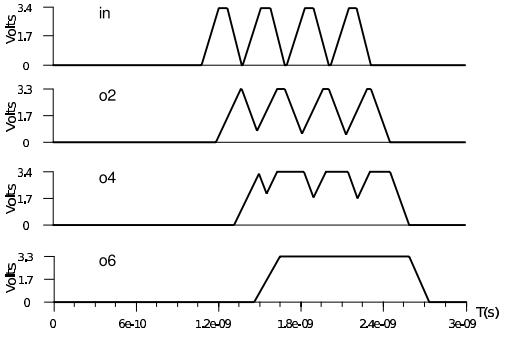


Fig. 9. Pulse train HALOTIS voltage waveforms with degradation effect (DDM)

(Fig. 10). This behaviour and its implication on the switching activity has been reported in detail in [16, 18]. This time, the current waveforms calculated using the DDM and the CDM differ since the CDM will consider additional transitions and current componets that are actually filtered. Fig 11 compares HSPICE and HALOTIS results using both DDM and CDM models. Like in the previous example, simulation using the DDM gives results that are similar to HSPICE results. In particular, current peaks are again very accurately determined.

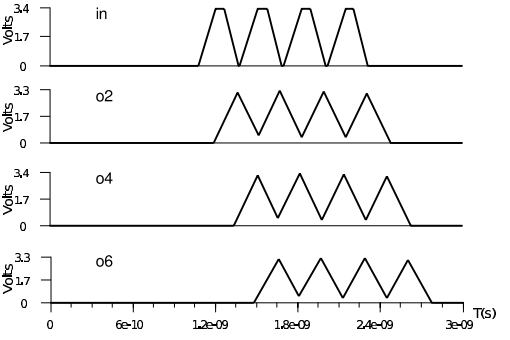


Fig. 10. Pulse train HALOTIS voltage waveforms without degradation effect (CDM)

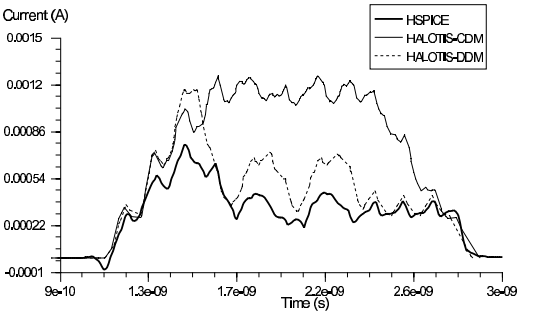


Fig. 11. Pulse train current waveforms. HSPICE, DDM and CDM comparison

Simulation without degradation effect (CDM) gives much worse results, even though the core behavioural model is the same that the one used by the DDM.

6 Conclusions

In this contribution a simple current model for logic transitions that can be used in logic-level simulators to obtain current estimations has been presented. The proposed model has been implemented in a experimental logic-level simulation tool that combines the current equations with the so-called Degradation Delay Model to obtain accurate current waveforms at the logic level when compared

to electrical simulators like HSPICE. It has been demonstrated that, despite its simplicity, the proposed model provides with accurate results while keeping the speed up of logic-level over electrical simulation (2 to 3 orders of magnitude). It has also been shown that including the degradation effect in logic simulation is a key point in order to achieve some level of accuracy, since conventional delay models will largely overestimate the switching activity, thus current, yielding to useless results despite the accuracy of the internal current model.

The combination of the DDM and logic-level current models appears as a good alternative to current estimations (and derived applications) at the logic level.

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