Efficient and Fast Current Curve Estimation of CMOS Digital Circuits at the Logic Level*

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Abstract. This contribution presents a method to obtain current estimations at the logic level. This method uses a simple current model and a current curve generation algorithm that is implemented as an attached module to a logic simulator under development called HALOTIS. The implementation is aimed at efficiency and overall estimations, making it suitable to switching noise evaluation and current peaks localisation. Simulation results and comparison to HSPICE confirm the usefulness and efficiency of the approach.

1 Introduction

Switching noise is becoming a major problem in current mixed signal circuits. The noise induced through substrate and power lines coupling by the digital part reduces the performance of the analog part which is built in the same substrate, as is the case of the resolution of A/D converters [1].

From the analog part, design and layout techniques have been employed to reduce the impact of this kind of noise, like guard rings. From the digital part, some work has been devoted to design low-switching-noise digital CMOS circuits [2,3,4] and to develop techniques to evaluate how noisy digital circuits are [5,6]. At the circuit level, supply and substrate currents are taken as a measure of the noise generation [5,6] while at the logic level, it is the switching activity density which has been taken as an adequate noise generation profile [5].

We believe that just the switching activity information is of limited use, since it does not distinguishes between light or heavy loaded gates, making it difficult to spot the most important parts of the noise estimation, like the current peaks.

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We think however that it is possible to obtain good switching noise profiles at the logic level, provided we use accurate simulation techniques and adequate models.

In this paper we propose a fast algorithm to evaluate the supply current spent by a digital circuit. At this time the motivation is its use as a method to estimate the switching noise generated by the circuit, so we use a very simple current model targeted at efficiency and peak current evaluation. Nevertheless, it is also the basis for other applications like accurate instant and average power estimations at the logic level. The algorithm is integrated as part of the HALOTIS logic timing simulator [7], so it inherits benefits of the event-driven technique (fast simulation) and of the accurate delay models it implements. Regarding the delay model, HALOTIS uses the *Degradation Delay Model* (DDM) which provides with a very accurate and efficient way to handle the generation and propagation of *glitches* [8,9,10,11]. This property is of special interest in this work, since these glitches contributes an important part of the switching activity and hence the average current [12].

In the next section, the current model is presented. Sect. 3 describes the implementation of the algorithm in HALOTIS logic simulator. Sect. 4 is devoted to simulations results, and we will finish by summarising the main conclusions.

2 Transition Based Simple Current Model

In this section we present a simple model to evaluate the current spent in a signal transition. The model is suitable to be implemented in the already mentioned HALOTIS logic timing simulator, or in any other logic timing tool that uses variable slope linear ramps to represent digital signal transitions.

Given a linear signal transition in node N, we evaluate the average current I_0 provided by the source as

$$I_0 = \frac{V_2 - V_1}{t_2 - t_1} C_L \tag{1}$$

where V_1 and V_2 are the initial and final transition voltages, t_1 and t_2 the initial and final transition times and C_L is the total capacitance of the node.

The simplest model to evaluate the current produced by a transition is just considering a constant current I_0 that lasts during the transition evolution, as shown in Fig. 1. It is important to note that V_1 and V_2 may be any voltage value between the supply rails, since the simulation engine is able to handle non-fully switched transitions.

It will be shown later in this paper that, despite its simplicity, the presented model, when combined with the appropriate delay model, is useful to to obtain good current profiles, specially when focusing on the determination of current peaks and the overall current waveform.

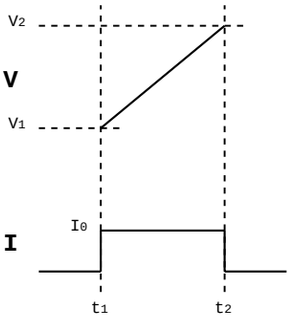

Fig. 1. Simple transition based current model

3 Model Implementation

The current model is implemented in HALOTIS as a separate module that processes node signal transitions on the fly as they are eliminated from the main simulation queue. The process, depicted in Fig. 2, takes place as follows: when processed transitions get out the simulation engine, they enter the *current pulse calculator*, which discards falling transitions, since only current driven by the power supply is of interest, while rising transitions are processed using the model described in the previous section, and a current pulse is obtained. Current pulses are then passed to the *cumulative graph* module which adds each new pulse to the current curve, which is this way dynamically generated. Current curve points can then be directed to the display or printer using conventional plotting software, both on the fly at simulations time or after the simulation process ends.

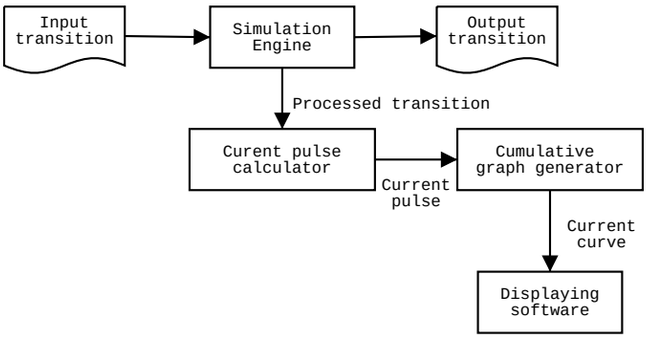

Fig. 2. Current generation algorithm implementation.

4 Results

To validate the model and algorithm, we have simulated two circuits using HSPICE [13] as a reference and HALOTIS. As we stated above, the use of glitch aware delay models is of great importance when evaluating the current. In order to show this point, HALOTIS simulations are made using the Delay Degradation Model (DDM), which accurately handles the propagation of glitches, and a *Conventional Delay Model* (CDM) which treats the propagation and elimination of glitches by using an *inertial delay* [14], like most standard logic simulators do.

The first example consists of a chain of regular inverters that propagates a fast train of pulses (Fig. 3). It is used as a simple test to check how the current calculation algorithm and the DDM works. Fig. 4 shows the voltages at even nodes of the chain using the three kinds of simulation. We can see that the use of the DDM is able to take account of the signal *degradation*, leading to very similar results when compared to HSPICE, but at the logic level. On the other hand, the CDM is not able to render this effect, producing an inaccurate result both in the timing and switching activity aspects.

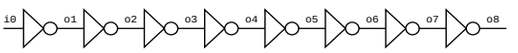

Fig. 3. Inverter chain.

The current figures obtained in the same three simulation cases are depicted in Fig. 5. Since only a few signal transitions are simulated during a short period of time, signal quantisation is quite evident in logic simulation results, in part due to the simplicity of the current model we are using. Nevertheless, DDM results quite well reflects the current evolution by reproducing the main parts of HSPICE's current curve: initial current rising, high current region followed by a middle current region, including a spurious current sink, and a final low current part. On the contrary, CDM results shows an average behaviour during the whole simulation, apart from the initial current rising and final current decreasing. This behaviour is a direct consequence of the overestimated switching activity obtained with conventional models, as was shown in Fig. 4.c.

A much more interesting result is obtained from the simulation of a rather complex circuits, like a 4x4 bit multiplier. In this case, many signal transitions take place at almost the same time showing up clearly its impact in the production of current peaks.

Fig. 6 and Fig. 7 show the results of two sequences simulated with HSPICE, HALOTIS-DDM and HALOTIS-CDM. From these curves we can see that the current generation algorithm implemented in HALOTIS is able to render the current profile of the circuit, to a point that it is possible to distinguish where current peaks are located, its approximate amplitude and how long the switching activity of the circuit lasts after an input pattern is applied. In both cases, not considering the degradation effect (CDM results) yields to an overestimation of

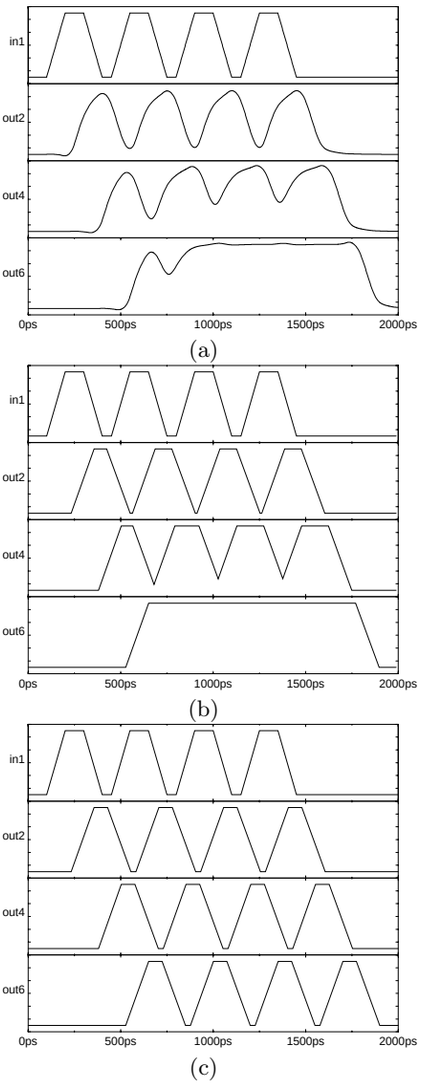

Fig. 4. Inverter chain voltage results: a) HSPICE, b) HALOTIS-DDM, c) HALOTIS-CDM.

the average current as a direct consequence of the overestimation of the switching activity already pointed out. This effect is specially obvious in the last pattern of the first sequence (Fig. 6) and in the fist and third patterns of the second sequence (Fig. 7).

As we noted above, current curve evaluations using the proposed method are done entirely at the logic level, thus important CPU time improvements

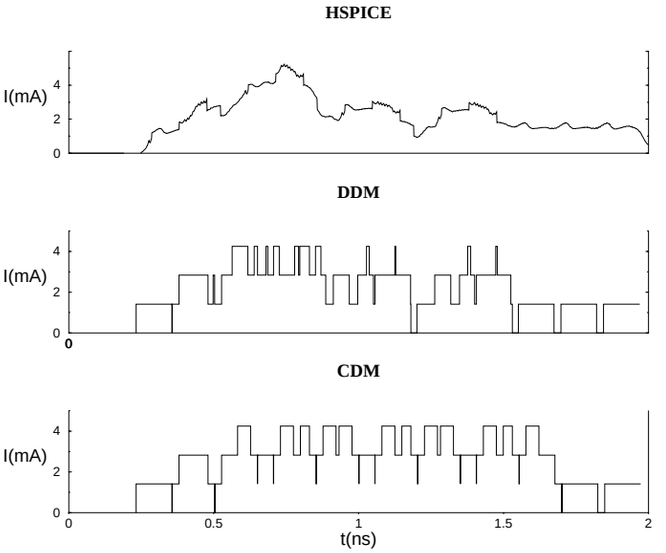

Fig. 5. Inverter chain current results using HSPICE, HALOTIS-DDM and HALOTIS-CDM.

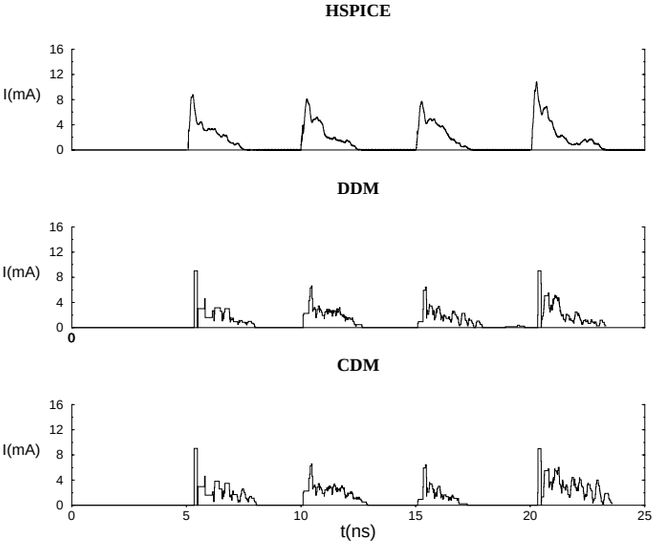

Fig. 6. Simulation results of sequence 0x0, 7x7, 5xA, Ex6 and FxF.

over HSPICE simulations are obtained. In Table 1 we show the CPU times spent in each type of simulation, as well as the speed up of logic simulations

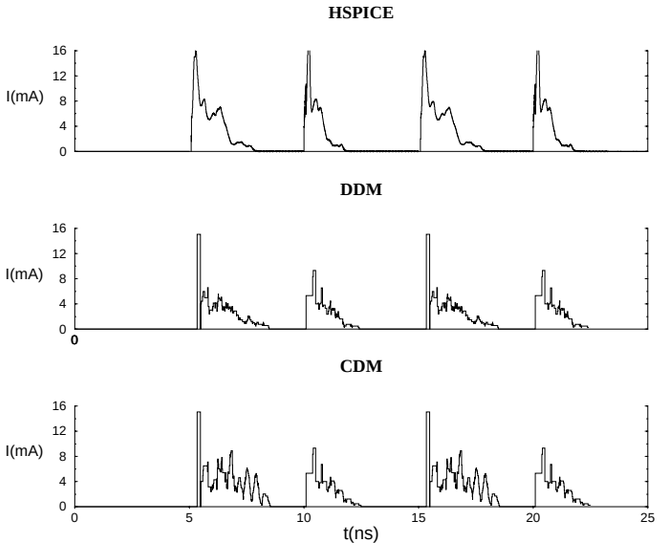

Fig. 7. Simulation results of sequence 0x0, FxF, 0x0, FxF, 0x0

over HSPICE and the overhead of applying the current calculation algorithm in the logic simulator, when compared to the logic simulation without current calculation. The current calculation overhead in HSPICE is negligible. As it is clear from the table, logic simulation speed up over HSPICE is in the order of 400 times, as expected. Although the DDM use slightly more complex formulas than the CDM, simulation times for the DDM are usually smaller than for the CDM, since the last one makes the simulator to process more transitions, derived from an overestimated switching activity. Regarding the overhead introduced by the current calculation algorithm, it is around 20% when the DDM is used and around 30% when the CDM is used. Both of them are quite affordable from the logic simulation perspective, since it is a matter of seconds in most cases.

Table 1. Multiplier simulation CPU times in seconds (speed up over HSPICE in parenthesis) and current calculation overhead in the logic simulation.

Pattern	HSPICE	DDM	CDM	DDM overhead	CDM overhead
0x0, 7x7, ...	280	0.58(483)	0.64(437)	23%	33%
0x0, FxF, ...	281	0.70(401)	0.80(351)	21%	33%

5 Conclusions

It has been presented a simple and fast algorithm to estimate the supply current at the logic level, with application to measure digital switching noise generation. Simulation results show that the algorithm is able to accurately locate current peaks and activity regions with improved speed over HSPICE within 2-3 orders of magnitude. It has been shown that the use of the degradation delay model plays an important role, since this model provides with the method to take into account only "real" transitions, and filter non-existent glitches propagated by conventional logic simulation tools. The current curve calculation module adds little (around 25%) overhead to the logic simulation process.

We believe that the proposed method is the basis of valuable tool for the digital designer willing to get fast current/noise estimations at the logic level in the early stages of the design.

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