Influence of Clocking Strategies on the Design of Low Switching-Noise Digital and Mixed-Signal VLSI Circuits

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Abstract. This communication shows the influence of clocking schemes on the digital switching noise generation. It will be shown how the choice of a suited clocking scheme for the digital part reduces the switching noise, thus alleviating the problematic associated to limitations of performances in mixed-signal Analog/Digital Integrated Circuits. Simulation data of a pipelined XOR chain using both a single-phase and a two-phase clocking schemes, as well as of two n-bit counters with different clocking styles lead, as conclusions, to recommend multiple clock-phase and asynchronous styles for reducing switching noise.

1 Introduction

Integration of digital and analog mixed-signal integrated circuits has taken significant advantages in the implementation of advanced electronic systems. However, the integration of large-scale digital and high-speed analog circuits in the same monolithic IC implies interactions, referred to as cross talk, between both parts, and analog signal degradation problems. In these mixed-signal circuits, the switching noise created by the digital circuits passes to the analog circuits, limiting their performances -resolution of A/D converters, jitter in PLLs, etc-, and making very difficult the realization of high resolution analog circuits on the same substrate with complex digital circuitry. Such noise can be easily measured by monitoring the peak value of dynamic current provided by the supply source (Fig 1), that is proportional to the carrier injection [1].

The use of noise reduction techniques alleviates the influence of switching noise [2]: to separate as much as possible the digital and the analog part; to use different supply and ground sources for analog and digital circuitry; to considerate the substrate coupling and reducing it with substrate biasing and using guard-rings, etc. All these methods are related to layout and analog design, but do not include digital design methodology.

Recently, some low-switching-noise digital CMOS families have been reported: CSL [3], FSCL [1] and CBL [4]. These current-mode structures work with supply cur-

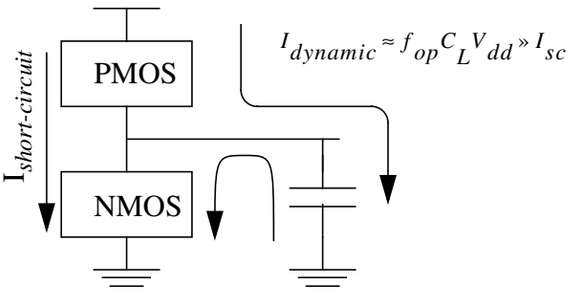

Fig. 1. Dynamic (dominant) and short-circuit current in CMOS.

rent almost constant, thus reducing variations in supply current and, hence, switching noise. However, static power consumption is the main penalty of such structures, making them unsuited for low-power applications. The use of these current-mode families is recommended only in risky-noise generation areas, while in other non-critical areas, logic should be implemented with more conventional techniques. However, the use of these current-mode logics is highly complicated, since these gates are very complex and difficult to design and test, they need current-mode to CMOS-conventional interfaces, and show static power consumption. Furthermore, additional reduction in switching noise implies higher static power consumption [5].

This communication explores additional ways of reducing switching noise from the digital domain, studying the influence of the clocking style in the digital part on the generation of switching noise, when using more conventional low-cost CMOS digital implementations.

This communication is divided as follows. Section 2 shows the theoretical influence of the clocking scheme in the switching-noise. Section 3 presents a comparison between a single-phase and a two-phase scheme as a case of study. Section 4 presents a comparison between synchronous and asynchronous counters, as example of study. Section 5 shows some simulation results. And finally, Section 6 presents the conclusions.

2 Switching Noise and Timing Schemes

The switching noise, also referred as dI/dt noise, increases when many circuits or blocks evaluate simultaneously, causing power supply fluctuations [6]. The use of an specific clock strategy when designing the digital part in a mixed-signal IC brings serious consequences relating to such noise generation. Since the timing scheme indicates the way of gates switch, and the supply current is the sum of contributions due to switching gates, as the number of synchronized gates switching increases, the peak supply current will be also increased. This is the case of Simultaneous Switching Noise (SSN) in buffer design [7] [8].

The use of a single-phase clock scheme (fig. 2a) forces that most of the transitions in the system take place within a relatively small interval around (during and after) the clock active edge. By using two clock phases (fig. 2b), or a double-edge clock, switching in combinational logic, as well as in clock generator logic and flip-flops, reduces the number of gates or subcircuits that simultaneously switch, reducing the peak current of supply source. Although the logic blocks can effectively switch at any time between consecutive active edges of the clocks considered (depending on the propagation delay of combinational logic), the activity i.e., the number of nodes that switch their logic value, will be statistically greater in the proximity of active clock edges (dashed area in the activity bars in fig. 2). If we consider that both implementations (fig. 2a and fig. 2b) are identical in the sense that the same logic is used and the same nodes have the same capacitive load associated and hence, the same average current is consumed (see equation in fig. 1), the maximum current level will be given in the single-phase clock scheme (fig. 2a), since all the flip-flops and logic blocks switch (almost) simultaneously. With this reasoning, the most suited synchronous solutions for low-noise generation use more than one clock phase, although introducing clock-skew problems, decreasing the operation reliability. In such case, a trade-off between low-noise and reliability should be found.

Self-timed [9] design (fig. 2c) is an elegant cost effective means to control noise in a predictable manner. By substituting the global clock by locally-generated clocks (clock1, clock2 and clock3) indicating the validity of data to be processed for the next logic block, switching of gates are unsynchronized, making that supply currents of different self-clocked blocks do not overlap, hence reducing the magnitude of the noise components. In this way, a self-timed circuit can be conceived like a k (large) clock-phase system, being the operation distributed in continuous time slots rather than in discrete time instants.

3 A Case of Study: Comparison between a Single-Phase and a Two-Phase Clock Schemes

In order to verify the reasoning of Section 2, we are going to measure the switching noise in a simple system using two different clocking schemes. The system in a XOR gate array of XOR gate with pipeline at a gate level. The flip-flops used in the pipeline stage have been designed by using a TSPC approach [10]. The reason of this choice is due to the more conventional master-slave flip-flops works in a equivalent two-phase configuration, so the comparison would not be fair, as we could confirm without any appreciable difference. Also TSPC are widely used in modern VLSI digital design.

In fig. 3 we show both circuits at a transistor level. In the case of single-phase clock scheme, we can distinguish two kinds of TSPC elements: TSPC NMOS, operating in the rising edge of the clock, and PMOS, operating in the falling edge. While, in the case of two-phase clock scheme, we can only need TSPC NMOS flip-flops. Due to the use of the NMOS and PMOS TSPC, the output waveforms will be the same in both cases, so the operation form will be identical in both case without decreasing the clock frequency for the two-phase clocking scheme.

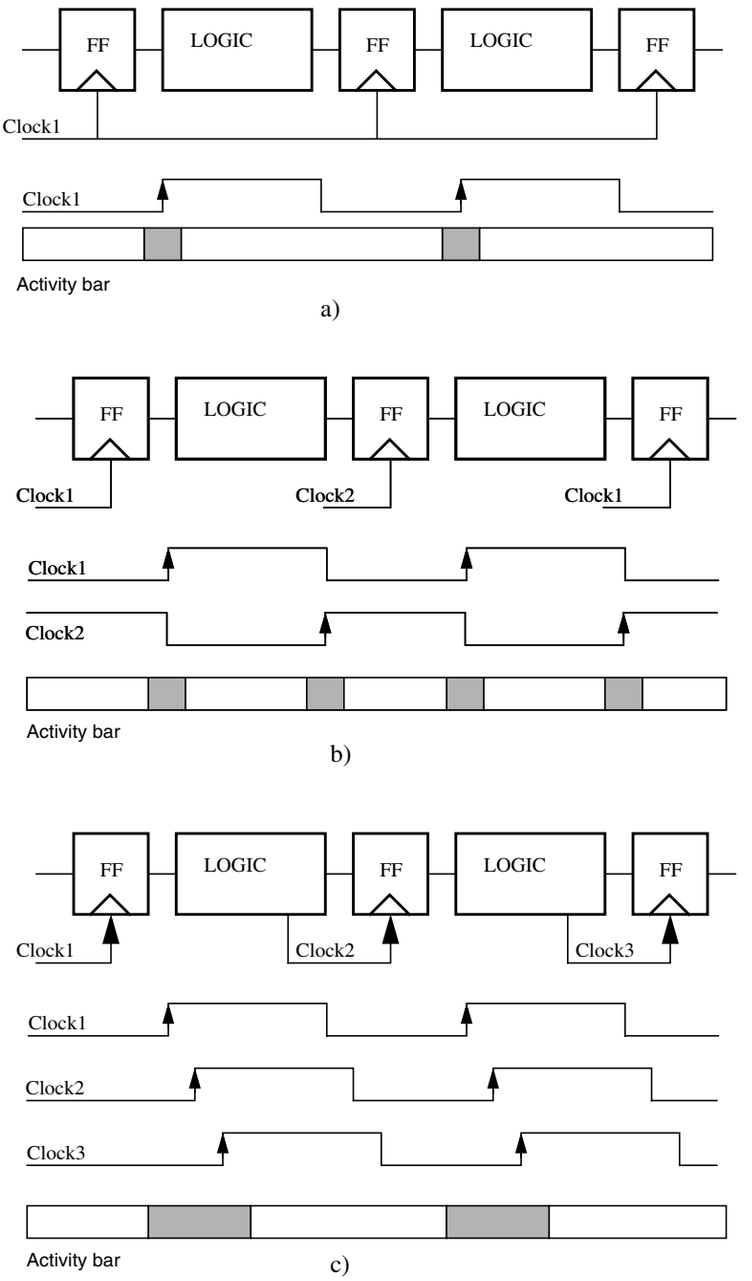

Fig. 2. Different clocking styles for a pipelined logic structure: a) Single-phase, b) Two phases, c) Self-timed. The dashed areas in the Activity bar indicate the maximum switching density.

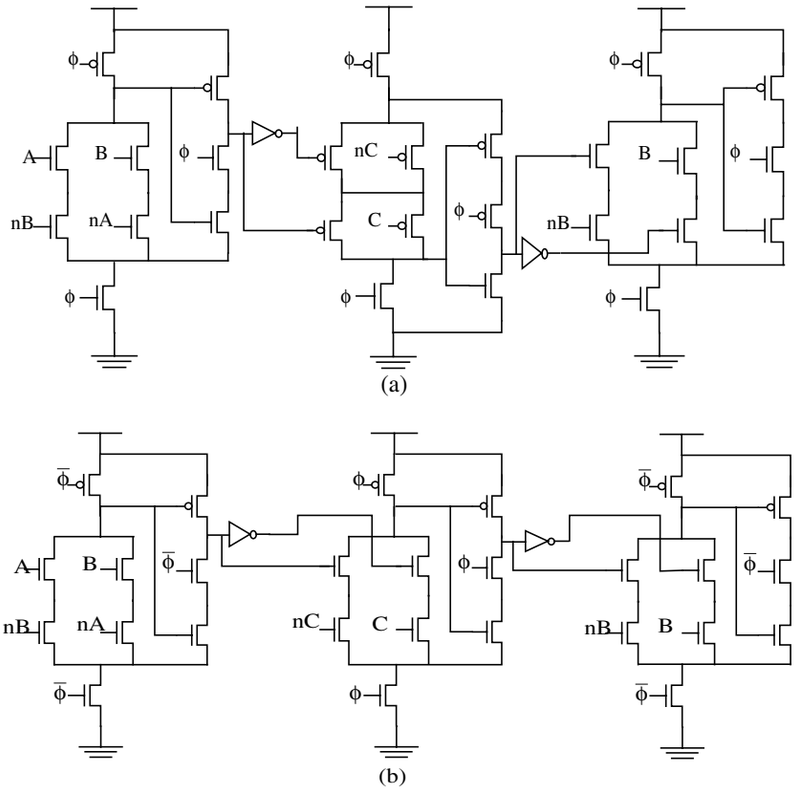

Fig. 3. Schemes at a transistor level corresponding to the array of XOR gates with a) a single-phase and b) a two-phase clock schemes.

4 Another Case of Study: Comparison between the Synchronou and the Asynchronous "Ripple" Counter

Following with the demonstration of the reasoning of Section 2, let us consider a n-bit counter as a generic example to show our claim of decreasing spikes in supply current, with synchronous and self-timed clocking strategies. The events counter is a sequential machine of wide use and interest in most digital and mixed-signal applications, specially for frequency division applications. The counter device counts events in the C signal, increasing or decreasing the count state. Two simple implementations of a 4-bit increasing counter are shown in fig. 4. Both modular implementations use T(oggle) flip-flops as elementary memory units. The synchronous implementation (fig. 4a) uses the C sig-

nal as clock of all the flip-flops, while in the ripple implementation (fig. 4b) the clock signal of each flip-flop is the output of the previous flip-flop in the counter. As it is clear, these are good examples of the different clocking strategies shown in the previous section.

In fig. 5, an HSPICE simulation of a detailed state transition (from 1111 to 0000) is shown for both counters. It can be easily seen how the transitions in Q_0, Q_1, Q_2 and Q_3 in the synchronous case are almost simultaneous, while in the asynchronous case, the transition in Q_i provokes the transition in Q_{i+1}, after the propagation delay of the flip-flop. The average supply current is approximately the same, but more "concentrated" in the synchronous case, meaning a higher maximum value and, hence, provoking greater switching noise.

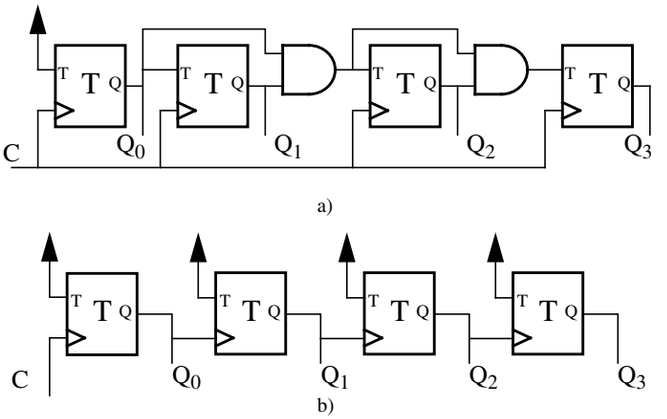

Fig. 4. 4-bit counter: a) synchronous, b) asynchronous "ripple".

5 Design and Simulation Results [11]

Simulations have been performed on a 0.7 μm standard technology. The results corresponding to the comparison between synchronous clock schemes are shown in table 1, while the results for the counters are shown in table 2.

Table 1. Simulation results of the synchronous clocking schemes for the pipelined XOR array. F=50 MHz.

	Transistors	Power (mW) Vdd=5v/3.3v	Iaverage (μA) Vdd=5v/3.3v	Ipeak (μA) Vdd=5v/3.3v
One-Phase	31	0.36 / 0.11	68.3 / 34.7	4200 / 1720
Two-Phase	31	0.36 / 0.08	68.8 / 26.4	2250 / 850

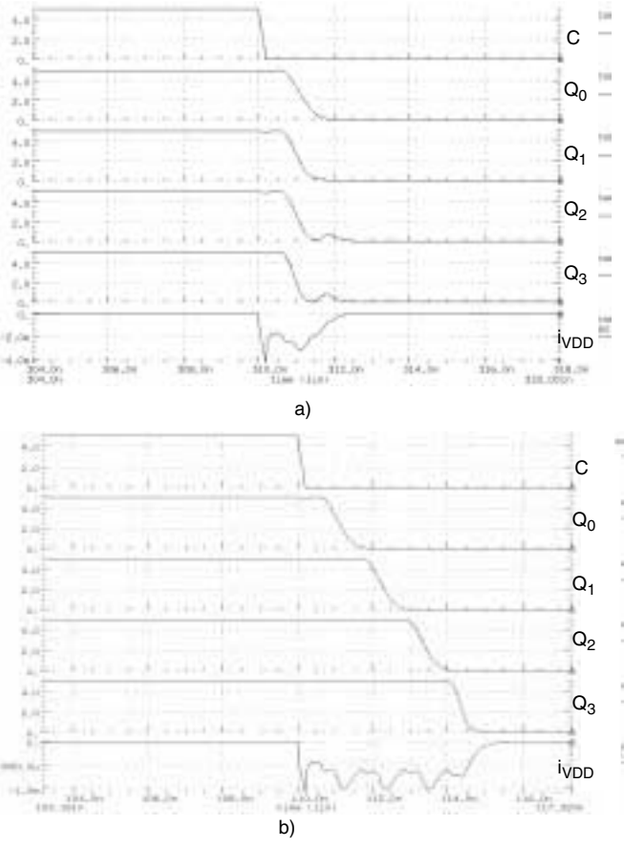

Fig. 5. Detailed transition from count state 1111 to 0000 in a) synchronous, b) asynchronous 4-bit counter.

Table 2. Simulation results for counters. F=50MHz. PDP: Power-Delay-Product.

	Transistors	PDP (pJ) Vdd=5v	Iaverage (µA) Vdd=5v/3.3v	Ipeak (µA) Vdd=5v/3.3v
4-bit synch.	116	0.17	170 / 100	4552 / 2410
4-bit asynch.	104	0.51	130 / 70	1274/ 666
8-bit synch.	244	0.24	221 / 125	9033 / 4809
8-bit asynch.	208	1.11	184 / 81.3	1421 / 708

In the case of average power consumption, we can see that there is almost any difference between both synchronous clocking schemes, being approximately the value corresponding to one-phase scheme a 105% of the corresponding to the two-phase one. In the case of counters, differences between synchronous and asynchronous are below 10%. These results can be seen in the fig. 6.

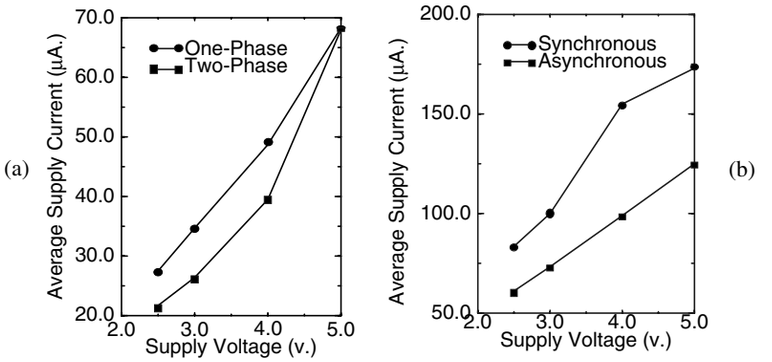

Fig. 6. Average supply current vs. supply voltage for a) the one-phase and two-phase clocking scheme and b) the 4-bit counter.

Concerning supply current peak, we can see that the peak corresponding to the single-phase is basically twice than the corresponding to the two-phase one, meaning that the two-phase scheme presents a better switching-noise behavior. In the case of counters, it is much more higher the peak value in supply current for the synchronous case (up to 4 times, depending on the Vdd value). These results can be seen in fig. 7.

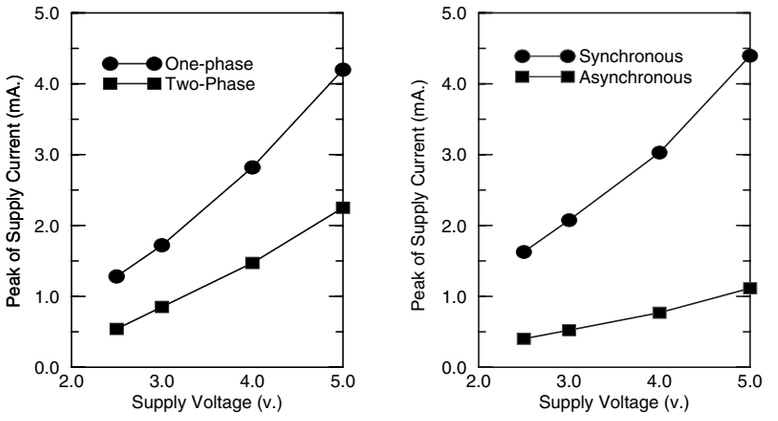

Fig. 7. Peak of supply current vs. supply voltage to (a) the one-phase and two-phase clocking scheme and (b) a 4-bit counter.

A clear measurement of the dependence of clocking schemes on peaks of supply currents is shown in fig. 8, where timing waveforms and spectra of supply current are

depicted. They show how the peak values in time of the synchronous are greater, and the harmonics placed in frequencies multiple of the fundamental clock frequency (50 MHz) are considerably higher (from 4 to 11 db).

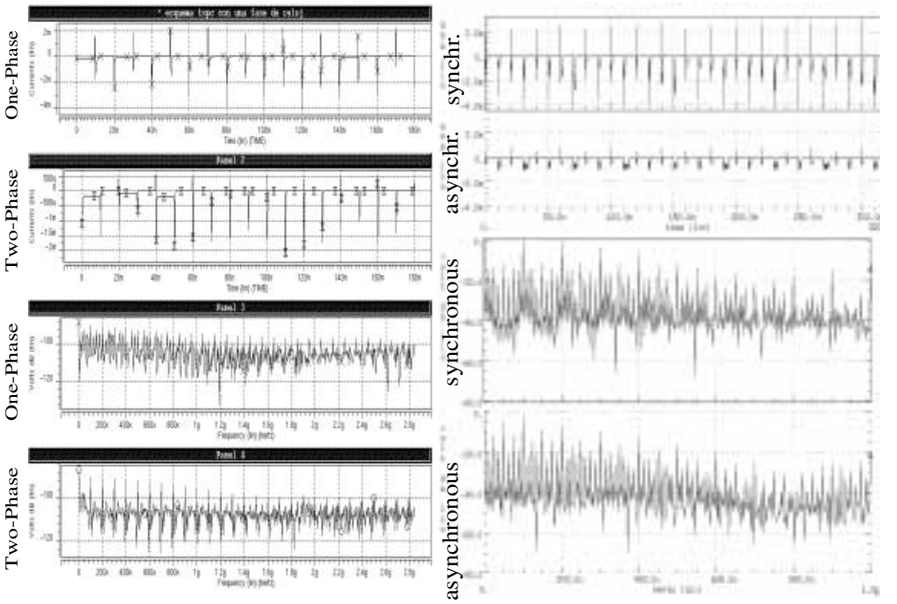

Fig. 8. Timing waveforms and spectra of supply current for a) synchronous clocking schemes and b) the 4-bit counter, Vdd = 5v, f = 50MHz.

As counters are useful circuits, we have measured as additional parameters in this demonstrator the power-delay product. Also, we have performed a comparison with the number of stages, what is equivalent to find out the influence of the transistor-count. These results are summarized as follows:

- The power-delay product, corresponding to counters (fig. 9), is better for the synchronous approach, meaning that better performances can be found, but at the cost of extra hardware, one two-input nand gate per bit.

- The maximum supply current (fig. 10) increases linearly with the counter length for the synchronous approach, while the value for the asynchronous one is almost constant. As the number of stages increases, there are more flip-flops switching simultaneously, increasing the switching noise.

6 Conclusions

This communication has shown the influence of the clocking strategy on the switching-noise generation. It will be shown how the choice of a suited clocking scheme for the digital part, alleviates the problematic associated to switching noise in mixed-signal

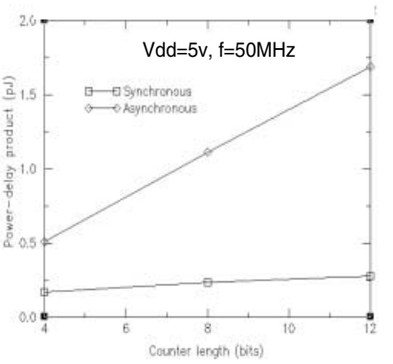

Fig. 9. Power-delay product vs counter length.

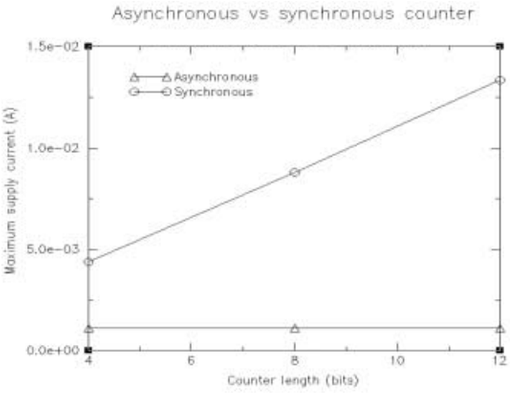

Fig. 10. Maximum supply current vs counter length.

Analog/Digital Integrated Circuits, where better timing and power performances do not necessarily imply more suitability for mixed-A/D design.

We have analyzed and simulated the switching noise generation by comparing the peak current results for two different synchronous clocking schemes (one- and two-phase clocking). Also, we have compared the results obtained for a synchronous and a asynchronous version of a common n-bit counter. Simulation data of different clocking styles have lead us to these two statements: a) Additional reduction of switching noise when using conventional digital CMOS circuits can be achieved by selecting the clock scheme suitably. b) The use of multiple clock-phase and asynchronous styles is strongly recommended. Although these solutions can introduce some problems of reliability (clock-skew), or complexity (more hardware), these are problems of minor concern in mixed-signal design, when comparing to switching noise effects.

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