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# A controller for practical stability of capacitor voltages in a five-level diode-clamped converter

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ABSTRACT

The balancing of the dc-link capacitor voltages represents the main technical challenge in multilevel diode-clamped converters. In particular, when the number of capacitors is greater than two, these power conversion systems must be actively controlled to achieve a correct voltage sharing. Focusing on the five-level diode-clamped converter topology, this paper deals with the voltage imbalance phenomenon from a control point view. For that purpose, the voltage balancing objective is addressed as a problem of ensuring the practical stability of a nonlinear system under the presence of external disturbances. Considering this approach, a novel control method is proposed to regulate the outputs of the system. It is based on several steps, which should be carried out during the controller design stage, that lead to define a discrete-time controller with sampling frequency corresponding to the triple of the ac-source frequency. Finally, the performance of the proposed controller is analyzed under varying operating conditions to demonstrate the capability and viability of the controller to attain the control goals.

KEYWORDS: multilevel power converter; diode-clamped converter (DCC); practical stability; dc-link capacitor voltage balancing; stability analysis

## 1. INTRODUCTION

### *1.1. Background: multilevel power converters*

Among the great variety of multilevel converter topologies [1, 2], the diode-clamped converter (DCC) has attracted special interest, particularly in medium-voltage and high-voltage applications for high-power systems, finding increased attention in academia as well as in industry [1, 3, 4]. In light of the world ever-rising demand for electrical energy, DCCs have emerged as an important solution due to the power levels reached by this power-conversion systems, and due to the attractive features and the more competitive performance they present [5, 6], in comparison with conventional two-level converters.

The idea behind multilevel converters is that by augmenting the number of levels, the voltages generated by the converter have more possible steps producing staircase waveforms, which approach the sinusoidal waveforms and reduce the total harmonic distortion [4, 5]. Thus, the generated voltages improve their quality as the number of levels increases, leading to multiple-step voltage waveforms with variable and controllable frequency, phase and amplitude. However, when the number of levels of the DCC is augmented, the structure of the converter becomes more and more complex. A greater number of power semiconductor switches, clamping diodes and dc-link capacitors is needed, increasing in this manner the device size and the assembly costs. Consequently, the difficulty of controlling the converter increases as well. In particular, the balancing of the dc-link

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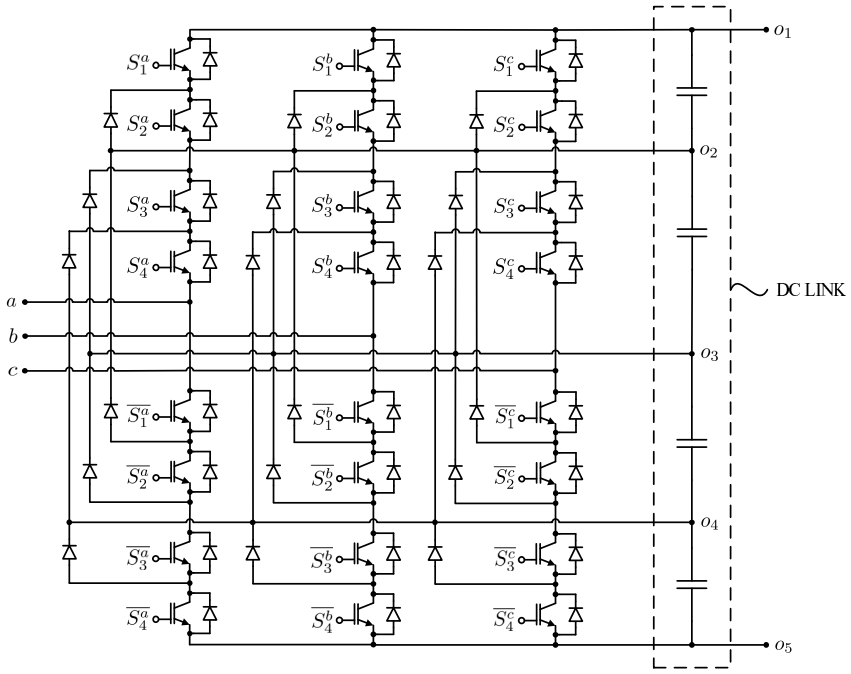



Figure 1. Circuit of a three-phase five-level diode-clamped power converter.

capacitor voltages becomes extremely complicated, especially for topologies that present more than three levels, and it represents one of the major technical challenges in multilevel converters. For these topologies, the converters must be actively controlled to achieve a correct voltage sharing.

Concerning the five-level DCC, topology illustrated in Fig. 1 and considered in this paper, the phenomenon of voltage imbalance of the dc-link capacitors represents a critical issue. Besides deteriorating the performance of the system, it may result in unsatisfactory behavior of the converter. On account of the different capacitor charging times during instantaneous active power transfers, the capacitor voltages tend to rise or fall in an uncontrolled way. Consequently, they can even cause the operational failure of the converter.

In view of this, there is an essential need to keep balanced the capacitor voltages. Nevertheless, dealing with the voltage imbalance problem is not an easy task. Considering conventional modulation techniques, multilevel DCCs present some limits [7, 8], for which an equal capacitor voltage sharing is not possible in all the operating conditions, if single multilevel inverters or rectifiers are considered. These theoretical and practical limits are related to the modulation index and the power factor. Due to this fact, the subject, that is, the balancing of the capacitor voltages, has been one of the most active research topics in the field of power electronics. It has been addressed in different ways, leading to several approaches and solutions in the technical literature:

1. The first and easiest approach to cope with the problem consists of supplying the dc link of the converter with four separate dc sources, one per dc-link capacitor [9].

2. The second approach is to install some voltage balance regulation circuitry. Inclusion of buck-boost converters to force energy transfer from outer capacitors to inner ones [10], additional circuit-based equalizing controllers with and without extra switching devices [11], voltage balancing based on auxiliary capacitors [12], or circuits to maintain the voltages across the capacitors constant [13], are some examples.

3. The third approach introduces a fourth leg in the converter, yielding the five-level four-leg four-wire DCC topology [14].

4. The fourth approach uses a back-to-back configuration, connecting a multilevel rectifier to a multilevel inverter, in order to widen the set of converter operating conditions [15–18]. This means that there are much more possibilities for balancing the charge among the dc-link capacitors. Nonetheless, even so, a voltage balancing strategy should be included. Some examples of control strategies considered to deal with the voltage imbalance problem in the back-to-back converter can be consulted in [19–21].

The requirements for additional power hardware or auxiliary devices that these approaches involve, represent a significant increase in the converter cost and add complexity. In order to provide a more economical solution, other approaches have been also investigated:

5. Another approach considers switching strategies based on modulation techniques [22, 23]. Taking advantage of the redundant switching states of the converter to optimize a certain cost function [24, 25], they guarantee the capacitor voltage balancing. Nevertheless, there exist some limitations to this method regarding the converter range of operation [7, 8]. To overcome the problem, modulation strategies combined with control schemes have been proposed [26,27]. Other authors use also modulation strategies but adding in this case chopper stages [28, 29] and front-end diode rectifiers [30]. In [31], a control method based on PWM that introduces multiband hysteresis comparators to simplify the control of the main circuit while injecting current components in the dc-link intermediate points of the DCC has been also proposed.

6. Other approach defines a discrete-time dynamic model of the converter with the purpose of applying a predictive control strategy. This approach has been presented in [32].

Therefore, among the viable voltage balancing solutions that reduce the voltage imbalance to an acceptable level, those that do not implement additional components need however a complex and more elaborated control strategy. Consequently, a higher computational time is required.

### *1.2. Considered control approach to cope with the problem*

Recently, a completely different approach has been proposed in [33]. In that paper, it is shown that the problem of the capacitor voltage imbalance can be addressed as a problem of regulating the multiple outputs of a nonlinear system subject to exogenous disturbances. In view of this result, this novel problem statement allows to widen the range of alternatives to cope with the voltage imbalance problem. Besides, it represents a more interesting but also involved approach, from a control point of view. Note that the topic of controlling a plant subject to disturbances has been widely studied in control theory [34, 35] and used for different engineering applications.

In the last decades, the problem of the presence of disturbances in nonlinear systems has attracted considerable attention [36–39]. Important research is still being done in this area considering various control methods [40–42]. Generally speaking, the control law to apply, commonly by error feedback, is designed with a twofold purpose [36]: it is designed, on the one hand, to achieve internal asymptotic stability and, on the other, to guarantee output regulation. Internal asymptotic stability means that, when the disturbances disappear, the equilibrium point of the closed-loop system is asymptotically stable. Output regulation means that, for all possible initial states of the closed-loop state variables, the tracking error tends to zero as time tends to infinity. Therefore, the controller should be designed in such a way that it asymptotically forces the tracking error to zero despite the presence of disturbances.

In contrast, returning to the matter at hand, the balancing of the capacitor voltages in the five-level DCC is not related to asymptotic stability requirements but with achieving the practical stability [43, 44] of the system. In this way, ensuring that the capacitor voltages remain within certain predefined subsets, the uncontrolled rise or fall of these voltages is avoided. This fact is basic in the design of the voltage balance controller proposed in this paper, which represents the main contribution of this work. For this purpose, the approach presented in [33] to describe the voltage imbalance problem is adopted, including also the preliminary control ideas discussed in

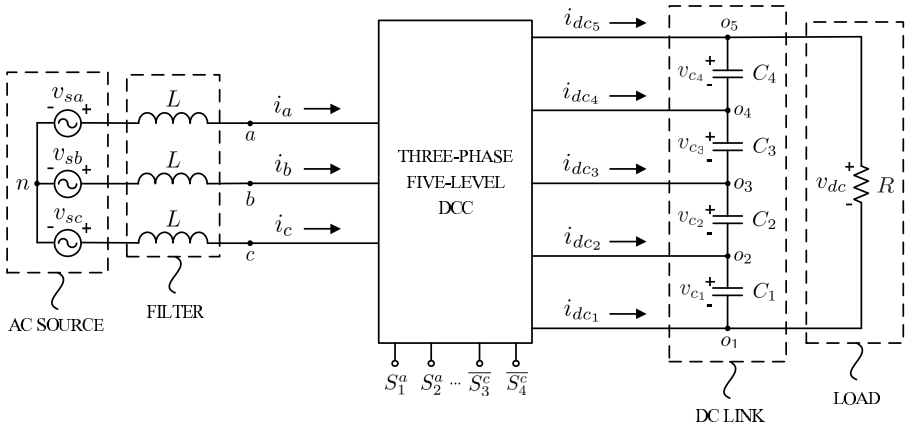



Figure 2. Schematic diagram of the five-level diode-clamped converter working as rectifier.

that paper that lead to define a discrete-time controller focused on an only given system operating point, whose sampling frequency is three times the frequency of the ac source connected to the converter. The new proposed controller, which is based on several steps that should be carried out during the design stage, presents the following improvements: (i) criterion of selection of the control inputs; (ii) controller extension to be used under varying operating conditions; (iii) and evaluation of the parametric robustness of the controller. In addition, the proposed controller enables voltage balancing without the need of implementing extra circuitry, and it presents also reduced computational cost. Furthermore, the stability of the closed-loop system is analyzed in this paper.

The structure of the paper is as follows. Section 2 describes the model of the five-level DCC and defines also the control objectives. Then, Section 3 states the problem of the capacitor voltage imbalance addressed in this paper. The design stage and the implementation of the controller is presented in Section 4, while the extension of the controller to be used under varying system operating conditions is discussed in Section 5. Afterwards, Section 6 is devoted to evaluate the performance evaluation of the controller. Finally, some concluding remarks are included in Section 7, summarizing the key results of the paper.

## 2. MODEL OF THE POWER CONVERTER AND CONTROL OBJECTIVES

Figure 2 illustrates a schematic diagram of the configuration considered in this paper, which is the rectifier operating mode of the five-level DCC. In this way, the converter is connected, on the one hand, to an ac source or to the grid through smoothing inductors $L$ and, on the other hand, to a pure resistive load $R$. The dc link is composed of capacitors $C_1$, $C_2$, $C_3$ and $C_4$, all of identical capacitance $C$. Their voltages are represented by $v_{c_1}$, $v_{c_2}$, $v_{c_3}$ and $v_{c_4}$. Besides, the phase currents are denoted by $i_a$, $i_b$ and $i_c$, while the phase voltages are defined by $v_{sa}$, $v_{sb}$ and $v_{sc}$.

### 2.1. *Continuous model of the five-level DCC*

The dynamic model of the five-level DCC presented in [45] is considered in this paper. Including an appropriated modulation strategy [5,6], the essential idea of the model is that it is assumed that when the frequency range of the system is much lower than the switching frequency, the gating signals that regulate the positions of the power switches of the converter can be replaced by their average values in that switching period. In this manner, the converter is described by a continuous model. The average values of the gating signals, denoted in what follows by $\delta_a$, $\delta_b$ and $\delta_c$, are the control inputs of the converter model. Because they are assumed to be carried out through a modulator, they should be located within the domain

$$D_{\delta_{abc}} \in \mathbb{R}^3 \quad := \quad D_{\delta_a} \times D_{\delta_b} \times D_{\delta_c}, \tag{1}$$

such that $D_{\delta_i} = [-1, 1]$, for $i = a,\ b,\ c$. In this manner, the modulation technique is correctly implemented.

The model includes, among others, the dynamics of the differences between the voltages of the dc-link capacitors. For this purpose, the voltage difference variables

$$v_{d_1} = v_{c_1} - v_{c_4} \tag{2}$$
$$v_{d_2} = v_{c_2} - v_{c_3} \tag{3}$$
$$v_{d_3} = v_{c_3} - v_{c_4}, \tag{4}$$

are introduced in the modeling process. In addition, the converter model in $\alpha\beta\gamma$ orthogonal coordinates is also presented, where both phase currents and voltages are transformed from $abc$ into $\alpha\beta\gamma$ coordinates, yielding the current variables $i_\alpha$ and $i_\beta$, and the voltage variables $v_\alpha$ and $v_\beta$, respectively. Moreover, the control inputs are also transformed into $\delta_\alpha$, $\delta_\beta$ and $\delta_\gamma$.

### 2.2. *Control objectives*

The control objectives for the rectifier configuration of the five-level DCC are stated in this section. On one hand, some are defined in relation to the voltage levels of the dc-link capacitors and, as pointed out in the introduction, are related to practical stability requirements.

*Definition 1*
A system is said to be practically stable if there exist positive constants $b$ and $c$, independent of $t_0 \geq 0$, and for every $a \in (0, c)$, there is $T_{ab} = T_{ab}(a, b) \geq 0$, independent of $t_0$, such that

$$||\boldsymbol{x}(t_0)|| \leq a \ \Rightarrow \ ||\boldsymbol{x}(t)|| \leq b\,, \qquad \forall t \geq t_0 + T_{ab}\,, \tag{5}$$

where $\boldsymbol{x} \in \mathbb{R}^n$ is the state of the system.

On the other hand, other control objectives are related to the management of the instantaneous powers [46]. They all are described as follows:

1. The voltage difference variables $v_{d_1}$, $v_{d_2}$ and $v_{d_3}$ should be regulated to assure the practical stability of the system.

2. The total dc-link voltage, denoted by $v_{dc}$, should be directed to its reference. The reference is defined by the positive constant $v_{dc}^*$.

3. The instantaneous active power $p$ defined as

$$p = v_\alpha i_\alpha + v_\beta i_\beta, \tag{6}$$

should be driven to its reference $p^*$.

4. The instantaneous reactive power $q$ defined as

$$q = v_\alpha i_\beta - v_\beta i_\alpha, \tag{7}$$

should be directed to its desired value $q^*$.

Since the paper addresses the phenomenon of voltage imbalance of the dc-link capacitors, it is mainly focused on the first control aim. Note that guaranteeing the fulfillment of this control objective, it is avoided the uncontrolled rise or fall of the dc-link capacitor voltages. Regarding the other control goals, it is assumed in the following that there exist other controllers that deal with them. Commonly, the control inputs $\delta_\alpha$ and $\delta_\beta$ together with the instantaneous power reference $p^*$ are used by the controllers to that end. Consequently, the control input $\delta_\gamma$ remains as a degree of freedom for coping with the capacitor voltage imbalance.

## 3. PROBLEM STATEMENT

As previously mentioned in Section 1, the approach presented in [33] to deal with the voltage imbalance problem in the five-level DCC is adopted here. In that paper, a mathematical analysis of the variation over the time of (2)-(4) in steady state is carried out considering some practical assumptions[†]. In this way, the converter dynamics are studied under assumptions: (i) the instantaneous power dynamics are much faster than the total dc-link voltage dynamics and than those of the capacitor voltage differences; and (ii) the total dc-link voltage has been properly regulated and can be approximated by its steady-state reference.

As a result, an approximated model, which will be used to design the controller, is derived from the original model [45], replacing some variables by their approximations in steady state. Concretely, the phase currents $i_\alpha$ and $i_\beta$ as well as the control inputs $\delta_\alpha$ and $\delta_\beta$ are, respectively, expressed by

$$i_\alpha\big|_{ss} \simeq \frac{1}{v_\alpha^2+v_\beta^2}\left(v_\alpha p^* - v_\beta q^*\right) \tag{8}$$

$$i_\beta\big|_{ss} \simeq \frac{1}{v_\alpha^2+v_\beta^2}\left(v_\beta p^* + v_\alpha q^*\right) \tag{9}$$

$$\delta_\alpha\big|_{ss} \simeq \frac{2}{v_{dc}^*}\left(\left(1+\frac{2\pi f L q^*}{v_\alpha^2+v_\beta^2}\right)v_\alpha + \frac{2\pi f L p^*}{v_\alpha^2+v_\beta^2}v_\beta\right) \tag{10}$$

$$\delta_\beta\big|_{ss} \simeq \frac{2}{v_{dc}^*}\left(\left(1+\frac{2\pi f L q^*}{v_\alpha^2+v_\beta^2}\right)v_\beta - \frac{2\pi f L p^*}{v_\alpha^2+v_\beta^2}v_\alpha\right). \tag{11}$$

The subscript $ss$ indicates the condition of steady state of the system, meaning that $p$, $q$ and $v_{dc}$ are located around their respective steady-state reference values $p^*$, $q^*$ and $v_{dc}^*$.

The approximated model derived is described by the set of equations

$$C\frac{dv_{d_1}}{dt} = \omega_{13}(t)\,\delta_\gamma^3 + \omega_{12}(t)\,\delta_\gamma^2 + \omega_{11}(t)\,\delta_\gamma + \omega_{10}(t) \tag{12}$$

$$C\frac{dv_{d_2}}{dt} = \omega_{23}(t)\,\delta_\gamma^3 + \omega_{22}(t)\,\delta_\gamma^2 + \omega_{21}(t)\,\delta_\gamma + \omega_{20}(t) \tag{13}$$

$$C\frac{dv_{d_3}}{dt} = \omega_{33}(t)\,\delta_\gamma^3 + \omega_{32}(t)\,\delta_\gamma^2 + \omega_{31}(t)\,\delta_\gamma + \omega_{30}(t)\,, \tag{14}$$

where $\delta_\gamma$ is the unique control input of the system. Notice that the dynamics of the state variables $v_{d_1}$, $v_{d_2}$ and $v_{d_3}$ are decoupled. Functions $\omega_{ij}(t)$, for $i = 1, 2, 3$ and $j = 0, 1, 2, 3$, are regarded as disturbances produced by an external generator or exosystem. They are defined as follows

$$\omega_{ij}(t) = \mu_{ij}\sin\left(3\cdot 2\pi f t + \theta_{ij}\right) + \eta_{ij}, \tag{15}$$

for $i = 1, 2, 3$ and $j = 0, 1, 2, 3$. Constant parameters $\mu_{ij}(p^*, q^*, v_{dc}^*)$ and $\theta_{ij}(p^*, q^*, v_{dc}^*)$ are the amplitudes and the phases of the sinusoidal terms of functions $\omega_{ij}(t)$, and $\eta_{ij}(p^*, q^*, v_{dc}^*)$ are their mean values. In addition, the frequency of the sinusoidal terms of functions $\omega_{ij}(t)$ corresponds to the triple frequency of the ac-source frequency, denoted by $f$, which is also the frequency of the phase voltages. This fact is related to the existence of an inherent ac-voltage fluctuation or ripple, at three times the frequency of the ac source, to each of the four dc-link capacitors [23, 29].

Hence, the voltage imbalance phenomenon is addressed as a problem of assuring the practical stability of the nonlinear system (12)-(14) subject to the disturbances (15). It is worth stressing that

[†]Similar analysis of the dynamics of the converter have been worked out in other multilevel topologies, for example, in the three-level neutral-point-clamped converter [47] or in the three-level diode-clamped back-to-back converter [48].

the disturbances are described by functions of time that depend on the particular system operating conditions, defined in steady state by the references $p^*$, $q^*$ and $v_{dc}^*$. Consequently, the constant parameters $\mu_{ij}$, $\theta_{ij}$ and $\eta_{ij}$ of the disturbances should be evaluated analytically or by means of simulation as a function of the particular steady-state references considered. In this regard, the evaluation of the specific values of the parameters of the disturbances represents a preliminary stage before beginning with the design of the controller.

## 4. CONTROLLER DESIGN AND IMPLEMENTATION

A key point of the controller presented in the following is that it is formulated as a discrete-time controller with sampling frequency corresponding to the triple of the frequency of the ac source. It is worth mentioning that this sampling frequency corresponds also to the frequency of the sinusoidal terms of the disturbances defined by (15) in the previous section. Furthermore, inside these periods the control input commutes between two constant values to be chosen by the controller at the beginning of the sampling period.

The primary reason behind this decision is to exploit the properties and knowledge of the disturbance patterns to cope with the complexity of the model (12)-(14). In other words, it is taken advantage of the fact that the period

$$T \;=\; \frac{1}{3f}, \tag{16}$$

i.e., the period of the sinusoidal terms of the disturbances, is known. Besides, the requirement of practical stability of the system can be satisfied assuring that the following variables

$$v_{d_i}(kT)\,, \quad \forall k \in \mathbb{N}, \quad \text{for } i = 1, 2, 3, \tag{17}$$

remain within certain subsets.

The dynamics of these variables are expressed by

$$v_{d_i}((k+1)\,T\,) \;=\; v_{d_i}(kT) \,+\, \triangle v_{d_i}\big|_{kT}^{(k+1)T}, \quad \text{for } i = 1, 2, 3, \tag{18}$$

where the terms $\triangle v_{d_i}\big|_{kT}^{(k+1)T}$ represent the net variation over a sampling period of the voltage difference variables $v_{d_1}$, $v_{d_2}$ and $v_{d_3}$. Taking into account the approximated model (12)-(14), they are described by

$$\begin{aligned} \triangle v_{d_i}\big|_{kT}^{(k+1)T} \;=\; & \int_{kT}^{(k+1)T} \omega_{i3}(t)\,\delta_\gamma^3\,dt \,+\, \int_{kT}^{(k+1)T} \omega_{i2}(t)\,\delta_\gamma^2\,dt \,+\, \int_{kT}^{(k+1)T} \omega_{i1}(t)\,\delta_\gamma\,dt \\ & + \int_{kT}^{(k+1)T} \omega_{i0}(t)\,dt\,, \quad \text{for } i = 1, 2, 3. \end{aligned} \tag{19}$$

Based on these previous concepts, several steps should be carried out during the controller design stage in order to implement subsequently the voltage balance controller.

### *4.1. Definition of the control law*

Considering the particular expression of the disturbances (15), the control law

$$\delta_\gamma \;=\; \begin{cases} \delta_{\gamma_1}, & \text{if} \quad \omega_{31}(t) \le \eta_{31} - \mu_{31}\cos(\pi\varepsilon) \quad \text{and} \quad kT \le t < (k+1)\,T \\ \delta_{\gamma_2}, & \text{if} \quad \omega_{31}(t) > \eta_{31} - \mu_{31}\cos(\pi\varepsilon) \quad \text{and} \quad kT \le t < (k+1)\,T, \end{cases} \tag{20}$$

is proposed, where $T$ is defined by (16). In this manner, the period of the sinusoidal terms of the disturbances is used to define the control law. Parameters $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ are a couple of constant values

to be chosen at the beginning of each sampling period, and constant $\varepsilon$ is a design parameter such that $0 < \varepsilon < 1$. Consequently, the total time periods $t_{\gamma_1}$ and $t_{\gamma_2}$ when, respectively, $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ are applied during a whole period $T$ depend on the choice of $\varepsilon$. They are described by

$$t_{\gamma_1} = \varepsilon T \tag{21}$$
$$t_{\gamma_2} = (1-\varepsilon)\, T. \tag{22}$$

*Remark 1*
The motivation for this control law is the following. When $\delta_\gamma$ is small enough, the disturbances $\omega_{i1}(t)$, for $i = 1, 2, 3$, are the $\delta_\gamma$-dependent dominant terms in (12)-(14). In addition, they are also the $\delta_\gamma$-dependent dominant terms of (19). Therefore, (19) can be approximated by

$$\triangle v_{d_i}\big|_{kT}^{(k+1)T} \simeq \int_{kT}^{(k+1)T} \omega_{i1}(t)\, \delta_\gamma \, dt + \int_{kT}^{(k+1)T} \omega_{i0}(t)\, dt, \quad \text{for } i = 1, 2, 3. \tag{23}$$

Then, considering these expressions together with the particular behavior of each one of the disturbances, it leads to approximate (18) by

$$v_{d_1}((k+1)\,T) \simeq v_{d_1}(kT) + \eta_{11} \int_{kT}^{(k+1)T} \delta_\gamma \, dt \tag{24}$$
$$v_{d_2}((k+1)\,T) \simeq v_{d_2}(kT) + \eta_{21} \int_{kT}^{(k+1)T} \delta_\gamma \, dt \tag{25}$$
$$v_{d_3}((k+1)\,T) \simeq v_{d_3}(kT) + \int_{kT}^{(k+1)T} \omega_{31}(t)\, \delta_\gamma \, dt + \eta_{30} T. \tag{26}$$

Besides, there exists an unique control input to deal with the regulation of (17), that is, with the regulation of three variables with decoupled dynamics (24)-(26). It suggests to use $\delta_\gamma$ to control any variable (or some of them) during some periods of time and to use it to control the rest of the variables (or the remaining one) in the spare time. As can be seen in (20), the selection of the control values to apply in each time instant is based on the evaluation of $\omega_{31}(t)$. Note that it is the only time-varying system parameter present in (24)-(26), since $\eta_{11}$, $\eta_{21}$ as well as $\eta_{30}$ are all constant values. In view of this, it is reasonable to control $v_{d_3}$ when $\omega_{31}(t)$ is large and control the other variables when the contrary occurs.

### 4.2. *First design step: analysis of the dynamics in discrete time of the capacitor voltage differences*

The target of the first design step is to analyze the behavior of the discrete-time dynamics (18) as a function of $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$, considering the proposed control law (20). In this way, the analysis serves as a basis for identifying and selecting the appropriate pair of constant control values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ that should be applied during a particular period of time (16). Since $\delta_\gamma$ is piece-wise constant, the analysis can be performed, and (19) can be then analytically calculated.

Beginning with the voltage difference variables $v_{d_1}$ and $v_{d_2}$, expressions (19) lead to the equations

$$\begin{aligned} \triangle v_{d_i}\big|_{kT}^{(k+1)T} = {} & \eta_{i3}\left(t_{\gamma_1}\delta_{\gamma_1}^3 + t_{\gamma_2}\delta_{\gamma_2}^3\right) + \sin(\pi\varepsilon)\,\frac{(-1)^i\,\mu_{i2}}{3\pi f}\left(\delta_{\gamma_1}^2 - \delta_{\gamma_2}^2\right) \\ & + \eta_{i1}\left(t_{\gamma_1}\delta_{\gamma_1} + t_{\gamma_2}\delta_{\gamma_2}\right), \quad \text{for } i = 1, 2. \end{aligned} \tag{27}$$

Table I. Parameters of the study system.

| Parameter | Value |
|---|---|
| Ac-source frequency ($f$) | 50 Hz |
| Phase voltages ($v_{sa}$, $v_{sb}$, $v_{sc}$) | 230 $V_{RMS}$ |
| Inductors ($L$) | 3 mH |
| Capacitors ($C_1$, $C_2$, $C_3$, $C_4$) | 4700 $\mu$F |
| Resistive load ($R$) | 120 $\Omega$ |
| Operating point: | |
| Instantaneous active power reference ($p^*$) | 4083.3 W |
| Instantaneous reactive power reference ($q^*$) | 0 VAr |
| Total dc-link voltage reference ($v_{dc}^*$) | 700 V |

Concerning the variable $v_{d_3}$, the expression that should be evaluated is defined in this case by (19), for $i = 3$. It results in the equation

$$\begin{aligned} \triangle v_{d_3}\big|_{kT}^{(k+1)T} \;=\; & \eta_{33}\left(t_{\gamma_1}\delta_{\gamma_1}^3 + t_{\gamma_2}\delta_{\gamma_2}^3\right) + \eta_{32}\left(t_{\gamma_1}\delta_{\gamma_1}^2 + t_{\gamma_2}\delta_{\gamma_2}^2\right) \\ & + \sin(\pi\varepsilon)\,\frac{\mu_{32}}{3\pi f}\left(\delta_{\gamma_2}^2 - \delta_{\gamma_1}^2\right) + \eta_{31}\left(t_{\gamma_1}\delta_{\gamma_1} + t_{\gamma_2}\delta_{\gamma_2}\right) \\ & + \sin(\pi\varepsilon)\,\frac{\mu_{31}}{3\pi f}\left(\delta_{\gamma_2} - \delta_{\gamma_1}\right) + \eta_{30}T\,. \end{aligned} \tag{28}$$

In the following, the values of $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ that make $\triangle v_{d_i}\big|_{kT}^{(k+1)T} = 0$, for $i = 1, 2, 3$, are studied. Consequently, (27) and (28) are set to zero, yielding the particular solutions situated, respectively, in manifolds

$$\mathcal{M}_i \;:=\; \left\{ (\delta_{\gamma_1}, \delta_{\gamma_2}) \in \mathbb{R}^2 \;\middle|\; \triangle v_{d_i}\big|_{kT}^{(k+1)T} = 0 \right\}, \quad \text{for } i = 1, 2, 3, \tag{29}$$

which can be represented by curves in the control input space $\delta_{\gamma_2} - \delta_{\gamma_1}$.

*Application example 1*
Consider the values of the system parameters shown in Table I and the behavior of the disturbances (15), for this specific operating point, that can be consulted in [33]. Under this particular situation, Fig. 3 illustrates manifolds (29) in the control input space $\delta_{\gamma_2} - \delta_{\gamma_1}$, when the design parameter $\varepsilon$ of (20) is set to $1/3$. Figure 4 depicts also manifolds (29) but in this case for $\varepsilon = 2/3$. Notice that the curves change depending on the chosen value of $\varepsilon$.

### *4.3. Second design step: generation of the look-up table for $\delta_\gamma$*

The objective at this design step it to generate a look-up table for control input $\delta_\gamma$ that includes a set of eight couples of constant values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$. These couples of values will be used subsequently via control law (20), when the controller is implemented in the system.

The selection of the values of $\delta_\gamma$ is based on the particular operating conditions of the system. Thus, for a given operating point, manifolds (29) delimit various areas in the control input space $\delta_{\gamma_2} - \delta_{\gamma_1}$. These areas are based on a partition of the control input space such that each subset provides a different set of signs of variables (19). Considering this fact, in this design step, a particular couple of values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ should be selected for each area.

*Application example 2*
Focusing on the figures described in the previous application example, both Fig. 3 and Fig. 4 show

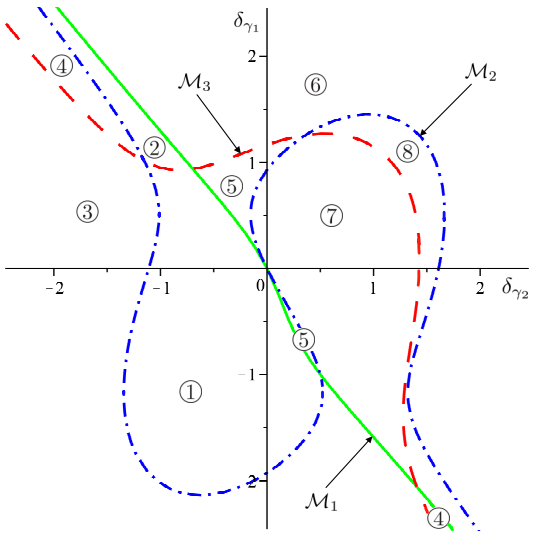



Figure 3. Manifolds $\mathcal{M}_i$, for $i = 1, 2, 3$, in the control input space $\delta_{\gamma_2} - \delta_{\gamma_1}$, when parameter $\varepsilon$ is set to $1/3$.

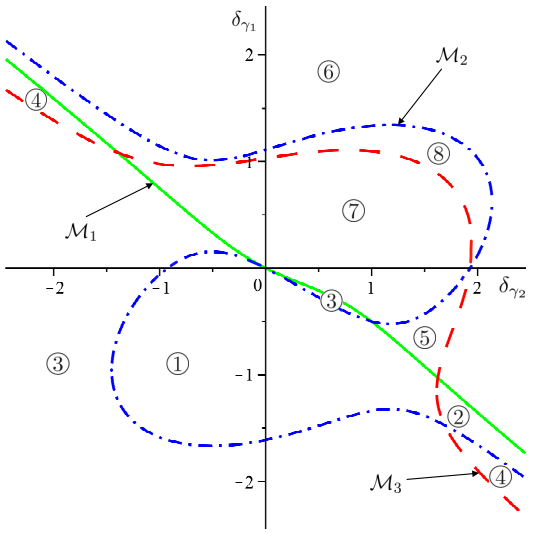



Figure 4. Manifolds $\mathcal{M}_i$, for $i = 1, 2, 3$, in the control input space $\delta_{\gamma_2} - \delta_{\gamma_1}$, when parameter $\varepsilon$ is set to $2/3$.

distinct areas determined by the curves (29). These areas are numbered from 1 to 8 in the figures and can be defined mathematically by different manifolds. For instance, the area denoted by number 1 is defined by

$$\begin{aligned} \text{Area 1} \quad := \quad & \Big\{ (\delta_{\gamma_1}, \delta_{\gamma_2}) \in \mathbb{R}^2 \mid \triangle v_{d_1}\big|_{kT}^{(k+1)T} > 0 \quad \bigcap \quad \triangle v_{d_2}\big|_{kT}^{(k+1)T} > 0 \\ & \bigcap \quad \triangle v_{d_3}\big|_{kT}^{(k+1)T} > 0 \Big\}. \end{aligned} \tag{30}$$

Regarding the other areas, their description is summarized in Table II. According to this table, notice that the application of (20) causes distinct effect in the voltage difference variations (19) depending on the particular area where the pair of values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ is selected.

With the purpose of choosing the eight specific pairs of values, the following consideration should be taken into account. As mentioned in Section 2, control inputs $\delta_\alpha$, $\delta_\beta$ and $\delta_\gamma$ represent

Table II. Description of the areas delimited by manifolds $\mathcal{M}_i$, for $i = 1, 2, 3$.

| | $\triangle v_{d_1}\big\vert_{kT}^{(k+1)T}$ | $\triangle v_{d_2}\big\vert_{kT}^{(k+1)T}$ | $\triangle v_{d_3}\big\vert_{kT}^{(k+1)T}$ |
|---|---|---|---|
| Area 1 | $+$ | $+$ | $+$ |
| Area 2 | $+$ | $+$ | $-$ |
| Area 3 | $+$ | $-$ | $+$ |
| Area 4 | $+$ | $-$ | $-$ |
| Area 5 | $-$ | $+$ | $+$ |
| Area 6 | $-$ | $+$ | $-$ |
| Area 7 | $-$ | $-$ | $+$ |
| Area 8 | $-$ | $-$ | $-$ |

in $\alpha\beta\gamma$ coordinates the average values of the gating signals. Thus, they are first transformed into $abc$ coordinates via the power-invariant form of the Inverse Clarke Transform. The following matrix

$$T_{\alpha\beta\gamma\to abc} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix}, \tag{31}$$

is used to that end. The transformation yields $\delta_a$, $\delta_b$ and $\delta_c$. Then, these control inputs are modulated to generate the gating signals. Because the control inputs in $abc$ coordinates should remain in the domain (1) to implement correctly the modulation, there exist also some theoretical limitations regarding $\delta_\alpha$, $\delta_\beta$ and $\delta_\gamma$. Hence, the choice of the values of $\delta_\gamma$ should be based on a trade-off between the different control objectives, since $\delta_\alpha$ and $\delta_\beta$ are devoted to regulate the instantaneous powers of the system.

In view of this, the criterion adopted in this paper is to select the couples of values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ as close to zero as possible. In order to achieve this goal, the design parameter $\varepsilon$ plays a fundamental role. As can be seen in Fig. 3 and Fig. 4, its specific chosen value makes the different areas change. Consequently, the value of $\varepsilon$ can be used to optimize the couple of values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ to select for each one of the eight areas. In addition, it is worth stressing that there might be situations such that (29) do not lead to eight distinct areas. For these particular cases, parameter $\varepsilon$ can be designed to make the manifolds (29) define new different areas in the control input space. Note that, in order to be able to compensate nonzero values of (17) with the proposed control method, it is necessary to produce all possible sign combinations of (27) and (28).

*Remark 2*

The procedure to obtain the couples of control values is based on the definition of a grid of points in the control input space $\delta_{\gamma_2} - \delta_{\gamma_1}$. Considering first an only fixed value of $\varepsilon$, functions (27) and (28) are evaluated for each one of the points of the grid. In this manner, it is possible to know exactly in which of the areas described by Table II the points are located. Then, for each one of the eight areas, among the whole set of points that belongs to a particular area, the specific point situated closer to zero is selected.

Afterwards, and with the aim of optimizing the chosen control values, the procedure is repeated for different values of $\varepsilon$. Thus, if any of the new selected couples of values is closer to zero than the one chosen before, the older couple of values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ is replaced by the new one. The whole procedure does not take more than a pair of minutes and is carried out off line.

Table III. Evaluation of the signs of the capacitor voltage difference variables.

| $v_{d_1}(kT)$ | $v_{d_2}(kT)$ | $v_{d_3}(kT)$ | | Signs | Selected area |
|---|---|---|---|---|---|
| $>0$ | $>0$ | $>0$ | $\longrightarrow$ | $+++$ | Area 8 |
| $>0$ | $>0$ | $<0$ | $\longrightarrow$ | $++-$ | Area 7 |
| $>0$ | $<0$ | $>0$ | $\longrightarrow$ | $+-+$ | Area 6 |
| $>0$ | $<0$ | $<0$ | $\longrightarrow$ | $+--$ | Area 5 |
| $<0$ | $>0$ | $>0$ | $\longrightarrow$ | $-++$ | Area 4 |
| $<0$ | $>0$ | $<0$ | $\longrightarrow$ | $-+-$ | Area 3 |
| $<0$ | $<0$ | $>0$ | $\longrightarrow$ | $--+$ | Area 2 |
| $<0$ | $<0$ | $<0$ | $\longrightarrow$ | $---$ | Area 1 |

Finally, the look-up table that will be used to choose the values of $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ at the beginning of each sampling period is generated. This table is composed of a set of couples of control values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ and is created including the specific pair of values selected for each one of the eight areas. Besides, the table should also include the specific value of the design parameter $\varepsilon$ associated with each particular pair of values.

### *4.4. Implementation of the control law*

The implementation of the control law is based on the on-line evaluation of the signs of the variables $v_{d_i}(kT)$, for $i = 1, 2, 3$. Thus, the voltage difference variables $v_{d_1}$, $v_{d_2}$ and $v_{d_3}$ should be first evaluated. Then, depending on the signs of these three variables, a specific couple of constant values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ of the look-up table described in Section 4.3 is selected. The chosen pair is the one that produces the opposite effect to that marked by the signs of (17) in the voltage difference variations (19). Table III illustrates this concept. Then, control law (20) is applied considering the particular value of $\varepsilon$ associated with the selected couple of values. That is, according to (20), the constant values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ are applied. The process is repeated each sampling period, which is equal to the period of the sinusoidal terms of the disturbances, defined by (16).

### *4.5. Stability analysis*

In order to analyze the stability of the resultant closed-loop system, the dc-link capacitor voltage differences (2)-(4) are represented in vectorial form by means of vector

$$\boldsymbol{v_d}(t) \quad = \quad [\, v_{d_1}(t) \quad v_{d_2}(t) \quad v_{d_3}(t) \,]^T , \tag{32}$$

to simplify the notation considered. Besides, the following bound is defined:

- $\triangle_{\max} = \max \left| \triangle v_{d_{ij}} \right|$, for $i = 1, 2, 3$ and $j = 1, ..., 8$, where the terms $\triangle v_{d_{ij}}$ stand for the specific values of the voltage difference variations (19) in each one of the eight regions defined in Table II, for the particular couples of control values of the look-up table for $\delta_\gamma$ described in Section 4.3 and their respective design parameters $\varepsilon$.

*Proposition 1*
Consider nonlinear system (12)-(14) with the control law given by (20). The values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ of the control law are chosen at the beginning of each sampling period $T$ from the generated look-up table for $\delta_\gamma$, considering the particular criterion described in Section 4.4 and illustrated in Table III. Then, system (12)-(14) is practically stable.

*Proof*
Consider first the discrete-time dynamics of the voltage difference variables expressed by (18) and

a large value for $||\boldsymbol{v_d}(0)||_\infty$. Because each specific couple of control values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ to apply during a time period $T$ is selected producing the opposite effect to that marked by the signs of variables $v_{d_i}(kT)$, for $i = 1, 2, 3$, in the voltage difference variations (19) and, in addition, these voltage variations are such that $\left| \triangle v_{d_i} |_{kT}^{(k+1)T} \right| \leq \triangle_{\max}$, for $i = 1, 2, 3$, after a finite time $t_1 = k_1 T$, it follows that

$$||\boldsymbol{v_d}(kT)||_\infty \leq \triangle_{\max}, \quad \forall k \geq k_1. \tag{33}$$

Note that if $||\boldsymbol{v_d}(0)||_\infty \leq \triangle_{\max}$, (33) is satisfied in this particular case $\forall k$, that is, it is satisfied for $k_1 = 0$. Then, consider the continuous-time evolution of $v_{d_i}(t)$, for $i = 1, 2, 3$, described by (12)-(14). Inside the time period $t \in [kT, (k+1)T]$, a bound denoted by $\Gamma$ for the time derivatives of $v_{d_i}(t)$ can be obtained as follows

$$\begin{aligned}
\left| \frac{dv_{d_i}(t)}{dt} \right| &= \frac{1}{C} \left| \omega_{i3}(t)\, \delta_\gamma^3 + \omega_{i2}(t)\, \delta_\gamma^2 + \omega_{i1}(t)\, \delta_\gamma + \omega_{i0}(t) \right| \\
&\leq \frac{1}{C} \left( |\omega_{i3}(t)|\, \delta_{\gamma_{\max}}^3 + |\omega_{i2}(t)|\, \delta_{\gamma_{\max}}^2 + |\omega_{i1}(t)|\, \delta_{\gamma_{\max}} + |\omega_{i0}(t)| \right) \\
&\leq \frac{1}{C} \left( \omega_{i3_{\max}} \delta_{\gamma_{\max}}^3 + \omega_{i2_{\max}} \delta_{\gamma_{\max}}^2 + \omega_{i1_{\max}} \delta_{\gamma_{\max}} + \omega_{i0_{\max}} \right) \\
&\leq \frac{1}{C} \max_{i=1,2,3} \left( \omega_{i3_{\max}} \delta_{\gamma_{\max}}^3 + \omega_{i2_{\max}} \delta_{\gamma_{\max}}^2 + \omega_{i1_{\max}} \delta_{\gamma_{\max}} + \omega_{i0_{\max}} \right) \\
&= \Gamma, \quad \text{for } i = 1, 2, 3.
\end{aligned} \tag{34}$$

Constant parameters $\delta_{\gamma_{\max}}$ and $\omega_{ij_{\max}}$, for $i = 1, 2, 3$ and $j = 0, 1, 2, 3$, are defined by:

- $\delta_{\gamma_{\max}} = \max |\delta_\gamma|$, where the considered values of $\delta_\gamma$ are those defined in the generated look-up table for this control input.
- $\omega_{ij_{\max}} = \max_{t \in [0,T]} |\omega_{ij}(t)|$, for $i = 1, 2, 3$ and $j = 0, 1, 2, 3$, where the terms $\omega_{ij}(t)$ are the disturbances of the system described by (15) and $T$ is defined by (16).

Finally, taking into account (33), expression (34) implies that

$$||\boldsymbol{v_d}(t)||_\infty \leq \triangle_{\max} + \Gamma \frac{T}{2}, \tag{35}$$

is satisfied $\forall t \geq t_1$. Hence, the voltage difference variables $v_{d_1}$, $v_{d_2}$ and $v_{d_3}$ are kept within certain predefined subsets, guaranteeing in this manner the practical stability of system (12)-(14). □

## 5. SYSTEM UNDER VARYING OPERATING CONDITIONS

The controller design step described in Section 4.3 is based on a specific operating point of the system. As a result, the generated look-up table as well as the controller based on the application of the values of this look-up table are only focused on those same operating conditions. Notice that some of the parameters $\mu_{ij}$, $\theta_{ij}$ and $\eta_{ij}$ of the disturbances (15) of the approximated model of the system appear in (27) and (28). Therefore, since these parameters depend on the operating point defined by references $p^*$, $q^*$ and $v_{dc}^*$, their specific values should be evaluated to carry out the second step of the controller design.

Nevertheless, a power converter should be able to work under different scenarios or conditions, not only for an only given operating point. Several approaches are presented in what follows to deal with this consideration. They represent the third design step of the controller, which should be carried out to extend the capability and viability of the proposed controller.

### 5.1. *Third design step: consideration of varying operating conditions*

*5.1.1. First approach* The first approach is based on the choice of the eight couples of control values for $\delta_\gamma$ taking into account not only the areas computed for a particular operating point, but those obtained for a operating range of the system, described by

$$(p^*, q^*, v_{dc}^*) \in \left[p_{min}^*, p_{max}^*\right] \times \left[q_{min}^*, q_{max}^*\right] \times \left[v_{dc_{min}}^*, v_{dc_{max}}^*\right]. \tag{36}$$

Therefore, the second step of the controller design should be slightly modified. With the purpose of creating the look-up table, the eight specific couples of values should be selected from each one of the eight common areas to the whole range of operation. More concretely, these common areas are those regions of the control input space such that the selection and application of a pair of values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ causes the same effect in (19) regardless of the operating point of the system, as long as it is defined within the range (36). In this manner, the chosen values are valid for the whole range of operation of the system.

Hence, considering the procedure described in Remark 2 to obtain the control values to generate the look-up table, in the present case, the functions (27) and (28) should be evaluated many times for each point of the grid. Thus, each function evaluation considers a different operating point defined within the range (36). In this way, (36) should be expressed as a set of operating points to be able to carry out the procedure. Thereby, it is possible to obtain those points of the grid that define the eight common areas to the whole range of operation. Then, for each one of these areas, that particular point located closer to zero and described by a specific pair of values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ is chosen. Finally, the procedure is repeated for other values of $\varepsilon$ with the purpose of optimizing the selected couples of control values. It is important to notice that the whole procedure is worked out off line too. In addition, it should be also mentioned that there might be situations such that the common areas can not be found, so this approach may not provide a solution.

*5.1.2. Second approach* The second approach uses a family of look-up tables. Each one is obtained carrying out the previous steps for a different operating point of the system. Accordingly, this approach is similar to a gain scheduler [49], where the references $p^*$, $q^*$ and $v_{dc}^*$, which are known for the controller, are the scheduling variables. For those operating conditions that have been not considered to generate the family of look-up tables, the controller should evaluate which is the closer specific system operating point of the set of operating points used to generate the look-up tables. The respective look-up table of this specific operating point should be used for this case.

*5.1.3. Third approach* Both previous approaches will allow the proposed controller to be used in varying operating conditions, extending the range of operation of the system. Nevertheless, there exist also some particular situations such that the same look-up table of values for $\delta_\gamma$ calculated for an only system operating point described by

$$\left(p^*, q^*, v_{dc}^*\right) = \left(p_0^*, 0, v_{dc_0}^*\right), \tag{37}$$

can be also used by the controller to ensure voltage balancing for diverse operating conditions. Specifically, these particular situations are described by those operating conditions such that any change in the reference $p^*$ is introduced in the system, but the rest of the system references are kept at their respective values considered during the design of the controller, i.e., at $q^* = 0$ and $v_{dc}^* = v_{dc_0}^*$. In this manner, the off-line design procedure of the controller can be simplified since neither of the two previous approaches should be worked out.

The third and last proposed approach is based on the mathematical analysis of the converter dynamics presented in [33], that leads to the model (12)-(14). This approximated model is derived from the original model [45], replacing some system variables by their approximations (8)-(11) in steady state. Besides, the present approach considers the following assumption.

*Assumption 1*
The system inductances $L$ are small enough such that the effects caused by changes in $p^*$ in the control inputs $\delta_\alpha$ and $\delta_\beta$, devoted to regulate the instantaneous powers, can be neglected in steady state.

When any change in the instantaneous active power reference is introduced in the system, the disturbances (15) are directly proportional to $p^*$, because the phase currents (8) and (9) used to derive the approximated model (12)-(14) are also directly proportional to $p^*$. Notice that the reference $q^*$ is set to zero. Consequently, the computation of manifolds (29) of Section 4.2 is totally independent of $p^*$, so neither the curves nor the areas in the control input space $\delta_{\gamma_2}$– $\delta_{\gamma_1}$ defined in Section 4.3 are affected by changes in $p^*$. Therefore, the specific couples of values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ of the look-up table for $\delta_\gamma$ calculated for the given operating point (37) continue being valid.

However, due to the variation in amplitude and mean value of the disturbances, control law (20) should be redefined in this third approach by

$$\delta_\gamma \;=\; \begin{cases} \delta_{\gamma_1}, \;\text{ if }\; \omega_{31}(t) \;\leq\; \lambda\,(\,\eta_{31} - \mu_{31}\cos(\pi\varepsilon)) \;\text{ and }\; kT \leq t < (k+1)\,T \\ \delta_{\gamma_2}, \;\text{ if }\; \omega_{31}(t) \;>\; \lambda\,(\,\eta_{31} - \mu_{31}\cos(\pi\varepsilon)) \;\text{ and }\; kT \leq t < (k+1)\,T, \end{cases} \tag{38}$$

since both $\mu_{31}$ and $\eta_{31}$ are directly proportional to $p^*$. Parameter $\lambda$ is the constant of proportionality defined by

$$\lambda \;=\; \frac{p_1^*}{p_0^*}, \tag{39}$$

where $p_1^*$ is the new value of $p^*$, and $p_0^*$ is the specific value considered during the design of the controller.

### 5.2. *Implementation of the control law under varying operating conditions*

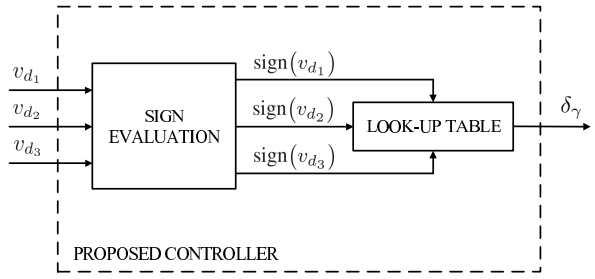
The controller implementation is similar to the one described in Section 4.4, for an only given operating point of the system. Nonetheless, when the third approach described in Section 5.1 to deal with varying operating conditions is considered, the control law to apply is (38). Besides, notice that, when the controller is designed considering the second approach of Section 5.1, steady-state references $p^*$, $q^*$ and $v_{dc}^*$ should be also evaluated together with the signs of the voltage difference variables $v_{d_1}$, $v_{d_2}$ and $v_{d_3}$, each sampling period. They are the scheduling variables used to determine what operating point the system is currently in and to enable the controller to apply a specific couple of constant values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ of the appropriate look-up table. The rest of the implementation process is exactly the same.

Finally, it is worth mentioning that since the number of combinations of the voltage difference variable signs is eight, the look-up table (or each table of the family of look-up tables if the second approach to consider varying operating conditions is used) should be composed of eight couples of values such that each couple corresponds with a particular area of those ones described in Table II. In this way, it is possible to choose the appropriate couple of values to balance the voltages in a correct way at the beginning of each sampling period.

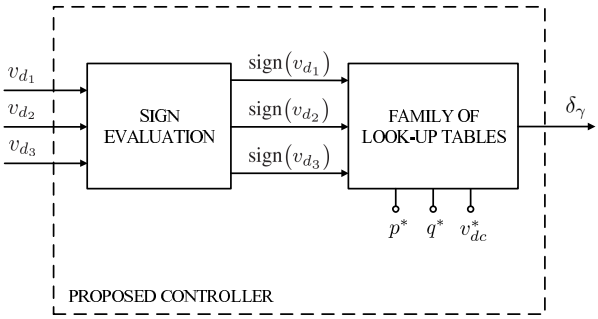
Figure 5 shows the schematic block diagram of the proposed voltage balance controller. The three different approaches considered to deal with varying operating conditions of the system are illustrated in the figure.

## 6. PERFORMANCE EVALUATION

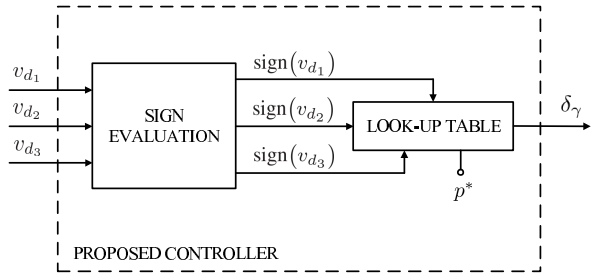
In this section, the evaluation results of the grid-connected converter performance under the voltage balancing method proposed to cope with the problem of the dc-link capacitor voltage imbalance are shown and discussed. To than end, the equations of the dynamic model of the five-level DCC [45] together with the proposed controller have been implemented in Simulink under MATLAB environment, carrying out a simulation. Besides, the controllers proposed in [50] have been included with the goal of regulating the instantaneous powers as well as the total dc-link voltage. It is worth stressing that the simulations are directly based on the continuous model of the five-level DCC, so no switching strategy is required.




(a) First approach considered to deal with varying operating conditions.




(b) Second approach considered to deal with varying operating conditions.




(c) Third approach considered to deal with varying operating conditions.

Figure 5. Schematic block diagram of the proposed voltage balance controller.

The values of the parameters used in the simulation are summarized in Table I. The simulation has been carried out in discrete time with a sampling time set to 200 $\mu$s. It is important to note that the sampling time is lower that the period of the sinusoidal terms of the disturbances, defined by (16). The period (16), which is also known, is used to implement the proposed voltage balance controller, since it determines when should the signs of the variables (17) be evaluated.

The design of the proposed voltage balance controller has been worked out considering only the operating point described in Table I. Consequently, the different design steps of this controller have been carried out in order to operate at the system conditions defined by $p^* = 4083.3$ W, $q^* = 0$ VAr and $v_{dc}^* = 700$ V. Therefore, the specific couples of values $\delta_{\gamma_1}$ and $\delta_{\gamma_2}$ of the look-up table defined in Section 4.3 have been off-line calculated exclusively for these particular system operating conditions. Concerning the other controllers implemented in the system, that is, the instantaneous power and total dc-link voltage controllers, their design parameters are shown in Table IV.

Nevertheless, the simulation considers different and varying operating conditions. Specifically, during the simulation carried out some of the system parameters have been suddenly modified.

Table IV. Design parameters of the instantaneous power controller and of the total dc-link voltage controller.

| Design parameter | Value |
|---|---|
| Instantaneous power controller constants ($k_p$, $k_q$) | $5 \cdot 10^{-7}$ |
| Total dc-link voltage controller proportional gain ($k_{pr}$) | 0.2 |
| Total dc-link voltage controller integral time ($T_{int}$) | 0.1 |

Thereby, the load at the dc link has been changed at $t = 0.3$ s first ($R$ moves from 120 Ω to 80 Ω), so the value of the reference of $p^*$ in steady state has been also abruptly modified. Note that the instantaneous active power reference can be approximated in steady state by

$$p^* \simeq \frac{v_{dc}^{*^2}}{R}. \tag{40}$$

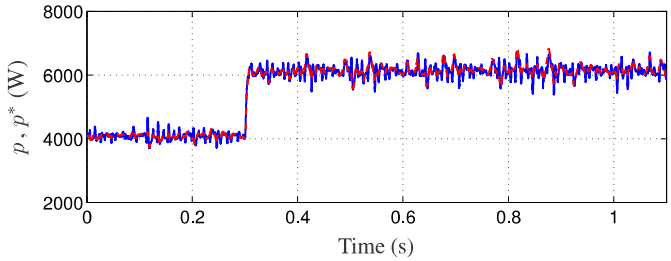
Then, an instantaneous reactive power reference step from $q^* = 0$ VAr to $q^* = 5000$ VAr at $t = 0.8$ s has been introduced in the system. In this way, the third of the approaches described in Section 5.1 to deal with the varying operating conditions has been considered, so the control law defined by (38) has been implemented in this case.

It is worth stressing that the third of the approaches of Section 5.1 is defined to be used only for changes of the steady-state instantaneous active power reference $p^*$, when $q^* = 0$. This situation occurs when the first of the modifications previously mentioned of the system parameters is introduced. Nevertheless, this approach is not defined to be used when the instantaneous reactive power reference step appears in the system. Even so, under these new conditions, the proposed controller has continued using the same look-up table of values. In this way, the present simulation is mainly focused on the analysis of the parametric robustness properties of the controller with respect to changes of the operating conditions, when the controller has not been designed considering the new operating conditions. Thus, the simulations are carried out in order to illustrate that when the changes introduced in the system operating conditions are not extreme (with respect to the operating point used to design the controller), the proposed controller can work correctly without the necessity of considering either the first approach or the second approach detailed in Section 5.1.

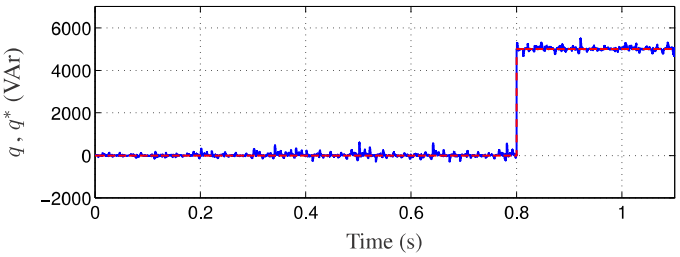
### *6.1. Simulation results*

The evolution of the instantaneous powers and of the total dc-link voltage is illustrated in Fig. 6, when first the load step, and then the instantaneous reactive power step, appear in the system. Beginning with the behavior of the variables $p$ and $q$, both instantaneous active and reactive powers track very quickly their respective references. Concerning the behavior of the total dc-link voltage, it presents a decrease when the load changes, but it subsequently tends correctly towards its reference, achieving $v_{dc}^*$ in a short interval of time. Therefore, the controllers regulate correctly these three variables. Note also that the variables require different time to achieve their respective references, when the load is modified. In this way, the instantaneous power dynamics are much faster than the total dc-link voltage dynamics, so the assumption regarding singular perturbations considered in [33] to derive the approximated model (12)-(14) is well grounded.

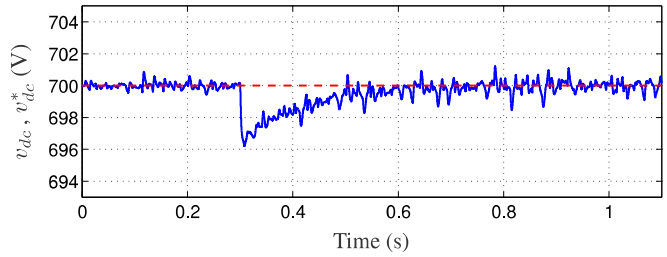
Finally, the time evolution of the voltages of the dc-link capacitors is illustrated in Fig. 7. The capacitor voltages present highest values of their voltage deviations with respect to the capacitor voltage reference $v_c^*$, which is defined by $v_c^* = 175$ V, after the changes of the operating point. Note that since in the five-level DCC there are four capacitors in the dc link, their reference voltages are defined by a quarter of the total dc-link voltage reference, that is, by $v_c^* = 175$ V in the present simulation. Therefore, the deviations are still admissible, because they are lower than 5% of the voltage reference $v_c^*$. In addition, the four variables are kept close to their reference value at all times, so the controller avoids the uncontrolled rise or fall of the capacitor voltages. In view of this, the voltage balancing method proposed in this paper for the three-phase five-level DCC seems to be a robust controller, assuring a solid performance of the converter under varying conditions




(a) Evolution of the instantaneous active power $p$ (solid) and of its reference $p^*$ (dashed).




(b) Evolution of the instantaneous reactive power $q$ (solid), and reference value $q^*$ (dashed) of this variable.



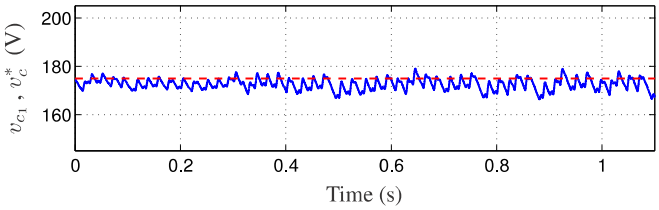

(c) Evolution of the total dc-link voltage $v_{dc}$ (solid), and reference value $v_{dc}^*$ (dashed) of this variable.

Figure 6. Behavior of the instantaneous powers and of the total dc-link voltage, considering varying operating conditions.

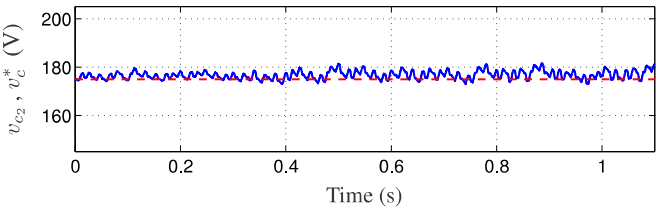
of operation, as long as the changes in the operating point are not extreme. Notice that only the parameter (39) of the control law (38) is proportionally adjusted during the simulation, and only when the load is modified.

*Remark 3*

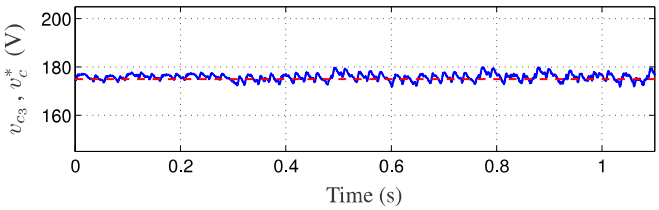
In order to illustrate clearer the requirements for a voltage balance controller, Fig. 8 depicts the evolution of the dc-link capacitor voltages considering the operating point described in Table I, when the controller proposed in this paper is disconnected from $t = 0.1$ s to $t = 0.15$ s. In this figure, it can be seen that the capacitor voltages start to fall or rise in an uncontrolled way at $t = 0.1$. However, when the controller is connected to the system again at $t = 0.15$ s, these voltages are rapidly controlled, beginning to move towards their reference value $v_c^*$ and remaining fluctuating finally around this value. Hence, a good voltage balancing is ensured.



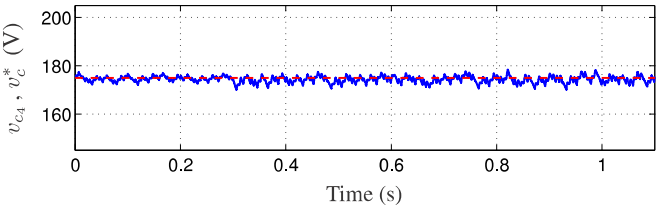

(a) Evolution of $v_{c_1}$ (solid), and reference value $v_c^*$ (dashed) of this variable.




(b) Evolution of $v_{c_2}$ (solid), and reference value $v_c^*$ (dashed) of this variable.




(c) Evolution of $v_{c_3}$ (solid), and reference value $v_c^*$ (dashed) of this variable.

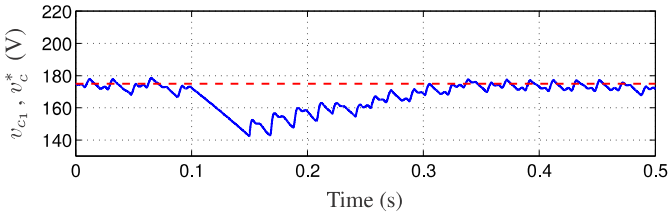



(d) Evolution of $v_{c_4}$ (solid), and reference value $v_c^*$ (dashed) of this variable.

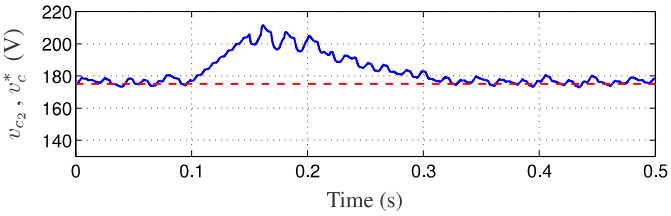
Figure 7. Behavior of the dc-link capacitor voltages under the proposed controller, considering varying operating conditions.

## 7. CONCLUDING REMARKS

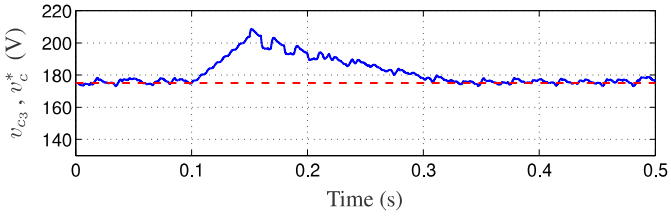
This paper have dealt with the voltage imbalance phenomenon present in the dc-link capacitors of five-level DCCs. To than end, the approach adopted has been based on ensuring the practical stability on the outputs of a nonlinear system under the presence of external disturbances. Then, several steps have been carried out with the goal of designing the controller. A salient feature of the controller is that it exploits the knowledge and the properties of the disturbance patterns to regulate the capacitor voltages, without canceling the disturbances of the system. Although the controller design is not simple, its implementation is not complex and presents lower computational cost than other voltage balancing strategies. Besides, it does not require additional elements, which is a relevant feature. Simulation results have validated the effectiveness of the controller to balance the dc-link capacitor voltages under different and varying operating conditions.



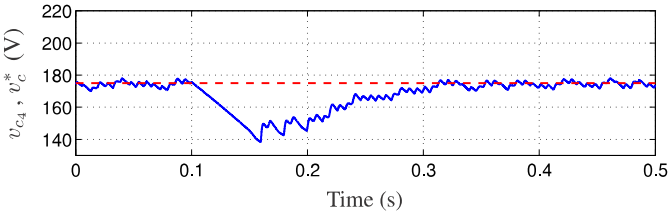

(a) Evolution of $v_{c_1}$ (solid), and reference value $v_c^*$ (dashed) of this variable.




(b) Evolution of $v_{c_2}$ (solid), and reference value $v_c^*$ (dashed) of this variable.




(c) Evolution of $v_{c_3}$ (solid), and reference value $v_c^*$ (dashed) of this variable.




(d) Evolution of $v_{c_4}$ (solid), and reference value $v_c^*$ (dashed) of this variable.

Figure 8. Behavior of the dc-link capacitor voltages, when the proposed controller is disconnected from $t = 0.1$ s to $t = 0.15$ s.

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REFERENCES

1. Abu-Rub H, Holtz J, Rodríguez J, Baoming G. Medium-voltage multilevel converters – state of the art, challenges, and requirements in industrial applications. *IEEE Transactions on Industrial Electronics 2010*; 57(8):2581–2596.
2. Rodríguez J, Bernet S, Wu B, Pontt JO, Kouro S. Multilevel voltage-source-converter topologies for industrial medium-voltage drives. *IEEE Transactions on Industrial Electronics 2007*; 54(6):2930–2945.
3. Kouro S, Malinowski M, Gopakumar K, Pou J, Franquelo LG, Wu B, Rodríguez J, Pérez MA, León JI. Recent advances and industrial applications of multilevel converters. *IEEE Transactions on Industrial Electronics 2010*; 57(8):2553–2580.
4. Rodríguez J, Lai JS, Peng FZ. Multilevel inverters: a survey of topologies, controls, and applications. *IEEE Transactions on Industrial Electronics 2002*; 49(4):724–738.

5. Rodríguez J, Franquelo LG, Kouro S, León JI, Portillo RC, Prats MM, Pérez MA. Multilevel converters: an enabling technology for high-power applications. *Proceedings of the IEEE 2009*; 97(11):1786–1817.
6. Franquelo LG, Rodríguez J, León JI, Kouro S, Portillo R, Prats MM. The age of multilevel converters arrives. *IEEE Industrial Electronics Magazine 2008*; 2(2):28–39.
7. Marchesoni M, Tenca P. Theoretical and practical limits in multilevel MPC inverters with passive front ends. *Proceedings of the 9th European Conference on Power Electronics and Applications - EPE'01*, Graz, Austria, 2001; 1–12.
8. Saeedifard M, Iravani R, Pou J. Analysis and control of dc-capacitor-voltage-drift phenomenon of a passive front-end five-level converter. *IEEE Transactions on Industrial Electronics 2007*; 54(6):3255–3266.
9. Menzies RW, Steimer P, Steinke JK. Five-level GTO inverters for large induction motor drives. *IEEE Transactions on Industry Applications 1994*; 30(4):938–944.
10. Choi NS, Cho JG, Cho CH. A general circuit topology of multilevel inverter. *Proceedings of the 22nd Annual IEEE Power Electronics Specialists Conference - PESC'91*, Cambridge, Massachusetts, USA, 1991; 96–103.
11. Shukla A, Ghosh A, Joshi A. Control schemes for dc capacitor voltages equalization in diode-clamped multilevel inverter-based DSTATCOM. *IEEE Transactions on Power Delivery 2008*; 23(2):1139–1149.
12. Shu Z, He X, Wang Z, Qiu D, Jing Y. Voltage balancing approaches for diode-clamped multilevel converters using auxiliary capacitor-based circuit. *IEEE Transactions on Power Electronics 2013*; 28(5):2111–2124.
13. Newton C, Sumner M. Novel technique for maintaining balanced internal dc link voltages in diode clamped five-level inverters. *IEE Proceedings Electric Power Applications 1999*; 146(3):341–349.
14. León JI, Franquelo LG, Portillo RC, Prats MM. Dc-link capacitors voltage balancing in multilevel four-leg diode-clamped converters. *Proceedings of the 31th Annual Conference of the IEEE Industrial Electronics Society - IECON'05*, Raleigh, North Carolina, USA, 2005; 1254–1259.
15. Marchesoni M, Tenca P. Diode-clamped multilevel converters: a practicable way to balance DC-link voltages. *IEEE Transactions on Industrial Electronics 2002*; 49(4):752–765.
16. Minshull SR, Bingham CM, Stone DA, Foster MP. Compensation of nonlinearities in diode-clamped multilevel converters. *IEEE Transactions on Industrial Electronics 2010*; 57(8):2651–2658.
17. Pan Z, Peng FZ, Corzine KA, Stefanovic VR, Leuthen JM, Gataric S. Voltage balancing control of diode-clamped multilevel rectifier/inverter systems. *IEEE Transactions on Industry Applications 2005*; 41(6):1698–1706.
18. Ishida T, Matsuse K, Miyamoto T, Sasagawa K, Huang L. Fundamental characteristics of five-level double converters with adjustable dc voltages for induction motor drives. *IEEE Transactions on Industrial Electronics 2002*; 49(4):775–782.
19. Saeedifard M, Iravani R, Pou J. A space vector modulation strategy for a back-to-back five-level HVDC converter system. *IEEE Transactions on Industrial Electronics 2009*; 56(2);452–466.
20. Pan Z, Peng FZ. A sinusoidal PWM method with voltage balancing capability for diode-clamped five-level converters. *IEEE Transactions on Industry Applications 2009*; 45(3):1028–1034.
21. Marchesoni M, Vaccaro L. Operating limits in multilevel MPC inverters with active front ends. *Proceedings of the International Symposium on Power Electronics, Electrical Drives, Automation and Motion - SPEEDAM'10*, Pisa, Italy, 2010; 192–197.
22. Saeedifard M, Iravani R, Pou J. Control and dc-capacitor voltage balancing of a space vector-modulated five-level STATCOM. *IET Power Electronics 2009*; 2(3):203–215.
23. Botao M, Congwei L, Yang Z, Fahai L. New SVPWM control scheme for three-phase diode clamping multilevel inverter with balanced dc voltages. *Proceedings of the 28th Annual Conference of the IEEE Industrial Electronics Society - IECON'02*, Seville, Spain, 2002; (2):903–907.
24. Khajehoddin SA, Bakhshai A, Jain PK. A simple voltage balancing scheme for m-level diode-clamped multilevel converters based on a generalized current flow model. *IEEE Transactions on Power Electronics 2008*; 23(5):2248–2259.
25. Shu Z, Ding N, Chen J, Zhu HF, He X. Multilevel SVPWM with dc-link capacitor voltage balancing control for diode-clamped multilevel converter based STATCOM. *IEEE Transactions on Industrial Electronics 2013*; 60(5):1884–1896.
26. Busquets-Monge S, Alepuz S, Bordonau J, Peracaula J. Voltage balancing control of diode-clamped multilevel converters with passive front-ends. *IEEE Transactions on Power Electronics 2008*; 23(4):1751–1758.
27. Busquets-Monge S, Alepuz S, Rocabert J, Bordonau J. Pulsewidth modulations for the comprehensive capacitor voltage balance of n-level three-leg diode-clamped converters. *IEEE Transactions on Power Electronics 2009*; 24(5):1364–1375.
28. Borghetti G, Carpaneto M, Marchesoni M, Tenca P, Vaccaro L. A new balancing technique with power losses minimization in diode-clamped multilevel converters. *Proceedings of the 12th European Conference on Power Electronics and Applications - EPE'07*, Aalborg, Denmark, 2007; 1–10.
29. Akagi H, Fujita H, Yonetani S, Kondo Y. A 6.6-kV transformerless STATCOM based on a five-level diode-clamped PWM converter: system design and experimentation of a 200-V 10-kVA laboratory model. *IEEE Transactions on Industry Applications 2008*; 44(2):672–680.
30. Hatti N, Hasegawa K, Akagi H. A 6.6-kV transformerless motor drive using a five-level diode-clamped PWM inverter for energy savings of pumps and blowers. *IEEE Transactions on Power Electronics 2009*; 24(3):796–803.
31. Ishida T, Matsuse K, Sugita K, Huang L, Sasagawa K. Dc voltage control strategy for a five-level converter. *IEEE Transactions on Power Electronics 2000*; 15(3):508–515.
32. Qin J, Saeedifard M. Capacitor voltage balancing of a five-level diode-clamped converter based on a predictive current control strategy. *Proceedings of the 26th Annual IEEE Applied Power Electronics Conference and Exposition - APEC'11*, Fort Worth, Texas, USA, 2011; 1656–1660.
33. Umbría F, Gómez-Estern F, Gordillo F, Salas F. Voltage balancing in five-level diode-clamped power converters. *Proceedings of the 9th IFAC Symposium on Nonlinear Control Systems - NOLCOS'13*, Toulouse, France, 2013; 365–370.
34. Khalil HK. *Nonlinear systems* (3rd edition). Prentice Hall: Upper Saddle River, NJ, USA, 2002.

35. Isidori A. *Nonlinear control systems II*. Springer-Verlag: London, England, UK, 1999.
36. Isidori A, Byrnes CI. Output regulation of nonlinear systems. *IEEE Transactions on Automatic Control 1990*; 35(2):131–140.
37. Nikiforov VO. Adaptive non-linear tracking with complete compensation of unknown disturbances. *European Journal of Control 1998*; 4(2):132–139.
38. Ding Z. Asymptotic rejection of general periodic disturbances in output-feedback nonlinear systems. *IEEE Transactions on Automatic Control 2006*; 51(2):303–308.
39. Ding Z. Output regulation of uncertain nonlinear systems with nonlinear exosystems. *IEEE Transactions on Automatic Control 2006*; 51(3):498–503.
40. Li R, Khalil HK. Nonlinear output regulation with adaptive conditional servocompensator. *Automatica 2012*; 48(10):2550–2559.
41. Dong X, Zhao J. Output regulation for a class of switched nonlinear systems: an average dwell-time method. *International Journal of Robust and Nonlinear Control 2013*; 23(4):439–449.
42. Ornelas-Téllez F, Sánchez EN, Loukianov AG, Rico JJ. Robust inverse optimal control for discrete-time nonlinear system stabilization. *European Journal of Control 2014*; 20(1):38–44.
43. LaSalle JP, Lefschetz S. *Stability by Liapunov's direct method with applications*. Academic Press: New York, NY, USA, 1961.
44. Lakshmikantham V, Leela S, Martynyuk AA. *Practical stability of nonlinear systems*. World Scientific: Singapore, 1990.
45. Portillo R, Carrasco JM, León JI, Galván E, Prats MM. Modeling of five-level converter used in a synchronous rectifier application. *Proceedings of the 36th Annual IEEE Power Electronics Specialists Conference - PESC'05*, Recife, Brazil, 2005; 1396–1401.
46. Akagi H, Kanazawa Y, Nabae A. Generalized theory of the instantaneous reactive power in three-phase circuits. *Proceedings of the International Power Electronics Conference - JIEE-IPEC'83*, Tokyo, Japan, 1983; 1375–1386.
47. Umbría F, Gordillo F, Gómez-Estern F, Salas F, Portillo RC, Vázquez S. Voltage balancing in three-level neutral-point-clamped converters via Luenberger observer. *Control Engineering Practice 2014*; 25:36–44.
48. Umbría F, Gordillo F, Salas F, Aracil J, Gómez-Estern F. Asymptotic rejection of sinusoidal disturbances based voltage balance control in back-to-back power converters. *International Journal of Robust and Nonlinear Control 2013*; 1–21 (http://dx.doi.org/10.1002/rnc.3036).
49. Rugh WJ, Shamma JS. Research on gain scheduling. *Automatica 2000*; 36(10):1401–1425.
50. Vázquez S, Sánchez JA, Carrasco JM, León JI, Galván E. A model-based direct power control for three-phase power converters. *IEEE Transactions on Industrial Electronics 2008*; 55(4):1647–1657.