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# Single bend wiring on surfaces

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#### Abstract

The following problem of rectilinear routing is studied: given pairs of points on a surface and a set of permissible orthogonal paths joining them, whether is it possible to choose a path for each pair avoiding all intersections. We prove that if each pair has one or two possible paths to join it, then the problem is solvable in quadratic time, and otherwise it is NP-complete. From that result, we will obtain that the problem of finding a surface of minimum genus on which the wires can be laid out with only one bend is NP-hard. © 2002 Elsevier Science B.V. All rights reserved.

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## 1. Introduction

Orthogonal layouts are used in many applications of computer science as circuit schematics, data flow diagrams in Software Engineering or entity relationships diagrams [1,2]. This fact has attracted the attention of many authors and numerous results have been obtained about orthogonal drawings [3,6,9-12].

The problem of connecting pairs of points on the plane using orthogonal paths with at most one bend was studied by Raghavan et al. [11]. A pair of points to be connected is called a *wire*. They develop an  $O(m^2)$  algorithm to determine whether or not a set of *m* point pairs can be wired in this manner on the plane. The paths are not allowed to cross, hence most wire sets cannot be wired in a rectilinear fashion on the plane. In this case, the authors proved that the problem of determining a maximum cardinality subset of wires which can be laid out in a single bend fashion on the plane is NP-hard.

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In order to extend the results of [11] to realistic constrains on circuit routing, some other works have appeared [4,7]. In many applications, the connections are constructed using more than one layout. This fact together with the results about the plane lead to the problem on other surfaces.

Observe that, as it is pointed out in [8] layout problem is a multiobjective optimization problem, and there are many cost functions that are of interest in layout. Among those functions we can cite two: *via count* and the *maximum number of bends per wire*. A via is a change of layer in a wire and usually introduces electrical instabilities that decrease the yield, additionally, the use of vias increase the difficulties of some manufacturing process. And a bend in a wire has adverse effects on the delay and other electrical properties of the wire. Although, vias and bends are related, in general they do not need to be correlated.

To allow only one bend for each wire has in addition some extra advantages on other cost functions, since wires with only one bend have always minimum length and all wires are represented in a minimum area. But, in this case, vias are unavoidable. In some sense, we address here the problem of minimizing vias in the following way, each time that two wires intersect, we can avoid that intersection by introducing a via. As far as a via introduces a hole in a printed board that presents typically two faces we can model our problem as a single bend wiring on a surface, of course to minimize the number of vias is equivalent to asking for the problem of minimizing the genus of the surface where we are representing our pairs of points. And we will prove that this is a NP-hard problem.

This paper is structured in the following way. In the next section, we will model in an adequate way our problem. Then, we will prove in the third section that if we use only two path between each pair of points, then the problem is solvable in polynomial time. The fourth section is devoted to the general problem, and we include a section with some concluding remarks and open problems.

# 2. Modeling single bend wiring on surfaces

First of all, an adequate representation of a surface of genus g is needed to connect pairs of points orthogonal paths, namely, a system of orthogonal lines must be defined on the surface. The planar representation of the surface of genus 1 (the torus) is a rectangle whose parallel sides are identified. This rectangle will be the external rectangle of the standard orthogonal surfaces that are constructed as follows: The standard orthogonal surface of genus g [6] is obtained by the deletion of g - 1 small rectangles or *windows* in the interior of the external rectangle (different positions for the same number of windows lead to homeomorphic surfaces). The sides of all rectangles (external rectangle and windows) are parallel and the opposite sides of each window are also identified. In this way, two distinguished directions are defined, the horizontal (= direction of the parallels) and the vertical direction (= direction of the meridians), respectively. Note that these directions are parallel to the sides of the external rectangle

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Fig. 1. The standard orthogonal surface of genus g and its orthogonal system.

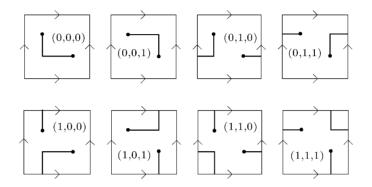


Fig. 2. The eight possible single bend wirings on a surface of genus g.

(see Fig. 1). Hence, in order to obtain such a representation of a surface it is necessary to fix one parallel and one meridian forming the sides of the external rectangle. They are called *external parallel and meridian*.

We can fix a coordinate system in which the axes are the external parallel and meridian, x- and y-axis respectively, and the origin is the point in the bottom left-hand corner of the standard orthogonal surface. In this way, any point or window on the surface may be specified by its x- and y-coordinates. Notice that a surface is defined by the number and positions of its windows.

An orthogonal path is made up of horizontal and vertical segments. These paths are called *rectilinear wirings* or *layouts*. The number of bends of each rectilinear path can be different, but, as we mentioned in the Introduction, from a practical point of view, there are many applications where it is necessary to limit to one the number of them on each rectilinear connection. When the wiring is restricted such that no wire has more than one bend, it is called a *single bend wiring*.

Given a pair of points on the plane, there are at most two ways to wire them using only one bend, lower and upper wirings (see Fig. 2 (0,0,0) and (0,0,1)); Fig. 2(0,\*,\*) corresponds to the possible single bend wirings for two points on the cylinder. In general, there are at most eight wirings connecting a wire on a surface of genus  $g \ge 1$  using only one bend (Fig. 2). But, it is very common to face situations where no all possible wirings are permitted, typically by the situation of some components that obstruct those wirings.

Each single bend wiring is identified by three Boolean variables (vc, hc, d) in the following way: The variables vc and hc indicate the possible intersection between the rectilinear layout and the external parallel and meridian respectively. Set vc (hc) to true if and only if the single bend wiring intersects with the external parallel (meridian). For each single bend wiring, the variable d indicates if the segment adjacent to the upper point wire is horizontal or vertical. Set d to true if and only if this segment is horizontal. Fig. 2 shows the eight possible wirings and the corresponding values of the variables. The single bend layouts with vc or hc being true are called *essential wirings*.

Below, we pose the general problem studied in this article, distinguishing whether the connections are forced to be constructed along fixed layouts or all the wirings are permitted.

Single bend wiring on surfaces with fixed layouts (*n*-sbws):

*Instance*: Surface  $\mathcal{S}$ , a wire set  $\mathcal{W}$  on  $\mathcal{S}$  and at most *n* possible single bend wirings for each wire.

Question: Can  $\mathscr{W}$  be single bend wired on  $\mathscr{S}$  using the given wirings and without intersection between the layouts of different wires?

For the sake of simplicity, a wire with n possible single bend wirings will be called an *n*-wire.

### Single bend wiring on surfaces (SBWS):

Instance: Surface  $\mathscr{S}$  and a wire set  $\mathscr{W}$  on  $\mathscr{S}$ .

Question: Can  $\mathcal{W}$  be single bend wired on  $\mathscr{S}$  without intersection between the layouts of different wires?

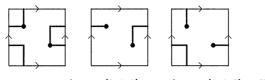
As the maximum number of single bend wirings on any surface is eight, for the sBws problem, each wire can be single bend wired using, exactly eight different layouts.

In Section 3, we show that the problem 2-sBws can be solved efficiently for arbitrary surfaces. The algorithm has time complexity  $O(m^2)$ , where *m* is the number of wires in the instance. In Section 4, we prove that the *n*-sBws problem for  $n \ge 3$  is NP-complete for arbitrary surfaces. Too, the NP-completeness of the sBws problem is established and, hence, finding a surface of minimum genus on which a given wire set can be single bend wired is NP-hard.

# 3. Feasibility of 2-sbws

In this section, we outline how to determine in polynomial time whether or not a given 2-wire set  $\mathcal{W}$  on a surface  $\mathcal{S}$  of genus g can be single bend wired feasibly (i.e., without intersections). Raghavan et al. [11] solved this problem on a plane layer, where at most two possible single bend wirings for each wire exist. On surfaces of higher genus, the number of possible layouts is increased. On the cylinder there are at most four possible layouts and on the torus and surfaces of higher genus there are at most eight layouts for each wire. In these cases, there are more than a single possibility for choosing the two allowed layouts. The inspection of the intersection of layouts on the plane considered in [11] can be applied only in few cases and new cases appear.

30



layout  $(0,1,1) \rightarrow u_i$  layout  $(1,1,0) \rightarrow \overline{u_i}$ 

Fig. 3. A wire on the torus with two prefixed layouts and the assignment of truth values for each layout.

We consider all m(m-1)/2 pairs of wires in  $\mathcal{W}$ , where m is the cardinality of  $\mathcal{W}$ . For each pair we have three options:

- (a) The two wires cannot be laid out feasibly. Then, the wire set  $\mathscr{W}$  cannot be single bend wired feasibly on the surface  $\mathscr{S}$ . If this case occurs for a pair, the answer for the 2-sbws given instance is no.
- (b) There are no intersections between layouts of two wires.
- (c) There are intersections between some layouts of both wires but there are one or more feasible combinations of layouts.

The information of a 2-sBWS instance can be shown as a *Krom formula* which is satisfiable if and only if the corresponding wire set can be laid out (without intersection) in single bend fashion. A *Krom formula* (or 2-CNF formula) is a Boolean expression which is in conjunctive normal form (CNF) and contains at most two literals per clause.

The codification process in a logic formula is done as follows: we associate a Boolean variable  $u_i$  to each wire  $w_i$  in  $\mathcal{W}$ . The truth value assigned to the variable corresponds to the layout of the wire, say true for the layout with smallest label (in the lexicographic ordering) (vc, hc, d), now called the *lower layout*, and false for the layout with biggest label (the *higher layout*). An example is shown in Fig. 3. vc, hc and d are the variables associated to the layout, as described in the introduction (see Fig. 2). Note that this assignment is compatible with the assignment done for the plane in [11] and, in this case, the words *higher* and *lower* refer to the geometrical location of the layouts.

Each interaction between two wires can be turned into a Boolean formula inspecting the possible crossings between layouts. There are sixteen classes of interaction:

- (1)  $\mathbf{u}_i \wedge \bar{\mathbf{u}}_i$ . Infeasibility. This corresponds to case (a) mentioned above.
- (2)  $\mathbf{u}_i \vee \bar{\mathbf{u}}_i$ . No intersections. This corresponds to case (b) mentioned above.
- (3)  $\mathbf{u}_i$ . The *lower layout* for  $w_i$  does not cross any layout from  $w_j$ , but the *higher layout* for  $w_i$  is infeasible.
- (4)  $\mathbf{u}_{j}$ . Symmetric to case (3) when *i* is replaced by *j*.
- (5)  $\mathbf{\bar{u}}_i$ . Symmetric to case (3) when the *lower layout* is replaced by the *higher layout*.
- (6)  $\mathbf{\tilde{u}}_i$ . Symmetric to case (4) when the *lower layout* is replaced by the *higher layout*.
- (7)  $\mathbf{u}_i \vee \bar{\mathbf{u}}_j$ . The *lower layout* for  $w_i$  does not intersect any layout of  $w_j$ , and the *higher layout* for  $w_j$  does not cross any layout of  $w_i$ . The *higher layout* of  $w_i$  and the *lower layout* of  $w_j$  can be laid out simultaneously.

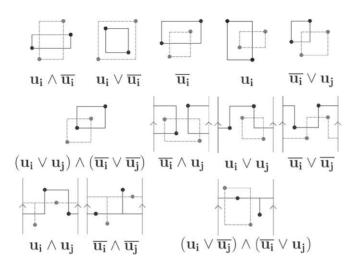


Fig. 4. All possible classes of interaction up to symmetries. The discontinuous lines correspond to the index j.

- (8)  $\mathbf{u}_i \vee \mathbf{u}_i$ . Symmetric to case (7) when *i* is replaced by *j*.
- (9)  $(\mathbf{u}_i \vee \mathbf{u}_j) \wedge (\bar{\mathbf{u}}_i \vee \bar{\mathbf{u}}_j)$ . Two possible connections. The *higher layout* for one of the two wires and the *lower layout* for the other one.
- (10)  $\mathbf{u}_i \wedge \bar{\mathbf{u}}_j$ . Only the *lower layout* for  $w_i$  and the *higher layout* for  $w_j$  are feasible simultaneously.
- (11)  $\mathbf{\bar{u}}_i \wedge \mathbf{u}_i$ . Symmetric to case (10) when *i* is replaced by *j*.
- (12)  $\mathbf{u}_i \vee \mathbf{u}_j$ . The *lower layouts* are both feasible and there are intersection between the *higher layouts*.
- (13)  $\mathbf{\bar{u}}_i \vee \mathbf{\bar{u}}_j$ . The *higher layouts* are both feasible and there are intersection between the *lower layouts*.
- (14)  $\mathbf{u}_i \wedge \mathbf{u}_j$ . Only the *lower layouts* are feasible simultaneously.
- (15)  $\mathbf{\bar{u}}_i \wedge \mathbf{\bar{u}}_j$ . Only the *higher layouts* are feasible simultaneously.
- (16)  $(\mathbf{u}_i \lor \bar{\mathbf{u}}_j) \land (\bar{\mathbf{u}}_i \lor \mathbf{u}_j)$ . In this case there are two possibilities. Either both wires have to be laid out using the *higher layout* or using both the *lower layout*.

Note that classes (1)–(9) of interactions can appear on the plane [11] and (1)–(16) can appear on the cylinder and on surfaces of higher genus. Note also that these sixteen clauses are all possible Boolean 2-clauses with at most two variables (Fig. 4).

Each pair of points can be connected using eight possible single bend wirings on a surface of genus g (Fig. 2). Then, we have 28 possible choices of two layouts for each 2-wire. Two pairs of points can be placed in 72 different relative positions, up to vertical symmetries between the pairs. Thus, there are 56 448 ( $28 \times 28 \times 72$ ) different pairs of 2-wires.

Using a simple computer routine, all the 56448 different pairs of wires on a surface of arbitrary genus have been turned into Boolean formulae. Note that a same pair can produce different clauses on different surfaces (see Fig. 5).

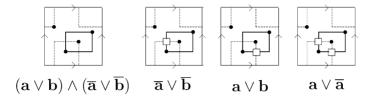


Fig. 5. Different clauses for the same wiring on different surfaces.

When all the interactions are turned into Boolean formulae, the result is a *Krom formula* with at most two clauses in each relation.

Theorem 1. The 2-sbws problem is solvable in quadratic time.

**Proof.** The m(m-1)/2 interaction relations between pairs of 2-wires determine the same number of Boolean formulae which must be satisfied simultaneously. Then, the conjunction of all these formulae corresponds to the entire set of pairs of 2-wires. Obviously, it is possible to exclude those formulae corresponding to case (2), because they are tautologies. This gives a *Krom formula* containing at most  $O(m^2)$  clauses. One can determine whether a *Krom formula* is satisfiable in linear time in the number of clauses and find within the same asymptotic time a satisfying truth assignment if one exists [5].

Hence, in our case it can be decided in  $O(m^2)$  time whether there exists a satisfying truth assignment and in the affirmative case such an assignment can be found in  $O(m^2)$  time.

If a satisfying truth assignment can be found, it is a simple task to construct the equivalent wire layout for the wire set  $\mathcal{W}$ .  $\Box$ 

## 4. Single bend wires on surfaces of minimum genus

Given a wire set, Raghavan et al. [11] developed an  $O(m^2)$  algorithm to determine whether or not a set of *m* wires can be single bend wired on a plane layer. For those wire sets that cannot be single bend wired on the plane, the question of determining a maximum cardinality subset such that all their wires can be laid out in single bend fashion on the plane is considered. These authors established the NP-hardness of this second problem.

Another option for such wire sets could be to introduce vias or layouts on surfaces of higher genus. As we have indicated in the introduction, there are at most two ways to wire a pair of points on the plane using only one bend. On an arbitrary surface, for a wire there are eight possible single bend layouts.

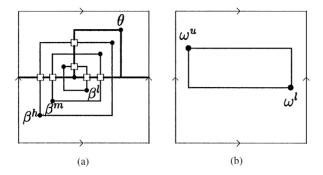


Fig. 6. (a) Clause assembly  $\alpha$ , (b) variable wire  $\omega$ .

In the previous section, we have seen that it is possible to solve in polynomial time single bend wiring on surfaces when only two layouts for each wire are permitted (2-wires). Now, we will observe that the situation changes drastically if three or more wiring are permitted for each wire.

In this section, we prove the completeness of two problems: n-sBws for  $n \ge 3$  and sBws. Note that the result for one problem is not an immediate consequence of the other one because, for each wire there are at most n possible wirings for the n-sBws problem and exactly eight wirings for the sBws problem. Observe that an optimization problem related with sBws is to find a surface of minimum genus on which the wires can be laid out with only one bend. Obviously, if we can give an answer to this problem in polynomial time, we will know to solve the sBws problem in polynomial time. Hence, the problem of determining the minimum genus of a surface on which a wire set can be laid out in single bend fashion is NP-hard.

# Theorem 2. The 3-sbws problem is NP-complete.

**Proof.** 3-sBWS is readily seen to be solvable in nondeterministic polynomial time, i.e., 3-sBWS is in NP. Thus, in order to prove the NP-completeness of the problem 3-sBWS, it suffices to transform an NP-complete problem to ours. In order to do this we consider the well-known NP-complete problem 3-sATISFIABILITY (3-SAT). Let  $U = \{u_1, u_2, ..., u_p\}$  be a set of variables and let  $C = \{c_1, c_2, ..., c_q\}$  be a set of clauses making up an arbitrary instance  $\mathcal{R}$  of 3-sAT. Corresponding to  $\mathcal{R}$ , we construct a 3-sBWS instance  $\mathcal{T}$  as follows:

Step 1. Each clause  $c_i$  will be represented by a *clause assembly*  $\alpha_i$ , shown in Fig. 6(a) (for each wire, only the permitted layouts are pictured). The three literals of each clause are indexed following the enumeration of its corresponding variables (it can be supposed no clause contains the same complemented and non-complemented variable). With this order, let  $l_i^l$ ,  $l_i^m$  and  $l_i^h$  be the lowest, medium and highest index literals of the clause  $c_i$ , respectively. The literal wires  $\beta_i^l$ ,  $\beta_i^m$  and  $\beta_i^h$  of the clause assembly  $\alpha_i$  are associated to  $l_i^l$ ,  $l_i^m$  and  $l_i^h$ , respectively.

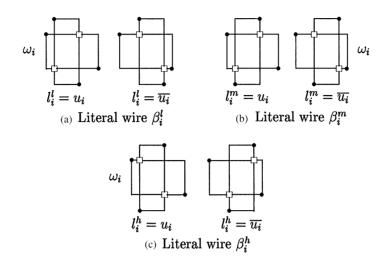


Fig. 7. Variable wire  $\omega_i$  and literal wires  $\beta_i$ .

Place the clause assemblies  $\alpha_1, \ldots, \alpha_q$  from top to bottom of the surface such that • if i < j then the literal wires  $\beta_i^l$ ,  $\beta_i^m$  and  $\beta_i^h$  are on the left of  $\beta_j^l$ ,  $\beta_j^m$  and  $\beta_j^h$ ; • there is no any meridian intersecting literal wires of different clauses.

The position of the lowest points of  $\beta^l$ ,  $\beta^m$  and  $\beta^h$  will be determined in Step 3.

For each clause in  $\mathcal{R}$ , the genus of the surface of  $\mathcal{T}$  is increased 6 units.

Step 2. Each variable  $u_i$  will be represented by a variable wire  $\omega_i$ , shown in Fig. 6(b). Let  $\omega_i^u$  and  $\omega_i^l$  be the upper and lower points of the variable wire, respectively. Place the variable wires  $\omega_1, \ldots, \omega_p$  under the clause assemblies, from  $\omega_1$  to  $\omega_p$ , such that

- $w_i^u$  is on the left of  $\beta_1^h$  and  $w_i^l$  is on the right of  $\beta_a^h$ , where i = 1, ..., p;
- $\omega_i$  and  $\omega_j$   $(i \neq j)$  do not intersect.

Step 3. Finally, we fix the position of the lowest points of the literal wires as shown in Fig. 7. The different situations depend on the type of literal wire, i.e.,  $\beta^l$ ,  $\beta^m$  or  $\beta^h$ , and whether or not the corresponding literal is a complemented one. In any case, the lowest points of the literal wires are placed under their respective variable wires. The genus of the surface is increased 2 units for each literal wire to place, hence 6q units.

In order to place these wires as Fig. 7 determines, the genus of the surface is increased to avoid intersections between literal wires and the posterior clauses assemblies and anterior variables wires. If literal  $l_i$  belongs to the clause  $c_j$  then the genus of the surface, that is 12q + 1, is increased 2(q - j) units to avoid intersections between  $\beta_i$  and the clause assemblies  $\alpha_{j+1}, \ldots, \alpha_q$ . In addition, it is necessary to add 4(i-1) units corresponding to  $\omega_1, \ldots, \omega_{i-1}$ .

This completes the construction of the 3-sews instance  $\mathcal{T}$  corresponding to  $\mathcal{R}$ . It is easily verified that the genus of the surface  $\mathcal{S}$  and the number of wires in  $\mathcal{T}$  constructed is polynomial in p and q.

Suppose that  $\mathscr{R}$  is satisfiable. Let  $u_i = z_i$ ,  $1 \leq i \leq p$ , be a truth assignment for which all the clauses in *C* are satisfied. A layout of the wires in  $\mathscr{T}$  is obtained as follows:

- (1) The assignment of the literal determines the layout of each clause assembly. If  $l^{l}(l^{h})$  is true then  $\beta^{l}(\beta^{h})$  is laid out using the upper layout. If it is false, the lower layout is used. On the contrary, if  $l^{m}$  is true,  $\beta^{m}$  is laid out using the lower wiring. If it is false, the upper layout is used. For each  $\alpha_{i}$ , observe that each *false wiring* (wiring associated to the false value) intersect with only one segment of the layouts of  $\theta_{i}$ .
  - Since  $u_i = z_i$ ,  $1 \le i \le p$ , satisfies all the clauses, at least one literal in each clause is true under this assignment. Hence, at least one false wiring is not used for the layout of the literal wires, which allows one of the layouts of  $\theta_i$  to be free.
- (2) For the variable wires, if  $z_i =$ true, then the wire  $\omega_i$  is laid out using the upper layout. If  $z_i =$ false, the lower layout is used. The wirings of variable wires and literal wires do not intersect with this choice as can be seen from Fig. 7.

Next, suppose that  $\mathscr{T}$  can be laid out on  $\mathscr{S}$ . Set  $u_i$  to true, if and only if, the upper wiring is used for the layout of  $\omega_i$ . From this assignment, it is easy to verify that the choice of the upper layouts of  $\beta^l$  and  $\beta^h$  and the lower one of  $\beta^m$  forces the truth value for  $l^l$ ,  $l^h$  and  $l^m$ , respectively (see Fig. 7). In each clause assembly there are three possible wirings for the wire  $\theta$ . It is easy to see by inspection that each one of these three possibilities forces the layout of a literal with truth value. Hence, this assignment satisfies all the clauses of the instance of 3-sat.  $\Box$ 

Fig. 8 shows an example for the set of variables  $U = \{u_1, u_2, u_3, u_4\}$  and the clauses  $C = \{c_1, c_2, c_3\}$  with  $c_1 = \{u_1, \bar{u}_2, u_3\}$ ,  $c_2 = \{\bar{u}_1, u_3, u_4\}$  and  $c_3 = \{u_1, u_2, \bar{u}_4\}$ .

Fig. 9 depicts a layout of the wires of the example (see Fig. 8) which corresponds to the truth assignment  $u_1 =$  true,  $u_2 =$  false,  $u_3 =$  false and  $u_4 =$  true.

As an immediate consequence of Theorem 2, the following corollary is obtained:

#### **Corollary 3.** The n-sbws problem is NP-complete for $n \ge 3$ .

Below, the NP-completeness of the sBws problem (without restrictions as to the number of permitted layouts) is proved. Note that this result cannot be followed directly from the NP-completeness of the n-sBws problem.

# Theorem 4. The sBws problem is NP-complete.

**Proof.** sBWs is easily seen to be in NP.

Again, we consider the NP-complete problem 3-SAT.

The main steps to construct an sBws instance are similar to those which we have seen in Theorem 2, but as we need to control the number of layouts of each wire (now all the wirings are permitted for each wire), three additional wires are placed as Fig. 10 indicates, forming the *blocker assembly*. There are two possible layouts for the

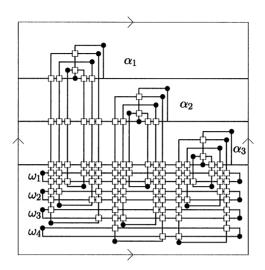


Fig. 8. An example of Theorem 2 for the set of variables  $U = \{u_1, u_2, u_3, u_4\}$  and the clauses  $C = \{c_1, c_2, c_3\}$  with  $c_1 = \{u_1, \bar{u}_2, u_3\}, c_2 = \{\bar{u}_1, u_3, u_4\}$  and  $c_3 = \{u_1, u_2, \bar{u}_4\}$ .

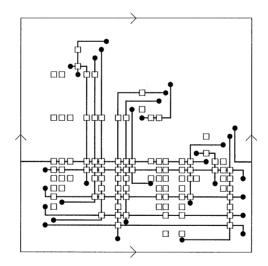


Fig. 9. Layout of the wires in Fig. 8.

wire  $\lambda$ , on the contrary, the only possible layouts of the wires  $\mu$  and v are depicted in Fig. 10(a). The symbolic form for the blocker assembly is shown in Fig. 10(b). When a layout has been blocked by the blocker assembly, only the remaining feasible layouts will be shown.  $\Box$ 

Now, the clause assemblies are constructed as Fig. 11 shows and are placed starting below  $\mu_1$  and such that the literal wires are placed between the meridians containing

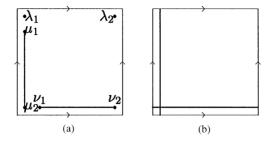


Fig. 10. Blocker assembly.

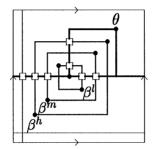


Fig. 11. Clause assembly.

 $v_1$  and  $v_2$ . Note that all the essential wirings for the literal and variable wires have been blocked by the blocker assembly. For each clause assembly, the wire  $\theta$  can use only the wirings showed in Fig. 11.

The considerations done in the proof of Theorem 2 are valid in order to prove the equivalence between the affirmative answers of both problems. And it is not essential which of the two possible layouts of wire  $\lambda$  is chosen from a truth assignment.

Figs. 12 and 13 are the adaptation of Figs. 8 and 9 to the sBws problem, respectively.

As we indicated above, if the sBWS problem can be solve in polynomial time, it is also possible to solve the problem of determining the minimum genus of a surface on which a wire set can be laid out in single bend fashion in polynomial time. Hence, the following result is obtained as a consequence of Theorem 4.

**Corollary 5.** *Given a wire set, finding a surface of minimum genus on which the wires can be laid out with only one bend is NP-hard.* 

## 5. Conclusions and open problems

Wire layout problems and in particular orthogonal layouts appear in many applications of computer science. In this paper, we have considered the problem of wiring pairs of points on different surfaces using wirings with only one bend. This problem was studied by Raghavan et al. [11] on the plane. They developed an  $O(m^2)$  algorithm

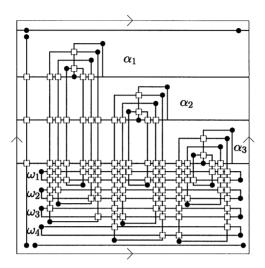


Fig. 12. An example of Theorem 4 for the clauses of Fig. 8.

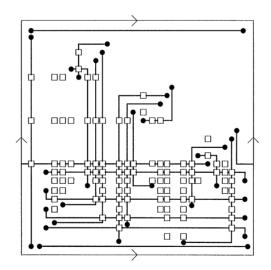


Fig. 13. Layout of the wires in Fig. 12 from the truth assignment of Fig. 9.

to determine whether or not a set of m wires can be single bend wired on the plane. As the layouts are not allowed to cross, the answer for most wire sets is negative. We generalize the problem allowing vias in the wires and so we consider pairs of points in surfaces rather than in the plane.

Given a wire set on a surface and only two possible single bend wirings for each wire, we prove that in this case the problem can be solved in polynomial time. The NP-completeness of the problem is obtained if the number of possible layouts is increased. So, the problem of finding the surface of minimum genus on which a wire set can be single bend wired is NP-hard.

Raghavan et al. [11] show that determining the maximum number of point pairs that can be wired with at most one bend on the plane is NP-hard. On the other hand, the same problem is posed considering multilayered wiring media but they show that determining the minimum number of layers needed to wire a set of point pairs is also NP-hard. We tried to relate these results to the problem on higher genus surfaces but, despite initial ideas, though, we see no way to derive our theorems, directly, or by way of corollary, from their results.

Many open problems arise in this context. Since the problems *n*-sBWs and sBWs are NP-complete, it will not be a rewarding task to develop an exact algorithm for their solution. On the other hand, the surface  $\mathscr{S}$  is arbitrary in the problems *n*-sBWs and sBWs and we might try to obtain efficient algorithms for special surfaces, for example for cylinders (in that case there are four possible single bend wirings for each wire). It is an open problem to decide whether or not a wire set can be laid out with only one bend on the cylinder having three or four possible layouts for each wire.

#### References

- C. Batini, E. Nardelli, R. Tamassia, A layout algorithm for data-flow diagrams, IEEE Trans. Software Eng. SE-12 (4) (1986) 538–546.
- [2] C. Batini, M. Talamo, R. Tamassia, Computer aided layout of entity-relationship diagrams, J. Systems Software 4 (1984) 163–173.
- [3] T.C. Biedl, Optimal orthogonal drawings of triconnected plane graphs, Proceedings of the SWAT'96, Lecture Notes in Computer Science, Vol. 1097, Springer, Berlin, 1996, pp. 333–344.
- [4] J.P. Cohoon, P.L. Heck, BEAVER: a computational–geometry–based tool for switchbox routing, IEEE Trans. Comput.-Aided Des. Integrated Circuits Systems 7 (6) (1988) 684–697.
- [5] S. Even, A. Itai, A. Shamir, On the complexity of timetable and multicommodity flow problems, SICOMP 5 (1976) 691–703.
- [6] M.A. Garrido, A. Márquez, Embedding a graph in the grid of a surface with the minimum number of bends is NP-hard, in: G. DiBattista (Ed.), Graph Drawing, Proceedings of the GD'97, Lecture Notes in Computer Science, Vol. 1353, Springer, Berlin, 1998, pp. 124–133.
- [7] Y. Hsu-Chun, On multilinear single bend wirability, IEEE Trans. Comput.-Aided Des. Integrated Circuits Systems 13 (6) (1994) 822–826.
- [8] T. Lengauer, Combinatorial Algorithms for Integrated Circuit Layout, Wiley, New York, 1990.
- [9] Y. Liu, A. Morgana, B. Simeone, General theoretical results on rectilinear embeddability of graphs, Acta Math. Appl. Sinica 7 (1991) 187–192.
- [10] Y. Liu, A. Morgana, B. Simeone, A linear algorithm for 2-bend embeddings of planar graphs in the two-dimensional grid, Discrete Appl. Math. 81 (1998) 69–91.
- [11] R. Raghavan, J. Cohoon, S. Sahni, Single bend wiring, J. Algorithms 7 (1986) 232-257.
- [12] R. Tamassia, On embedding a graph in the grid with the minimum number of bends, SIAM J. Comput. 16 (1987) 421–444.