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ABSTRACT: The use of Sigma-Delta (ΣΔ) modulation for analog-to-digital conversion (ADC) in the communication frequency range is evaluated. Two high-order multi-bit architectures are proposed to achieve +12-bit dynamic range at 4Msample/s Nyquist rate using very low oversampling ratio. They show very low sensitivity to the internal D-to-A conversion (DAC) error with no calibration required. Simulations show that such performance can be achieved even in presence of circuit imperfections.

1. Introduction

Sigma-Delta modulators (ΣΔM) have been successfully employed in the past for low-, medium-frequency ADC [1]. In these converters the use of oversampling and noise-shaping techniques avoids the need of extremely accurate analog building blocks, which is very suitable in the context of emerging poor-analog-performance sub-micron CMOS processes [2]. Such advantages have encouraged to widen the bandwidth of ΣΔ converters up to data acquisition and communication applications [3]-[6], displacing the Nyquist-rate converter architectures (folding, interpolative, etc.).

The signal bandwidth f_x and the sampling frequency f_S of a ΣΔ converter are related through the oversampling ratio $M = f_S/(2f_x)$. Thus, increasing the signal frequency while keeping achievable sampling frequency implies the reduction of M required to obtain given resolution. This last can be roughly estimated, considering only quantization noise, as follows:

$$B(\text{bit}) = \frac{1}{2}\log_2\left[\frac{(2^b-1)^2(2L+1)M^{2L+1}}{\pi^{2L}}\right] \qquad (1)$$

where b is the resolution (bit) of the internal quantizer and L is the modulator order. It is clear from (1) that high-order multi-bit quantization ΣΔMs are natural candidates to achieve high-resolution, high-speed ADC. However two important drawbacks arise: on the one hand, unlike 1st- and 2nd-order loops, high-order loops are not unconditionally stable; on the other, the linearity of a multi-bit ΣΔM is ultimately limited by that of the multi-bit DAC in the feedback path*. Both problems have already been partially solved; in particular, high-order ΣΔMs have been stabilized in practice through several techniques [1]: i.e., proper choice of the scaling factors, use of multi-path feed-forward structures, or resetting of the internal variables if unstable operation is detected [7]. On the other hand, a common strategy to palliate the strong dependence on the internal DAC linearity consists of using calibration either in the analog or in the digital domain [1].

Moreover, some ΣΔM architectures overcome these problems with neither calibration nor resetting required; the basic idea consists of: first, performing the high-order filtering by cascading low-order (1st- and 2nd-) ΣΔMs to guarantee unconditional stability; and, second, using multi-bit quantization only at the last stage of the cascade to attenuate the influence of the multi-bit DAC non-linearity [4][8].

This paper explores the use of such techniques to obtain 12bit *DR*, 4Msample/s ADC. In Section 2, two cascade multi-bit architectures are considered: a 4th-order 3-stage cascade (with the structure 2-1-1) and a 5th-order 4-stage cascade (2-1-1-1), both including multi-bit quantization. Section 3 is dedicated to analyze the impact of circuit imperfections and the results are compared to those obtained for other high-speed ΣΔ modulator architectures.

2. Cascade multi-bit ΣΔMs

Fig.1 shows a generic *L*th-order *N*-stage cascade multi-bit ΣΔM. It includes single-bit quantization in all the stages of the cascade except in the last one which incorporates a multi-bit quantizer. The advan-

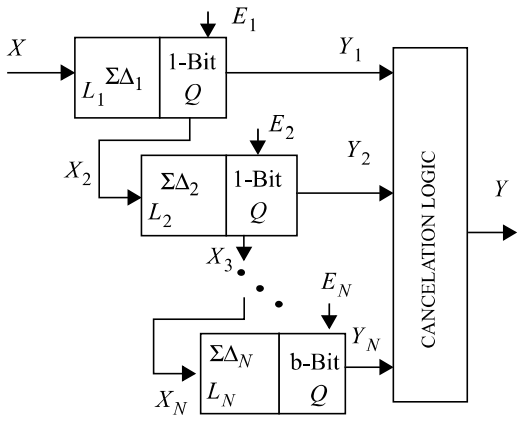

Fig. 1: Generic *L*th-order *N*-stage cascade multi-bit ΣΔM

*. Note, that this is not a problem for single-bit quantization, because the two-level DAC is intrinsically linear.

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tages of doing so are pointed out by calculating the Z-domain transfer function for each error contribution: Like in single-bit cascade ΣΔMs the quantization error induced in each stage is re-modulated by the following in the cascade. Once in the digital domain, by properly combining the outputs of the stages, which contain digital representations of different quantization errors, it is possible to cancel out the quantization error in all stages except, obviously, that in the last one, which appears at the modulator output attenuated by a shaping function of order equal to the summation of the order of all stages. Thus, ideally, the following is obtained for the Z-domain output:

$$Y(z)= z^{-L}X(z) + d(1-z^{-1})^{L}E_N(z) - d(1-z^{-1})^{(L-L_N)}E_D(z) \tag{2}$$

where $X(z)$ is the Z-transform of the modulator input, d is an scalar larger than unity that results from the need of properly scaling the signal transferred from a stage to the next one in order to prevent premature overloading, $E_N(z)$ is the last stage quantization error, $E_D(z)$ is the error induced in the last stage DAC, and $L = L_1 + \ldots + L_N$. Note that $E_D(z)$ is $(L-L_N)$th-order shaped, which may significantly relax the linearity specification of the DAC, with no correction nor calibration required.

Based on the topology of Fig.1, two multi-bit ΣΔM architectures have been proposed: the one in [4], uses a 2-stage 2-1 cascade (2-1*mb*), that is $L_1 = 2$ and $L_2 = 1$, while the one in [9], uses a 2-stage 2-2 cascade (2-2*mb*), $L_1 = 2$ and $L_2 = 2$. By replacing these values in (2), the power spectral density (*PSD*) of the last stage DAC error is 2nd-order shaped in both cases. Assuming ideal conditions except for the DAC-induced error, the in-band error powers are:

$$P_{2\text{-}1mb} = d^2\left(\sigma_Q^2\,\frac{\pi^6}{7M^7} + \sigma_D^2\frac{\pi^4}{5M^5}\right)$$
$$P_{2\text{-}2mb} = d^2\left(\sigma_Q^2\,\frac{\pi^8}{9M^9} + \sigma_D^2\frac{\pi^4}{5M^5}\right) \tag{3}$$

where $\sigma_Q^2 = [\Delta/(2^b-1)]^2/12$ is the power of the last-stage quantization error (Δ stands for the last-stage quantizer full-scale) and σ_D^2 represents the DAC-induced error power. The latter is hence attenuated by the fifth power of M in both architectures.

Fig.2 shows two novel ΣΔM architectures, also based on the generic representation of Fig.1, that better exploits the exposed technique. Fig.2(a) is a 3-stage 2-1-1 cascade with multi-bit quantization in the third stage (2-1^2*mb*), while Fig.2(b) is a 4-stage 2-1-1-1 cascade with multi-bit quantization in the fourth stage (2-1^3*mb*). The presence of three (for the 2-1^2*mb*) and four (for the 2-1^3*mb*) integrators before the point where the internal DAC error is injected provides 3rd-order and 4th-order shaping functions respectively for the *PSD* of such error. This result is easily obtained from the general formulation in (2) where now $L_1 = 2, L_2 = 1$ and $L_3 = 1$ (for the 2-1^2*mb*) and $L_1 = 2, L_2 = 1, L_3 = 1$ and $L_4 = 1$ (for the 2-1^3*mb*), giving

$$Y(z)|_{2\text{-}1^2mb} = z^{-4}X(z) + d_3(1-z^{-1})^4E_3(z) - d_3(1-z^{-1})^3E_D(z)$$
$$Y(z)|_{2\text{-}1^3mb} = z^{-5}X(z) + d_5(1-z^{-1})^5E_4(z) - d_5(1-z^{-1})^4E_D(z) \tag{4}$$

where it has been assumed that the relationships among digital and analog coefficients and the values of the digital filters $H_k(z)$, $k = 1, \ldots, 6$ are those shown in Tables 1 and 2, respectively. Therefore, the in-band error power at both modulator outputs yields

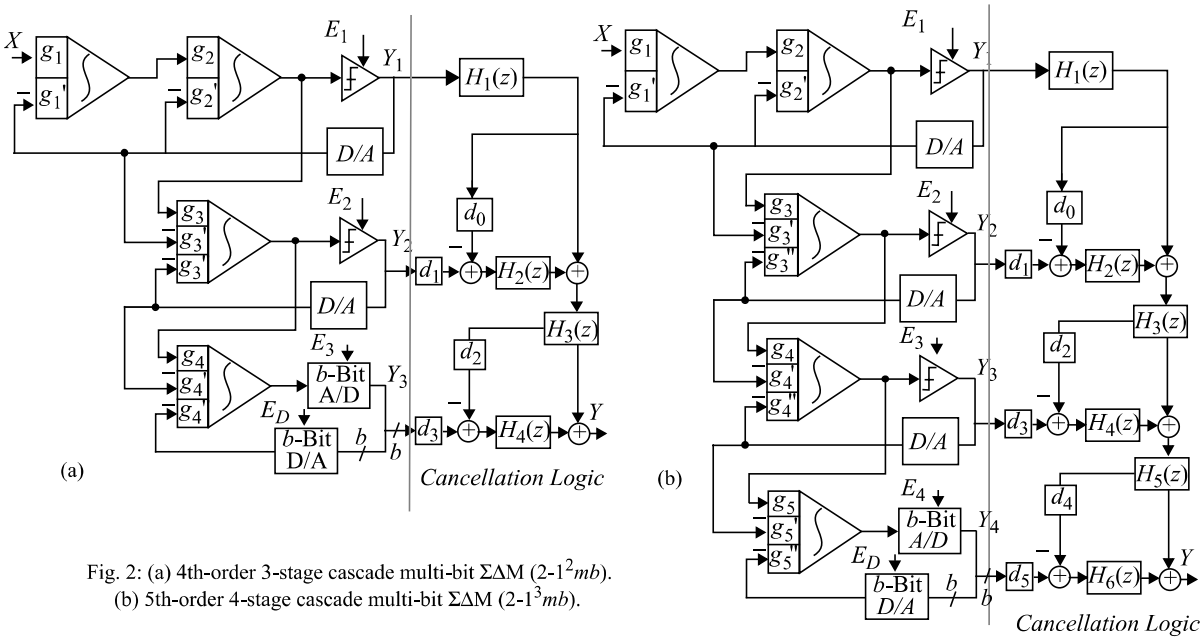

Fig. 2: (a) 4th-order 3-stage cascade multi-bit ΣΔM (2-1^2*mb*). (b) 5th-order 4-stage cascade multi-bit ΣΔM (2-1^3*mb*).

$$P_{2\text{-}1^2mb} = d_3^2\left(\sigma_Q^2\,\frac{\pi^8}{9M^9} + \sigma_D^2\frac{\pi^6}{7M^7}\right)$$
$$P_{2\text{-}1^3mb} = d_5^2\left(\sigma_Q^2\,\frac{\pi^{10}}{11M^{11}} + \sigma_D^2\frac{\pi^8}{9M^9}\right) \quad (5)$$

where it is pointed out that the weight of the DAC error contribution has been reduced in two and four powers of *M*, respectively, in relation to the expressions in (3). This significantly relaxes the linearity requirement of the last-stage DAC and hence simplifies its design.

Table 1: Digital transfer functions and relationships among coefficients in Fig.2(a)

Digital	Digital/Analog	Analog
$H_1(z) = z^{-1}$	$d_0 = 1 - \frac{g_3'}{g_1 g_2 g_3}$	$g_1' = g_1$
$H_2(z) = (1-z^{-1})^2$	$d_1 = \frac{g_3''}{g_1 g_2 g_3}$	$g_2' = 2g_1' g_2$
$H_3(z) = z^{-1}$	$d_2 = 0$	$g_4' = g_3'' g_4$
$H_4(z) = (1-z^{-1})^3$	$d_3 = \frac{g_4''}{g_1 g_2 g_3 g_4}$	

Table 2: Digital transfer functions and relationships among coefficients in Fig.2(b)

Digital	Digital/Analog	Analog
$H_1(z) = z^{-1}$	$d_0 = 1 - \frac{g_3'}{g_1 g_2 g_3}$	$g_1' = g_1$
$H_2(z) = (1-z^{-1})^2$	$d_1 = \frac{g_3''}{g_1 g_2 g_3}$	$g_2' = 2g_1' g_2$
$H_3(z) = z^{-1}$	$d_2 = 0$	$g_4' = g_3'' g_4$
$H_4(z) = (1-z^{-1})^3$	$d_3 = \frac{g_4''}{g_1 g_2 g_3 g_4}$	$g_5' = g_4'' g_5$
$H_5(z) = z^{-1}$	$d_4 = 0$	
$H_6(z) = (1-z^{-1})^4$	$d_5 = \frac{g_5''}{g_1 g_2 g_3 g_4 g_5}$	

2.1 Integrator weight optimization

Whatever set of coefficients (integrator weights in Fig.2) fulfilling the relationships of Tables I and II leads to the expressions in (4). Nevertheless for real implementations the following considerations must be taken into account:

- The level of the signal transferred from one stage to the next one must be low enough not to overload the latter. These levels are approximately equal to the reference voltages for a 1st-order modulator, and 90% of the reference voltages for a 2nd-order modulator.
- The output swing needed in the integrators, which depends on their weights as well as on the input level, must be physically achievable. In switched-capacitor implementations this limit is imposed by the supply voltages.
- Digital coefficients d_3 and d_5, which amplify the last-stage quantization error in (4), should be as small as possible.

Additional considerations in order to simplify the implementation are:

- The digital coefficients should be 0, ±1 or multiple of 2.
- The gain of the last-stage multi-bit quantizer, which, unlike that of the single-bit quantizers, is well defined, must be such that the loop gain of this stage equals unity. In order to simplify the design of the multi-bit quantizer the gain required to fulfill the previous condition should not be too large.

Based on these criteria, the selection of the weight coefficients can be mapped into an optimization problem solvable by computational algorithms. In particular, we used a modified version of the simulation annealing algorithm [6]. Results are shown in Table 3. With these values the integrator output swing requirement is reduced to only the reference voltages for the 2-1^2*mb* and twice that value for the 2-1^3*mb*. Note that in both cases the *PSD* of the last-stage quantization noise is amplified by 2, $d_3 = d_5 = 2$ in (4). This means a systematic loss of resolution of 6dB (1bit) respect to the ideal case given in (1)†. However, this loss is small compared to that caused by the stabilization and non-linearity correction mechanisms used in other approaches [1].

Table 3: Analog and digital coefficients in Fig.2. Shaded cells correspond to the 2-1^3*mb* modulator.

g_1	0.25	0.25	g_4	2	0.5	d_0	-1
g_1’	0.25	0.25	g_4’	1	0.5	d_1	2
g_2	1	1	g_4”	1	0.5	d_2	0
g_2’	0.5	0.5	g_5	-	2	d_3	2
g_3	1	2	g_5’	-	1	d_4	0
g_3’	0.5	1	g_5”	-	1	d_5	2
g_3”	0.5	1					

These coefficients present two additional advantages:

†. Another 5th-order multi-bit architecture initially considered by us, the 2^2-1*mb* ΣΔM, formed by two 2nd-order stages and a 1st-order stage, was discarded at this point because the selection of coefficients required to avoid the overloading of the last stage lead to $d_5 = 8$ (3bit lost with respect to the ideal case).

- Because in all three-weight integrators the largest weight can be easily obtained as a linear combination of the other weights, an SC implementation will only require two-branch integrators. Note that only one branch is needed for the first integrator.
- The input of the last stage is just the quantization noise generated in the previous stage, which in practice is not correlated with the modulator input; so, the DAC non-linearity will not distort the modulated output signal.

3. Influence of circuit imperfections

Except for the DAC-induced errors, the architectural study in previous Section assumes ideal conditions. Nevertheless, circuit imperfections must be taken into account for practical designs [1][6]. Circuit non-idealities degrading the performance of ΣΔ modulators can be grouped in two categories: (a) those that change the quantization noise transfer function, whose effect strongly depends on the architecture considered, for instance integrator leakage and weight mismatching, and (b) those that can be modeled as an error source at the first integrator; such approximation is justified by the fact that the contributions of remaining integrators are attenuated by increasing powers of the oversampling ratio. This is the case of defective settling in integrators, thermal noise, etc.

3.1 Integrator leakage and weight mismatching

Ideal study of Section 2 assumes that the relationships of Table 1 and 2 are fulfilled and that the transfer function of the integrators is exactly $z^{-1}/(1-z^{-1})$. However, in practice these assumptions are not valid: on the one hand, the actual values of the integrator weights differ from their nominal values due to mismatch in capacitors ratios; on the other, the integrator transfer function above is modified by the finite open-loop gain of the amplifiers. Both non-ideal aspects result in incomplete cancellation of the quantization error generated in the former stages thus degrading the signal-to-noise ratio (*SNR*) [6][10]. Analysis shows that the extra in-band error power due to these non-idealities is:

$$P_E = \sigma_C^2\left[\frac{(g_1+g_2+g_2')^2}{A_V^2}\frac{\pi^2}{3M^3}+\varepsilon_1^2\frac{\pi^4}{5M^5}\right] \qquad (6)$$

where A_V stands for the integrator DC-gain, ε_1 refers to mismatching in weights g_1, g_2, g_3 and g_3" and $\sigma_C^2 = \Delta^2/12$ is the quantization error power of a single-bit quantizer.

Note that eventually this extra noise can mask those in (5), so that there is a practical upper limit for the resolution of the multi-bit quantizer. The value of this limit can be more accurately evaluated using behavioral simulation [6][11]. Fig.3 shows the simulated signal-to-(noise+distortion) ratio (*SNDR*) of the 2-1^2*mb,* and 2-1^3*mb* modulators, Fig.3(a) and (b) respectively, for an input tone with amplitude equal to the half-scale input range, as a function of the last quantizer resolution. Oversampling ratios are 16 and 8, respectively. These simulations correspond to the worst case in presence of integrator finite DC-gain, weight mismatching and DAC non-linearity (*INL*).

Note that the non-ideal curve saturates around 3bit for the 2-1^2*mb* modulator and 4bit for the 2-1^3*mb*. So, under the conditions above, using higher resolution quantizers would not lead to further improvement. However, as shown later, such resolutions are enough to significantly relax the circuit requirements with respect to previous approaches.

3.2 Other circuits imperfections

We have evaluated the influence of the non-idealities belonging to the second category in the beginning of this Section by using the modulator sizing tool in [6][11]. This tool, combining accurate analytical expressions for each error contribution and statistical optimization, allows to obtain the less-demanding building block specifications that do not degrade the modulator performance.

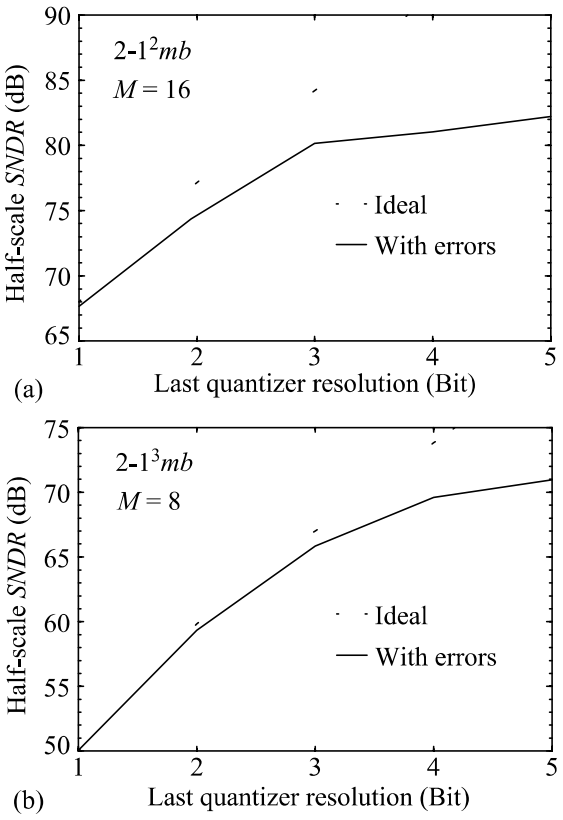

Fig. 3: Half-scale *SNDR* vs. the resolution of the multi-bit quantizer for (a) 2-1^2*mb* and (b) 2-1^3*mb* modulators. Simulation parameters are: $A_v = 1500$; standard deviation of integrator weights = 0.1% and DAC *INL* = 1% Δ.

Table 4: Modulator sizing results

SPECS: 12bit@4MS/s@1V		**2-1^2*mb***	**2-1^3*mb***	**2-1^2**	**2-1*mb***	Unit
Modulator	Oversampling ratio	16	8	20	16	
	Sampling frequency	64	32	80	64	MHz
	Reference voltages	±1	±1	±1	±1	V
Integrators	Sampling capacitor	0.5	0.5	0.5	0.5	pF
	Unitary capacitor	0.5	0.5	0.5	0.5	pF
	Capacitor non-linearity* ≤	25	25	25	25	ppm/V
	Switch ON resistance	0.75	1	0.75	0.5	kΩ
Opamps	DC-gain ≥	63dB	65dB	63dB	65dB	
	DC-gain non-linearity ≤	20%	20%	20%	20%	V^{-2}
	Transconductance	7	4	8	7	mA/V
	Maximum output current ≥	1.5	0.6	1.75	1.5	mA
	Differential output swing ≥	±1	±1 / ±2†	±1	±1	V
Comparators	Hysteresis ≤	30	30	30	30	mV
	Resolution time ≤	4	8	3	4	ns
A/D/A converter	Resolution	2	4	1	3	bit
	Non-linearity (*INL*) ≤	1%FS	0.7%FS	-	0.4%FS	
Dynamic range:		77dB (12.5bit)	74.4dB (12.07bit)	81.2dB (13.2bit)	74.6dB (12.1bit)	
Quantization noise		-80dB	-77.7dB	-85.2dB	-77.8dB	
Thermal noise		-91.1dB	-89.1dB	-91.6dB	-92.8dB	
Incomplete settling noise		-118.1dB	-151.4dB	-101dB	-137.8dB	
Harmonic distortion		-112.6dB	-113dB	-112.6dB	-113dB	

*. Significant only for single-ended implementations

†. Only third integrator needs ±2V output swing

Table 4 summarizes the circuit requirements to obtain resolutions in the range 12 to 13bit at 4Msample/s, 1-V FS with both architectures. Note that such performance is achieved with $M = 8$ (32-MHz sampling rate) for the 2-1^3*mb* modulator and $M = 16$ (64-MHz sampling rate) for the 2-1^2*mb*, using 4- and 2-bit quantization, respectively. Main differences between both sizings are in the dynamic specifications (opamp transconductance, output current, and quantizer resolution time). For instance, the amplifier transconductance required for 2-1^3*mb* is around one half of that required for 2-1^2*mb*. The same applies for the maximum output current. In terms of power consumption, the current per opamp needed for the 2-1^3*mb* would be from 25% to 50% of that required for the 2-1^2*mb*.

Another feature, very convenient for low-voltage CMOS implementations, is that the use of optimized weights allows the integrator output swing to be only the reference voltage (±1V), except for the third integrator of the 2-1^3*mb* modulator which for scaling requirements must be at least twice that value.

The already mentioned low sensitivity of the new architectures to the DAC non-linearity is confirmed by the relatively large *INL* allowed without degrading the required performance. Such values, around 1%FS, represent an effective resolution of about 6bit for the last-stage DAC, which is feasible at the sampling rate.

It is worth mentioning that the sizing in Table 4 takes into account the influence of the two main non-idealities of cascade multi-bit modulators: integrator leakage (through the value of the amplifier DC-gain) and weight mismatching (through the value of the unitary capacitor to be used in the layout, as in [6]).

For comparison purposes, Table 4 also includes the sizing for two previously reported architectures: a 4th-order 3-stage (2-1^2) single-bit modulator [3] and a 3rd-order 2-stage multi-bit (2-1*mb*) modulator [4]. The required performance is achieved with 20 and 16 oversampling ratios, respectively, although the latter is combined with 3-bit quantization in the last stage. Both modulators are shown to be disadvantageous for this application. On the one hand, because the oversampling ratio of the 2-1^2 modulator is not a power of two, the design of the decimator may result in a more complicated, less efficient digital filter. On the other, the fulfillment of the dynamic requirements for this modulator would need an increase of around 30% in

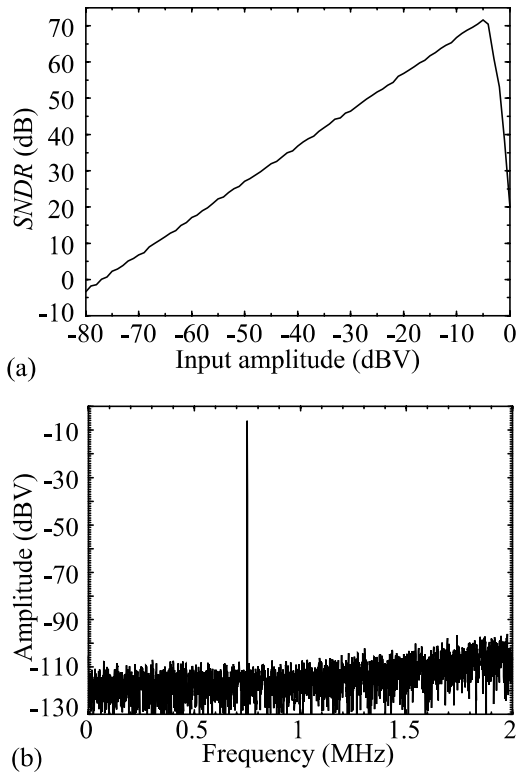

Fig. 4: 2-1^2*mb* modulator with sizing in Table 4: (a) *SNDR* vs. input amplitude and (b) output spectrum for a -6dBV@750kHz input tone.

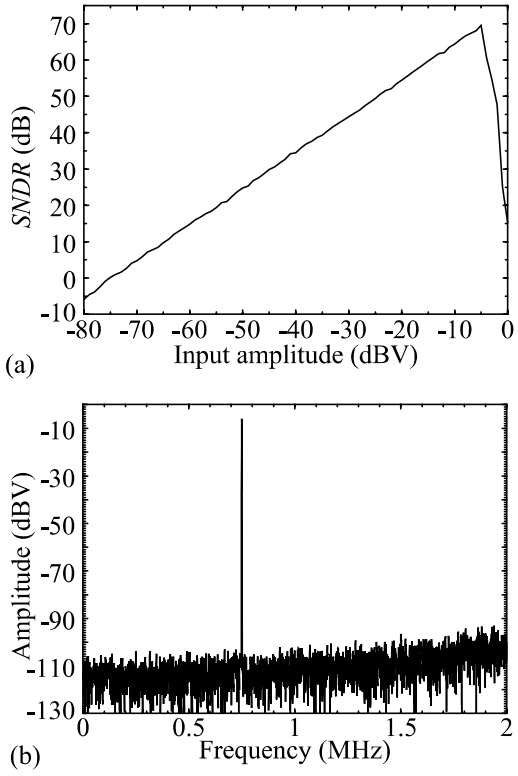

Fig. 5: 2-1^3*mb* modulator with sizing in Table 4: (a) *SNDR* vs. input amplitude and (b) output spectrum for a -6dBV@750kHz input tone.

the current per opamp with respect to the 2-1^2*mb*. Regarding the 2-1*mb* architecture, which requires dynamic parameters similar to those for the 2-1^2*mb*, the *INL* must be half of that for the latter, which means one more bit in the effective resolution of last-stage DAC.

Fig.4 shows some results for the 2-1^2*mb* modulator obtained with the behavioral simulation tool in [6][11]. This simulation includes all the circuit non-idealities in Table 4. In particular, the impact of weight mismatching has been evaluated by Monte-Carlo analysis. Fig.4(a) shows the worst-case signal-to-(noise+distortion) ratio (*SNDR*) after decimation as a function of the input amplitude. Decimation by 16 was performed using a 1024-coefficient FIR filter, which ensures that the passband is flat up to 2MHz. The dynamic range can be obtained from this curve as the distance between the reference level (0dBV) and the point where the *SNDR* crosses 0dB, resulting approximately 76dB (12.4bit effective resolution). Fig.4(b) shows the output spectrum of the 2-1^2*mb* modulator for a half-scale (-6dBV) input tone at 750kHz. Note that no harmonic distortion is present and that noise floor is flat up to 1MHz approximately as a consequence of un-shaped error contributions as, for instance, thermal noise.

Fig.5 shows equivalent results for the 2-1^3*mb* modulator. Dynamic range is 75dB (12.1-bit effective resolution).

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