Signal Sampling Based Transition Modeling for Digital Gates Characterization *

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Abstract. Current characterization methods introduce an important error in the measurement process. In this paper, we present a novel method to drive the timing characterization of logic gates under variable input transition times. The method is based on sampling and scaling realistic transition waveforms and it is easy to implement and introduces negligible computational overhead in the characterization process. We show how models characterized using the proposed method may improve accuracy from 5% to 8%.

1 Introduction

During the design stages of a digital circuit, simulation is applied to validate a design before fabrication. Typically, only critical parts of the circuit are simulated using low-level simulators working at the electric level (SPICE, HSPICE [1], etc.). This kind of simulation is accurate but very time and resources consuming and is usually not applicable to the whole circuit. On the other hand, logic-level simulators are able to handle big circuits and even whole systems by using simplified, logic-level models and very fast event-driven algorithms [2]. This is done at the expense of accuracy, due to the simplified nature of logic-level models and algorithms. The accuracy of the logic-level simulation is typically measured by comparing to electrical-level simulation results which are much more accurate.

The scientific community has spent a great effort in developing better logic-level models, commonly referred to as delay models. These models try to calculate the propagation time of an input transition in a logic gate to the output. The propagation delay depends on multiple factors: the output load of the gate,

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the waveform of the input transition, the supply voltage and the internal design characteristics of the gate itself. New generation delay models try to take into account all these effects [3–9].

In order to build new delay models and/or characterize the model parameters of a logic block, accurate electrical simulation of the block is carried out under controlled external conditions that may be altered as necessary. These variable conditions are the supply voltage, the output load and the input waveform. Providing a given supply voltage is not a problem and the output load can be easily and accurately modelled by a capacitor, at least in a CMOS technology. The input waveform, however, presents some problems: on the one hand, we need to be able to apply different types of input transitions, ranging from slow to fast ones to cover all the possible operations of the gate but, on the other hand, the generated input transitions need to be similar to the actual waveforms in a real circuit. The most commonly used approach is to build linear input transitions and use the transition slope or the transition time as the variable representing the waveform shape. The delay model, then, will include the dependence on this transition time. This approach assumes that the linearized input transition is equivalent to a real transition and a mapping between linear and real transitions is provided. Some of these mapping approaches are:

- A ramp with the same slope than the real transition at $V_{DD}/2$ [6].
- Similar to the previous one but applying a correcting factor [10].
- A ramp crossing the real transition at given voltage levels, like 10%-90%, 20%-80%, or 30%-70% [11].

Among many proposed approaches for input transition linearization not a commonly criteria has been accepted because none of them have proved to be fully satisfactory. In our opinion, using linear input transitions to drive a model characterization is a source of inaccuracy since real transitions often diverge from a linear ramp, specially at the beginning and end of the transition as shown in Fig. 1.

In this paper we propose a better method to synthesize input transitions for gate characterization. The method consists of using a PWL (piecewise linear) curve instead of a ramp. A reference PWL curve is obtained by sampling a single "real" transition obtained from accurate electric-level simulation. The number of points in the PWL curve is high enough to make it very close in slope to the real input transition. The slope of the curve measured at the 20% and 80% of the supply rail is taken as the characteristic parameter of the transition. During a characterization process, this reference curve is used so that arbitrary values of the slope are obtained by scaling the time axis of the reference curve as necessary to obtain a modified transition of the required slope. This is a simple and fast calculation. The modified curve can then be applied to the gate under test to collect new timing data.

It is important to remark that only one reference curve is necessary for a single technology process or even for several technology processes, and that it is easy to obtain by simulating a single transition in a reference circuit with an

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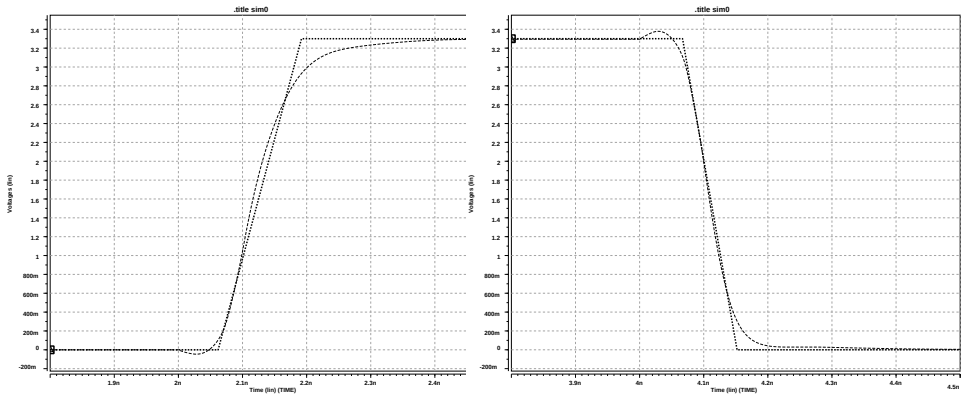

(a) (b)

Fig. 1. Ramp approach method using 20%-80% criterion.

accurate electrical simulator like HSPICE. Also, like in the conventional ramp approach, the only characteristic transition parameter used is the slope.

By using this approach we can drive any characterization process where input transition time needs to be controlled by using more realistic waveforms that will provide us with more accurate data. To show this, after presenting the method to obtain the reference transition in Sect. 2, we will set up a simple look-up table based model in Sect. 3. The model will be characterized using the conventional approach with input ramps and using the proposed sampled input transitions. In Sect. 4, we will use a test bench that will be simulated using HSPICE under different load and input conditions. Electrical simulation results will be compared to calculations from the previous characterized models. Finally, in Sect. 5, we will summarize some conclusions.

2 Obtention and Usage of the Sampled Input Signals

To obtain the sampled signal, we have simulated an inverter chain with six gates (Fig. 2). The analysis has been carried out in a 0.35 μm CMOS technology using the standard cell library provided by the foundry, and all simulations have been performed using HSPICE. We have supplied a step input to the first inverter and sampled the output of the third one allowing this inverter to be supplied with a real input signal (provided by the second gate) and to be charged with a real gate at its output (the fourth gate). This process has been performed for both raising and falling output cases obtaining two sets of 500 samples that conform the two sampled input signals (Fig. 3). The sample period has been established to be 1 ps.

In order to use the sampled data, we only have to scale the set of samples depending on the input slope we need. For example, if we need an input transition time of 100 ps, we must firstly establish a criterion for the choice of these points

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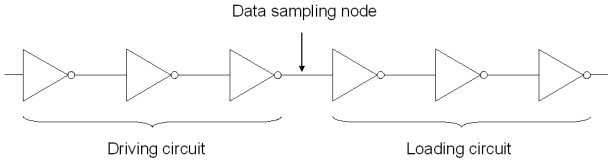
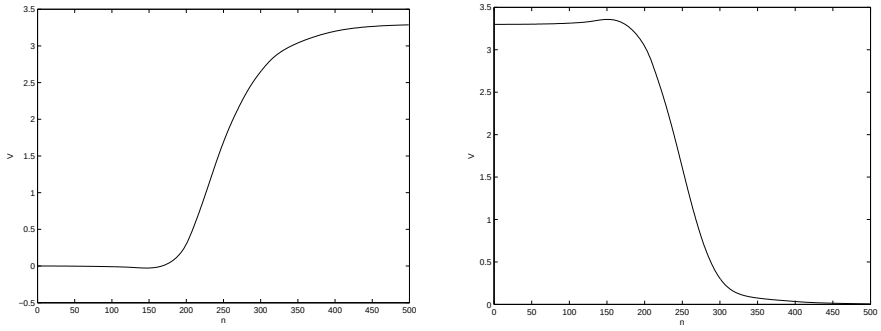


Fig. 2. Obtention of sampled reference curve.



(a) (b)

Fig. 3. Sampled signals for both raising (a) and falling (b) output cases (each one compounded of 500 samples).

(we have used the 20%-80% criterion) and scan the set of samples until we find the two samples that better approximate the values $0.20V_{DD}$ and $0.80V_{DD}$.

Once we have the indexes of these samples, we must calculate the new period time as the ratio between the needed input transition time and the amount of samples:

$$t_{step} = \frac{0.60\tau_{in}}{i_{80\%} - i_{20\%}} \tag{1}$$

Now, we can supply these new data to the gate and perform the simulation. We have carried out our tests using HSPICE and have automated the process of generating this scaled input according to this simulator. The developed function defines a PWL input signal and supplies it to the gate under analysis. The mentioned function has been implemented in C language.

3 Application to simple look-up table delay model

In this section we will apply the proposed method to the characterization of a simple look-up table based delay model. A CMOS inverter is taken as a sample gate and timing information (propagation delay and output transition time) is collected for a range of input transition time values and two typical loading conditions using accurate circuit-level simulation (HSPICE). All these measures

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are stored in a table so that timing information for arbitrary input transition time and load can be calculated by interpolating the stored data.

We want to point out that, in our opinion, the use of look-up table models in general is not a good choice because of their high requirements in characterization time and data storage. Equation-based models are much more efficient. However, using a table model in this paper allow us to analyze the behaviour of the proposed method isolated from additional effects.

To build the model table, we need to control the input waveform to provide different transition times. The characterization process is done twice, once using traditional straight input ramps method (IR-method), and once again using scaled sampled inputs (SI-method) as described in the previous section. In the next section we will compare the accuracy of both approaches.

4 Simulation results and analysis

To compare the IR-method with the proposed SI-method, we will use the test circuit in Fig. 4.a.

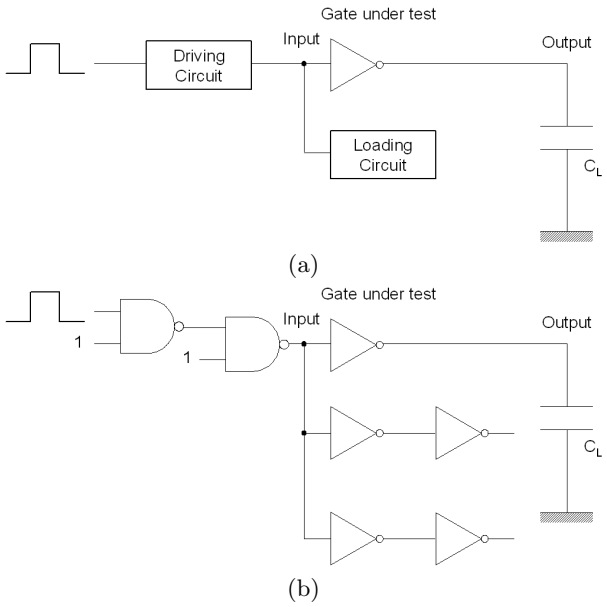

Fig. 4. Test circuit: (a) Generic circuit and (b) Driving NANDs circuit.

The test circuit provides various realistic input transitions to the gate under test. Since the transition waveform will depend on the nature of the driving circuit and the loading conditions at the input node to the gate under test, different cases have been simulated:

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– Case 1: The driving circuit is a chain of two CMOS inverters.
– Case 2: The driving circuit is a chain of two CMOS NAND gates with one of their inputs set to logic '1'.

The loading circuit is a chain of two inverters. In order to obtain several transition times and different input waveforms, the circuit has been simulated in three ways: (a) without loading circuit, (b) with one loading circuit, and (c) with two loading circuits (Fig. 4.b).

For each case and for every loading circuit configuration, the gate under test is analyzed for two values of the loading capacitance: $C_L = 2C_{in}$ and $C_L = 4C_{in}$; where C_{in} is the equivalent input capacitance of the gate under test.

HSPICE simulations are carried out on all these cases, both for rising and falling input transitions, so that extensive timing information about the operation of the gate under a range of realistic conditions is obtained. HSPICE results are shown in Table 1 and Table 2 for cases 1 and 2 respectively.

Table 1. HSPICE results for case 1

Input behav.	Load circ.	C_L/C_{in}	τ_{in} (ps)	t_{p0} (ps)	τ_{out} (ps)
Rise	0	2	136.3	83.7	126.7
		4	135.2	112.8	182.8
	1	2	188.3	90.0	137.1
		4	187.0	121.3	194.0
	2	2	245.0	95.2	147.9
		4	243.0	128.8	205.8
Fall	0	2	101.0	86.2	167.8
		4	100.6	119.6	248.3
	1	2	133.5	93.5	174.8
		4	133.1	128.1	255.0
	2	2	166.3	100.4	182.3
		4	165.7	136.3	262.5

In order to analyze the accuracy of the proposed characterization method, the input transition times obtained from HSPICE simulations are used to compute the calculated delay and output transition time from the look-up table models characterized in Sect. 2. Calculations are done by linear interpolation. Propagation delay and output transition times results are shown in Table 3 and Table 4. For the sake of clarity, only deviation percentages with respect to HSPICE are shown.

Both in Table 3 and Table 4, we can see that the proposed approach gives much better results than the traditional method, in every of the 24 cases simulated. In order to get the big picture, summarized results are presented in Table 5, where minimum, maximum, and average deviations with respect to HSPICE have been calculated for the six different simulated configurations of input and output loading conditions.

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Table 2. HSPICE results for case 2

Input behav.	Load circ.	C_L/C_{in}	τ_{in} (ps)	t_{p0} (ps)	τ_{out} (ps)
Rise	0	2	200.7	90.6	138.9
		4	199.3	122.3	196.0
	1	2	255.2	95.5	149.1
		4	253.2	129.2	207.2
	2	2	315.3	99.6	159.5
		4	312.7	135.3	218.8
Fall	0	2	137.9	95.1	177.5
		4	137.5	130.2	256.7
	1	2	167.2	101.1	183.8
		4	166.6	137.4	263.7
	2	2	196.3	106.8	190.3
		4	195.7	144.2	270.8

Table 3. IR-method and SI-method relative error for case 1

				IR-method		SI-method	
Input behav.	Load circ.	C_L/C_{in}	τ_{in} (ps)	t_{p0} (%)	τ_{out} (%)	t_{p0} (%)	τ_{out} (%)
Rise	0	2	136.3	8.58	9.20	0.90	0.12
		4	135.2	8.74	6.88	0.41	0.56
	1	2	188.3	7.41	8.43	1.53	0.49
		4	187.0	9.06	9.32	0.98	0.04
	2	2	245.0	5.27	7.24	0.90	0.78
		4	243.0	8.42	9.02	1.77	0.52
Fall	0	2	101.0	3.88	3.73	0.25	0.42
		4	100.6	3.54	1.97	0.41	0.56
	1	2	133.5	4.54	6.44	1.20	1.02
		4	133.1	4.89	3.90	1.09	0.38
	2	2	166.3	4.50	7.39	2.27	2.06
		4	165.7	5.84	6.04	2.17	1.57

Table 4. IR-method and SI-method relative error for case 2

				IR-method		SI-method	
Input behav.	Load circ.	C_L/C_{in}	τ_{in} (ps)	t_{p0} (%)	τ_{out} (%)	t_{p0} (%)	τ_{out} (%)
Rise	0	2	136.3	6.26	7.85	0.72	0.17
		4	135.2	8.43	8.97	0.63	0.16
	1	2	188.3	4.68	6.41	0.41	0.32
		4	187.0	7.63	8.61	1.17	0.21
	2	2	245.0	3.79	3.85	0.15	0.07
		4	243.0	5.80	7.97	0.59	0.26
Fall	0	2	101.0	5.25	7.45	2.10	2.09
		4	100.6	5.75	4.44	2.00	0.80
	1	2	133.5	4.98	8.07	2.79	2.77
		4	133.1	6.47	6.44	2.82	1.96
	2	2	166.3	4.51	8.73	3.17	3.51
		4	165.7	6.87	8.39	3.31	3.13

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In most cases, the proposed approach introduce an average relative error around 1% or below, while the traditional method average error is around 6%. Another important result is that the "maximum" error observed with the proposed method is 3.5%, while the "minimum" error introduced by the ramp approach is always above 3.5% except for one case, that is 2%. In some cases, the relative error is reduced up to 8%. Timing estimation is then clearly improved by using the sampled input based method.

Table 5. Summarized results

			Minimum		Average		Maximum	
			IR	SI	IR	SI	IR	SI
t_{p0}	Case 1	Rise	5.27%	0.41%	7.91%	1.08%	9.06%	1.77%
		Fall	3.54%	0.25%	4.53%	1.23%	5.84%	2.27%
	Case 2	Rise	3.79%	0.15%	6.10%	0.61%	8.43%	1.17%
		Fall	4.51%	2.00%	5.64%	2.70%	6.87%	3.31%
τ_{out}	Case 1	Rise	6.88%	0.04%	8.35%	0.42%	9.32%	0.78%
		Fall	1.97%	0.38%	4.91%	1.00%	7.39%	2.06%
	Case 2	Rise	3.85%	0.07%	7.28%	0.20%	8.97%	0.32%
		Fall	4.44%	0.80%	7.25%	2.38%	8.73%	3.51%

5 Conclusions

A novel method to drive the timing characterization of logic gates under variable input transition times has been presented. The method is based on sampling and scaling realistic transition waveforms and it is easy to implement and introduces negligible computational overhead in the characterization process.

It has been shown that models characterized using the proposed method may improve accuracy from 5% to 8%, just by using the proposed method.

At the sight of these results, we see that using simple input ramps may be an important source of error during model characterization (5%-8%). The proposed method greatly improves this situation by reducing the error due to the use of synthetic input transitions below 2% in most cases.

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