```
1   ----------------------------------------------------------------------------
2   -- Hardware AMBA bus IP for image scaling
3   ----------------------------------------------------------------------------
4   -- Entity:      TFG_VRESIZE_KERNEL
5   -- File:        TFG_VRESIZE_KERNEL.vhd
6   -- Author:      Luis Miguel Gonzalez Berrocal
7   ----------------------------------------------------------------------------
8   -- VHDL Standard: VHDL'93
9   ----------------------------------------------------------------------------
10  -- Naming Conventions
11  -- active low signals:                  "*_n"
12  -- clock signals:                       "clk", "clk_div#", "clk_#x"
13  -- reset signals:                       "rst", "rst_n"
14  -- generics:                            "C_*"
15  -- user defined types:                  "*_TYPE"
16  -- state machine next state:            "*_ns"
17  -- state machine current state:         "*_cs"
18  -- combinatorial signals:               "*_com"
19  -- pipelined or register delay signals: "*_d#"
20  -- counter signals:                     "*_cnt*"
21  -- clock enable signals:                "*_ce"
22  -- internal version of output port:     "*_i"
23  -- device pins:                         "*_pin"
24  -- ports:                               "Names begin with Uppercase"
25  -- processes:                           "*_PROCESS"
26  -- component instantiations:            "<ENTITY_>I_<#|FUNC>"
27  -- registers:                           "*_REG"
28  ----------------------------------------------------------------------------
29
30  library ieee;
31  use ieee.std_logic_1164.all;
32  use ieee.std_logic_unsigned.all;
33
34  entity TFG_VRESIZE_KERNEL is
35        generic (SHIFT : integer := 22);
36        port (Clk              : in std_logic;                        -- clk
37              Rst_n            : in std_logic;                        -- active low
    reset
38              Pixel_hinter_even : in  std_logic_vector (31 downto 0);  -- pixel of the
    pseudo row even
39              Pixel_hinter_odd  : in  std_logic_vector (31 downto 0);  -- pixel of the
    pseudo row odd
40              Beta_even         : in  std_logic_vector (15 downto 0);  -- vertical
    interpolation factor for pixel_hinter_even
41              Beta_odd          : in  std_logic_vector (15 downto 0);  -- vertical
    interpolation factor for pixel_hinter_odd
42              Pixel_out         : out  std_logic_vector (7 downto 0)); -- pixel of the
    destination image
43  end TFG_VRESIZE_KERNEL;
44
45  architecture Behavioral of TFG_VRESIZE_KERNEL is
46
47        signal interpolated_com : std_logic_vector (47 downto 0);
48        signal pixel_out_i : std_logic_vector (7 downto 0);
49
50  begin
51
```

```
52          combinatorial_PROCESS : process (Pixel_hinter_even, Pixel_hinter_odd, Beta_even,
     Beta_odd, interpolated_com)
53          begin
54                interpolated_com <= Pixel_hinter_even * Beta_even + Pixel_hinter_odd *
    Beta_odd + 2**(SHIFT - 1);
55
56                if (interpolated_com (31 downto 22) > X"FF") then
57                      pixel_out_i <= X"FF";
58                else
59                      pixel_out_i <= interpolated_com (29 downto 22);
60                end if;
61          end process;
62
63          sequential_PROCESS : process (Clk, Rst_n)
64          begin
65                if (Rst_n = '0') then
66                      Pixel_out <= (others => '0');
67                elsif (Clk = '1' and Clk'event) then
68                      Pixel_out <= pixel_out_i;
69                end if;
70          end process;
71
72    end Behavioral;
```