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1  ----------------------------------------------------------------------------
2  -- Hardware AMBA bus IP for image scaling
3  ----------------------------------------------------------------------------
4  -- Entity:      TFG_HRESIZE_KERNEL
5  -- File:        TFG_HRESIZE_KERNEL.vhd
6  -- Author:      Luis Miguel Gonzalez Berrocal
7  ----------------------------------------------------------------------------
8  -- VHDL Standard: VHDL'93
9  ----------------------------------------------------------------------------
10 -- Naming Conventions
11 -- active low signals:                  "*_n"
12 -- clock signals:                       "clk", "clk_div#", "clk_#x"
13 -- reset signals:                       "rst", "rst_n"
14 -- generics:                           "C_*"
15 -- user defined types:                 "*_TYPE"
16 -- state machine next state:           "*_ns"
17 -- state machine current state:        "*_cs"
18 -- combinatorial signals:              "*_com"
19 -- pipelined or register delay signals: "*_d#"
20 -- counter signals:                     "*_cnt*"
21 -- clock enable signals:               "*_ce"
22 -- internal version of output port:    "*_i"
23 -- device pins:                        "*_pin"
24 -- ports:                             "Names begin with Uppercase"
25 -- processes:                         "*_PROCESS"
26 -- component instantiations:          "<ENTITY_>I_<#|FUNC>"
27 -- registers:                         "*_REG"
28 ----------------------------------------------------------------------------
29
30 library ieee;
31 use ieee.std_logic_1164.all;
32 use ieee.std_logic_unsigned.all;
33
34 entity TFG_HRESIZE_KERNEL is
35       port (Clk             : in std_logic;                        -- clk
36             Rst_n           : in std_logic;                        -- active low reset
37             Pixel_even      : in std_logic_vector (7 downto 0);    -- pixel n of the
   source image
38             Pixel_odd       : in std_logic_vector (7 downto 0);    -- pixel n + 1 of
   the source image
39             Alpha_even      : in std_logic_vector (15 downto 0);   -- horizontal
   interpolation factor for pixel_even
40             Alpha_odd       : in std_logic_vector (15 downto 0);   -- horizontal
   interpolation factor for pixel_odd
41             Pixel_hinter_out : out std_logic_vector (31 downto 0)); -- pixel of the
   pseudo row
42 end TFG_HRESIZE_KERNEL;
43
44 architecture Behavioral of TFG_HRESIZE_KERNEL is
45
46 signal pixel_hinter_out_i : std_logic_vector (31 downto 0);
47
48 begin
49
50       combinatorial_PROCESS : process (Pixel_even, Pixel_odd, Alpha_even, Alpha_odd)
51       begin
52             pixel_hinter_out_i <= X"00" & (Pixel_even * Alpha_even + Pixel_odd *
```

```
     Alpha_odd);
53         end process;
54
55         sequential_PROCESS : process (Clk, Rst_n)
56         begin
57               if (Rst_n = '0') then
58                     Pixel_hinter_out <= (others => '0');
59               elsif (Clk = '1' and Clk'event) then
60                     Pixel_hinter_out <= pixel_hinter_out_i;
61               end if;
62         end process;
63
64   end Behavioral;
65
66
```