Programmable SC Biquad Using One Single Capacitor Bank

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Abstract

This paper presents a new technique for programming SC circuits using a single time-multiplexed capacitor bank, achieving a significant reduction in capacitance area. Simulation results of a programmable biquad low pass filter show the validity of the proposed method.

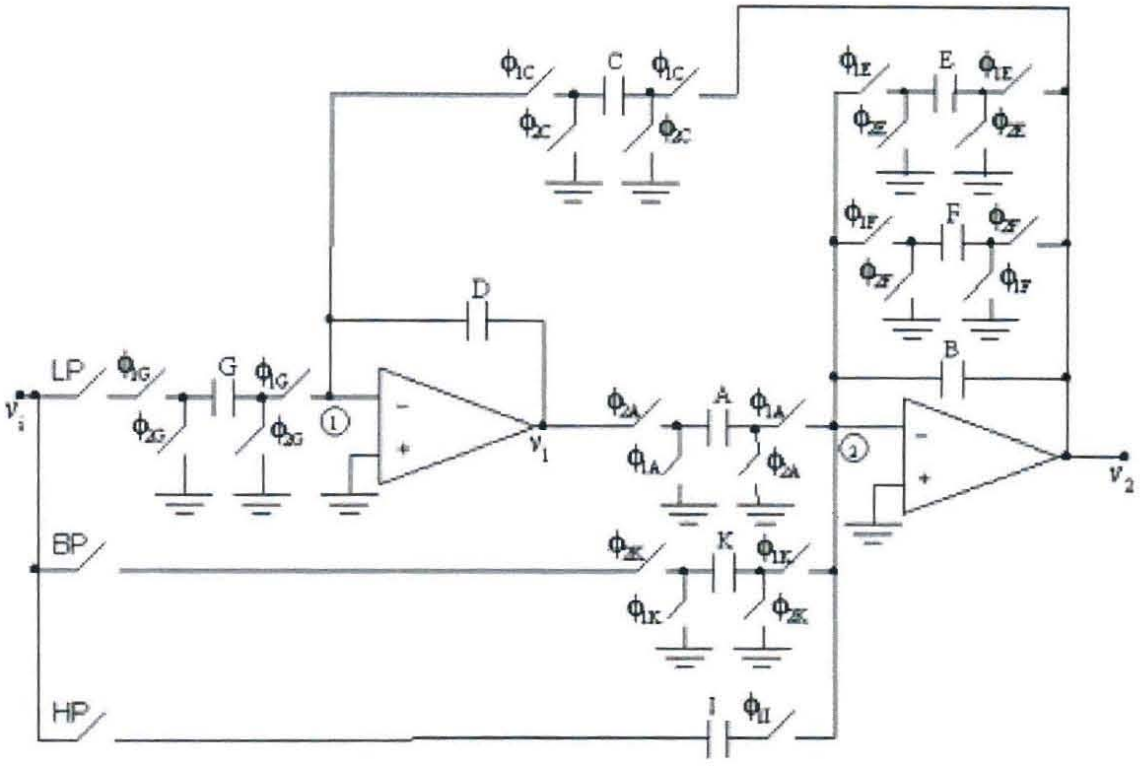


Figure 1. Universal biquad SC filter.

I. Introduction

SC filtering is a consolidated technique widely used in CMOS and BiCMOS analog and mixed-signal circuits. Many applications require filtering with programmable frequency responses. Most of previous implementations of programmable SC filters used digitally-controlled binary weighted capacitor arrays [1]-[2], leading to large area of silicon and hence, high cost of manufacturing. In [3], two capacitor quasi-passive algorithmic DAC´s were used for programming each capacitance value, leading to a significant reduction in the overall capacitance area.

Time-multiplexing is another technique that has been used to save area and to reduce power consumption in high order SC filters [4]-[6]. Different multiplexing strategies have been used. In [4], several integrator capacitors were multiplexed onto a single op-amp. In [5], the amplifiers were time-shared to realize two poles of filtering per amplifier in a ladder structure. In [6], an amplifier time-sharing technique was proposed to realize an arbitrary number of biquadratic cells with only two amplifiers. In [7], periodical nonuniform individual samplig of each SC structure in a filter was used to program SC circuits.

All previous approaches used one bank of capacitors per amplifier input. In this paper, a new technique for programming SC circuits is

proposed that uses one single time-multiplexed bank of capacitors for all the op-amp inputs.

Using the by-inspection analysis method for multiphase SC networks proposed in [8], the following transfer function is obtained

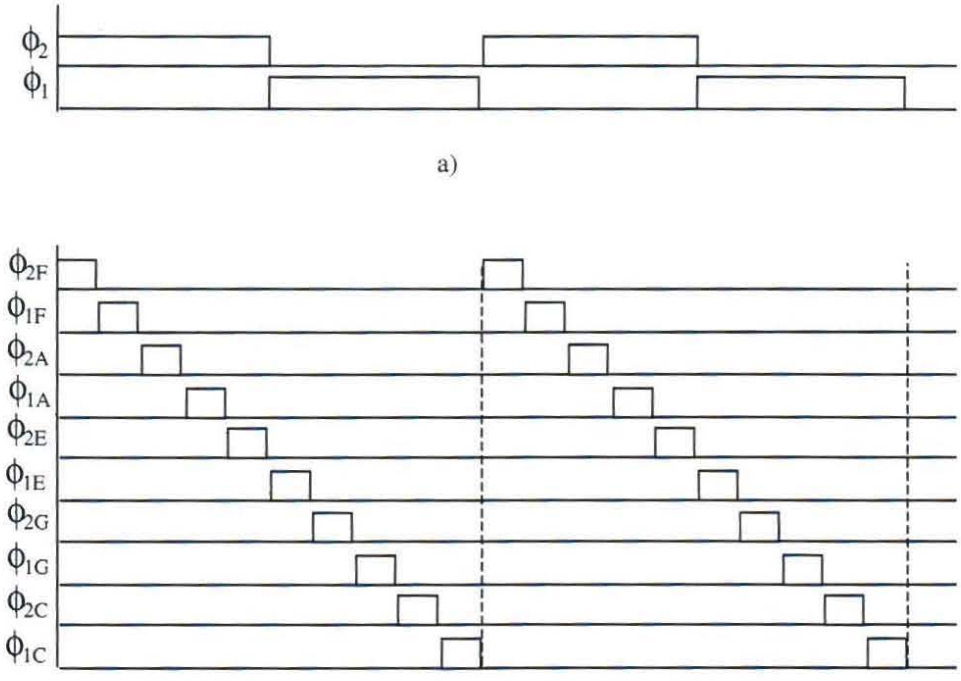


Figure 2. Time diagram for the circuit in figure 1. a) Conventional and b) proposed clock signals

II. Programmable SC biquad with one single capacitor bank

The proposed technique will be illustrated using the universal second order filter shown in figure 1 as an example. This circuit can provide BP, LP, and HP transfer functions, by enabling the corresponding signal paths by proper switching. Let's first consider the LP transfer function. Under conventional sampling operation, there are only two non-overlapping clock phases $\emptyset_1$ and $\emptyset_2$ (figure 2a). In this case, clock signals $\emptyset_{1\text{-}i}$, i $\{ i = A,C,E,F,G \}$ coincide with $\emptyset_1$ and clock signals $\emptyset_{2\text{-}i}$, $\{ i = A,C,E,F,G \}$ coincide with $\emptyset_2$. The transfer function of the SC filter is given by:

$$H(z) = -\frac{\frac{AG}{D(B+E)} \cdot z^{-1}}{1-\left[1+\frac{B+F}{B+E}-\frac{AC}{D(B+E)}\right] \cdot z^{-1}+\frac{B+F}{B+E} \cdot z^{-2}} \qquad (1)$$

Let's now divide the overall repetition period T_s into 10 equal-spaced intervals of duration $T_s / 10$, and define $\emptyset_{1\text{-}i}$, $\{ i = A,C,E,F,G \}$ and $\emptyset_{2\text{-}i}$, $\{ i = A,C,E,F,G \}$ with the timing shown in figure 2b.

Using the by-inspection analysis method for multiphase SC networks proposed in [8], the following transfer function is obtained

$$H(z) = -\frac{\frac{AG}{D(B+E)} \cdot z^{-5}}{1-\left[1+\frac{B+F}{B+E}-\frac{AC}{D(B+E)}\right] \cdot z^{-5}+\frac{B+F}{B+E} \cdot z^{-10}} \qquad (2)$$

which, disregarding the z^{-5} unit delay, is identical to (1).

Note that, under the timing proposed in figure 2b, capacitors A,C,E,F and G can be time-multiplexed using one single bank of capacitors, leading to the circuit in figure 3.

III. Simulation Results

To demonstrate the validity of the proposed technique, SWITCAP simulations of the circuit in figure 3 have been done. Capacitor values were determined for a nominal cutoff frequency $f_0 = 10\ KHz$, quality factor $Q = 0.707$, and unity dc gain. The master clock cycle was chosen to be $f_s = 1\ MHz$, leading to the following nominal capacitor values: $A = 1.2\ pF$, $B = 11.9\ pF$, $C = F = G = 0.4\ pF$, $D = 12\ pF$, and $E = 1.6\ pF$. Capacitors $\{A,C,E,F,G\}$ were implemented using one single bank of 8 binary weighted capacitors with $0.1\ pF$ of minimum value. Many

different transfer functions can be implemented in this way. Figure 4a shows the filter response when capacitors *{A,C,E,F,G}* are scaled for the same *k* factor, *k*= {1/4, 1/2, 1, 2, 4, 8}. Figure 4b shows the filter response when the capacitor *F* changes from *0.1 to 1.4 pF* and capacitors *{A,C,E,G}* have nominal values.

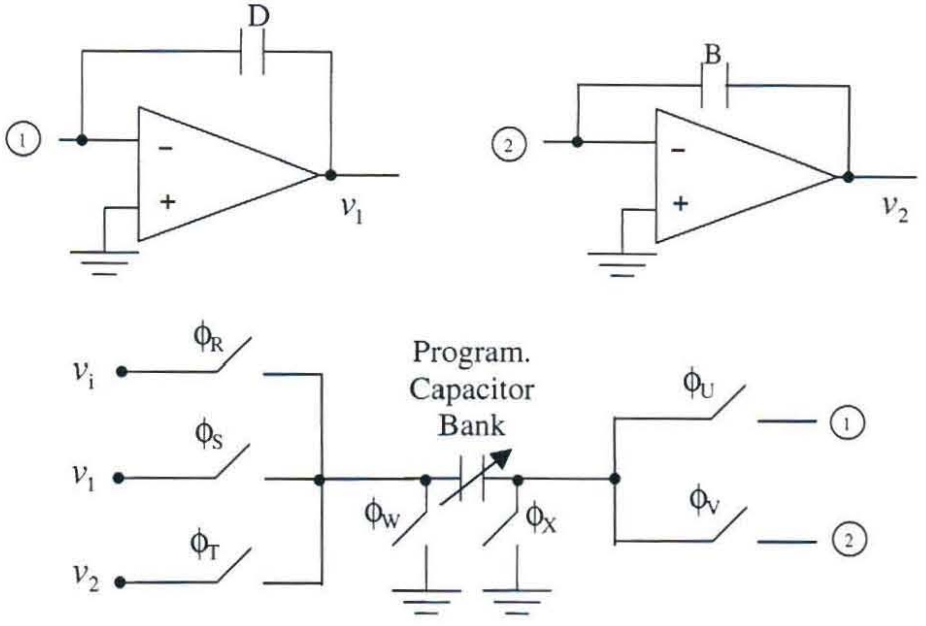
As expected, cutoff frequency and quality factor follow the approximate expressions

$$f_0 \approx \frac{f_s}{2\pi}\sqrt{\frac{AC}{D(B+E)}} \quad \text{and}$$

$$Q \approx \frac{1}{E-F}\sqrt{\frac{AC(B+E)}{D}} \qquad (3)$$

Although the transfer functions in (1) and (2) are identical (except for the z^{-5} unit delay), op-amp outputs are identical only during *1/5th* of the whole period T_s. This effect can not be ignored when the ratio $f_o/(5\,f_s)$ approaches *1/2*. For instance, assuming *[-1,1]* to be the amplifier output signal swing in the LP SC filter of figure 3, the maximum input signal amplitude is *882 mV* for the nominal filter (*k=1*), and *481 mV* for the least favorable case (*k=8*), as confirmed by SWITCAP simulations.

Similar results could be obtained using the BP and HP transfer functions of the circuit in figure 1. For the HP function, capacitor *I* cannot be programmed with the time-multiplexing technique proposed here, so a second capacitor bank would be required for programming capacitor *I*.



$$\phi_R = \phi_{1G} \qquad \phi_S = \phi_{2A} \qquad \phi_T = \phi_{2F} + \phi_{1E} + \phi_{1C}$$

$$\phi_U = \phi_{1G} + \phi_{1C} \qquad \phi_V = \phi_{1F} + \phi_{1A} + \phi_{1E}$$

$$\phi_W = \phi_{1F} + \phi_{1A} + \phi_{2E} + \phi_{2G} + \phi_{2C} \qquad \phi_X = \phi_{2F} + \phi_{2A} + \phi_{2E} + \phi_{2G} + \phi_{2C}$$

Figure 3. Programmable Low Pass SC biquad using one single capacitor bank.

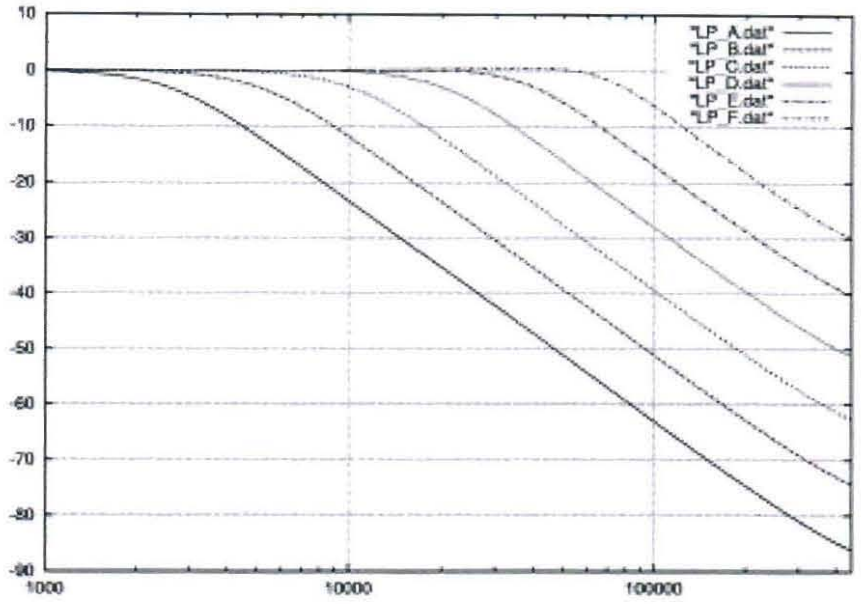
The proposed technique can be also used with other time-multiplexing techniques to implement higher order filters. Furthermore, a single quasi-passive algorithmic DAC [3] could have been used instead of the programmable capacitor bank of figure 3, with similar results.

It has to be mentioned that, in somes cases, switching capacitors with the timing of figure 2b may reduce the input dynamic range.

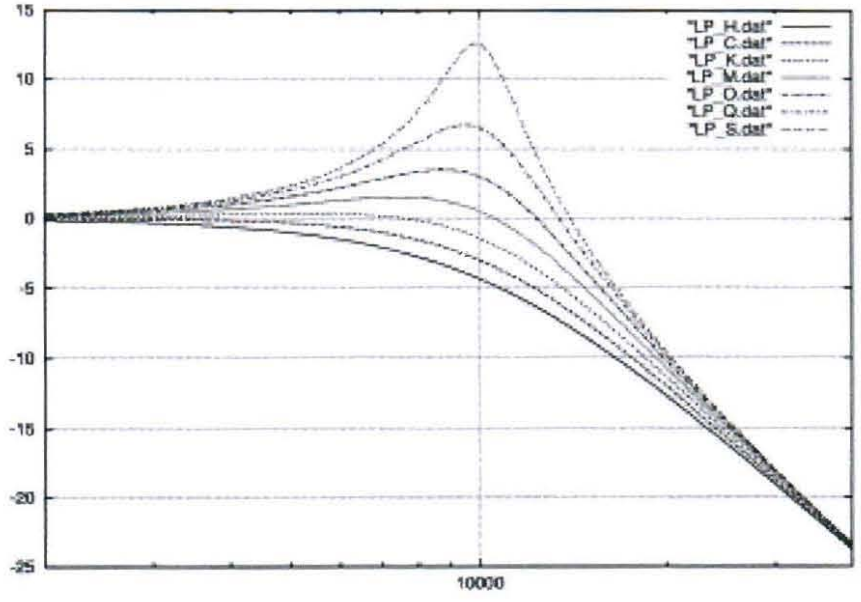
IV. Conclusions

To the authors' knowledge, no other method has been reported allowing a biquad section to be programmed using one single capacitor bank. The proposed technique achieves a very compact and area efficient implementation of SC filters. Compared to a conventional programmable biquad using multiple capacitor banks, the filter in figure 3 has a 40% area

occupancy, for a standard 0.35 μm CMOS technology. Concerning power consumption, the op-amps are required to switch faster, but with a lower capacitance load. Therefore, no a significant increase in power consumption is expected.



a)



b)

Figure 4. a) Frequency and b) Quality factor programmability

References

[1] ALLSTOT, D.J., BRODERSEN, R.W., and GRAY, P.R.: "An Electrically-Programmable Switched Capacitor Filter´´. *IEEE J.Solid-State Circuits*, 1979, 14 (6), pp. 1034-1041.

[2] COX, D.B.: "A Digitally Programmable Switched-Capacitor Universal Active Filter/Oscillator´´. *IEEE J.Solid-State Circuits*, 1983, 18 (4), pp. 383-389.

[3] PAULINO, N., FRANCA, J.E., and MARTINS, F.P.: "Programmable CMOS Switched-Capacitor Biquad using Quasi-Passive Algorithmic DAC's´´. *IEEE J.Solid-State Circuits*, 1995, 30 (6), pp. 715-719.

[4] BOSSHART, P.W.: "A Multiplexed Switched-Capacitor Filter Bank´´. *IEEE J.Solid-State Circuits*, 1980, 15 (6), pp. 939-945.

[5] ALLSTOT, D.J., and TAN, K.S.: "Simplified MOS Switched-Capacitor Ladder Filter Structures´´. *IEEE J.Solid-State Circuits*, 1981, 16 (6), pp. 724-729.

[6] CASTELLO, R., GRASSI, A.J., and DONATI, S.: "A 500-nA Sixth Order Bandpass SC Filter´´. *IEEE J.Solid-State Circuits*, 1990, 25 (3), pp. 669-676.

[7] J. L. AUSIN, J. F. DUQUE - CARRILLO, G. TORELLI, E. SANCHEZ-SINENCIO, F.MALOBERTI:"Periodical nonuniform individual sampled switched-capacitor circuits". IEEE Proc. of Int. Symp.. on CAS, ISCAS 2000, vol.V, pp. 449-452,
Geneva, Switzerland, May 2000.

[8] DABROWSKI, A., and MOSCHYTZ, G.S.: "Direct Analysis of Multiphase Switched-Capacitor Networks Using Signal-Flow Graphs´´. *IEEE Trans. Circuits Syst.*, 1990, 37 (5), pp. 594-6.