# DIGITAL TEST DESIGN WITH AN "AD HOC" STRATEGY FOR AN INDUSTRIAL ASIC WITH LARGE DIMENSION

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*Abstract*—
**The development of digital ASIC's with a large area states a lot of doubts when the engineer must design a test strategy. The design of an industrial circuit advises a test to be made quite similar to the normal field functioning. If the size of the die is large or quite complex this idea can be unreachable. The techniques of automatic test maybe relevant, though it should be increased the cell and routing area. If the circuit has been designed with a hierarchical manner with separated blocks, or works with some precompiled megacells, the application of these techniques can be inadvisable, so that we suggest a mixed solution. In this paper we describe a set of "ad hoc" strategies for the construction of a test for a large digital circuit, it has been introduced some additional simple circuits able to make visible some parts of the whole chip. Those ideas have been introduced in an industrial circuit which today is being manufactured.**

## I. Introduction

Obtaining a test covering of a digital integrated circuit is one of the stages which implies a lot of effort in the designing chain. If the design has a huge size this work can be performed by the VHDL compiler [1]. Its function consists of introducing scan–path chains [2] plus the generation of a set of test vectors for them, where the original configuration of the circuit is modified and all of the nodes within the circuits are tested [3].
Even if the components of the circuit cannot be led by the test compiler (such as precompiled cells, bidirectional internal buses, latches, ...etc), or the design is so large that the circuit must be developed in smaller blocks by different designers, the task becomes more complex. In the former case the designer must "trust" in the effectiveness of the test, together with a particular ruler for the VHDL code generation. In the latter it is necessary the optimization of the whole design by a test designer different to the one who designed every single block, where an additional effort is required (as regards the size of the whole design, the memory of the work station ...).
If there are not enough pins for testing the circuit, the total number of test vectors generated by the test compiler can exceed the maximum number allowed by the foundry. In large circuits there is an additional risk due to the clock delays that maybe big enough to produce race problems. This test circuit can mask unchecked delay problems, since the foundry only checks the test stimulus, which are not necessary to be functional vectors.
In this paper we propose a set of simple digital modules, which have been used in the development of an integrated circuit under the conditions stated above. Some internal structures have been taken into consideration in order to introduce some specific circuits in their test. This method can be used as a model for other large circuits because it does not exclude the use of automatic test tools in internal blocks of the circuit. In section II it is described the most used structured of the circuit, whose task consists of making it observable. In section III a stopping the general clock technique and improve the efficacy of the above circuit is proposed. In section IV it's described a mixed strategy of "scan–path", plus the viewer for more complex modules.

## II. Description of the viewer circuit

One repetitive structure typical of large size ASIC consists of connecting some blocks (operators and registers) to a bus. This bus is not usually visible from the outer, so that the connected blocks are not visible too. The *scan–path* technique has solved this problem adding some scan chains to the circuit. This solution introduces multiplexers in the circuits and increases the routing and cell area. The proposed structure takes into account the internal bus as a central part of the described module. All the elements are attached to it, and as a result its observation can improve the testability of the whole block. The controllability of the module is performed introducing a functional analysis, so we don't have to make an internal modification of it.
Figure 1 shows the proposed module for making visible all the blocks with this internal structure. Consists of a counter plus a multiplexer based on three–states gates which shows in a serial mode the bus content.

The additional area introduced by this structure is very small, compared with that introduced by the scan–path. The size of this structure in independent from the number of registers and operators attached to the bus, and only depends on the number of signals that can be observed. The classical scan–path technique increases the area when the number of flip–flops grows. To improve the efficacy of the module it has been necessary to introduce a stop clock mechanism which allows the bus content to be "freezed".

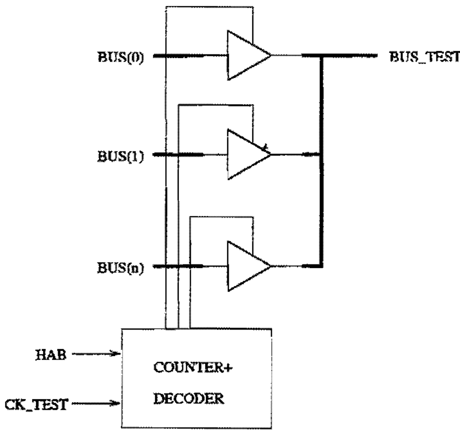


*Figure 1:*

## III. System clock stopping

Figure 2 shows the designed module for performing the clock stop. The aim is let the clock free of glitches that may lead the to undesirable situations, and also maintain an unique clock pin. In this way, the vector compression algorithm for test machine are possible to be introduced [3] Obviously, with this technique, the total vector number grows within the number of connected modules. However, this growth is not effective, if the compression vector algorithms are applied.
Figure 2 shows the proposed algorithm chart, limited by the active edge of the general clock, which is a rise edge.

## IV. Mixed technique

This technique can be spread to circuits with other different structures. Those modules without internal buses can be tested introducing a *scan–path* circuit and associate the output to a "viewer" that improves the efficiency of the scan path vectors. Random pulses can be introduced in the scan

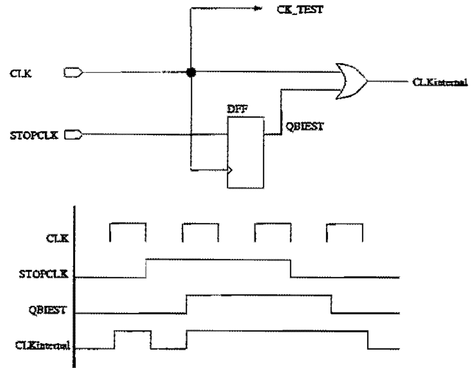


*Figure 2:*

chain since those generated by the automatic test tool can be used. This can improve the test cover index of the "dark" modules, taking into account the limited number of the test vectors required by the foundry. If there are several blocks the same random sequence can be injected to all the blocks simultaneously.

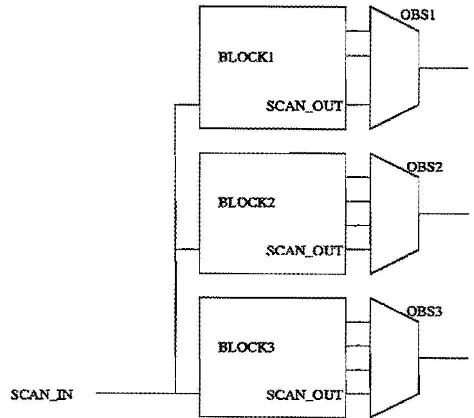


*Figure 3:*

## V. Conclusions

A simple test scheme for a large circuit with different blocks has been proposed. It consists of a technique which allows the use of functional vector patterns and improves the observability of the whole circuit. The use of those vectors let the detection of problems with different nature, such as clock race. The functional vectors must show the

presence of those problems, so they must be included in the whole vector set.
The test of a large circuit including macrocells has been performed. It has a such a size that a SUN 20 station was unable to store it into it's memory (256 Mb) to insert the test circuit for the whole design and then reoptimize it.
The whole set implies an important reduction of test area and as a result, of the whole circuit. Some functional and race problems can be detected. The whole circuit has obtained a test covering index of 90% and a final area reduction of a 20% compared to the solution with the automatic test. This reduction is due to a save in the standard cell area (DFFR=2097.6 $\mu m^2$, SFFR=2523.2 $\mu m^2$ in the ES2 library) and the routing area (the presence of the signal for activating the "scan–path" mechanism, the data signal that it introduces, which attach to all the flip–flops of the circuit). The second effect is the most important, in most cases.
Those technique are applied to an large size ASIC for industrial aims. Now it's in prototype test phase.

## References


[1] *Synopsys Online Documentation* v3.3a. Synopsys Inc.

[2] *Test Compiler Reference Manual.* Synopsys Inc.

[3] *ES2 Cadence Design Kit User Guide.*