Design of a band-pass sigma-delta modulator with reduced number of opamps

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Abstract

This paper is intended to compare the performance of a Band-Pass converter structure and its Low-Pass prototype 2nd order Sigma-Delta Analog to Digital converter. For this purpose Matlab simulations for the 4th order Band-Pass converter have been performed and its power consumption calculated when using the equivalent Op-Amp used in the Low-Pass modulator. First of all will be described the method used to calculate the transfer function and, thus, the structure of the Band-Pass structure to be tested. After a band-pass transfer function has been obtained it is implemented using reduced number of opamps. This topology is compared to the existing ones and a system level simulation and characterisation is performed. Finally, jitter limitations are studied. Transistor level simulations using Spectre have been done in order to validate MATLAB simulations prior to layout design.

1. Introduction

In applications where an IF signal has to be demodulated and converted to digital, two solutions may be used. The first one consists in down-converting the signal to base-band and converting to. Two converters would be needed. This solution is sensible to the mismatch between the real and imaginary branches of the demodulator. Other problems as offset and 1/f noise sensitivities affect the performance of the low-pass conversion.

An alternative solution is to perform a band-pass A/D conversion of the IF signal and demodulate in the digital domain. This can be accomplished using a band-pass sigma-delta modulator. This method is free from the two-path mismatch because it uses only one converter. The low frequency disables the effects of the 1/f noise. The main disadvantage of these structures is the effect of jitter on the SNDR. This makes necessary to build a low jittery clock that ensures that the input sampled signal SNR is enough not to degrade the modulator's performance.

Two methods are available to find an appropriate transfer function for the band-pass modulator. The simplest way is to start with an existing low-pass structure and perform a low-pass-to-band-pass transformation [1]. The second method is to design the transfer function via a Generalised Filter Approximator [2]. These are routines that adjust the poles and zeros of H(z) to accomplish with the amplitude specifications demanded by the designer. After that design, a stability study must be performed to guarantee the correct behaviour. Transforming an existing low-pass into a band-pass structure is more used because low-pass structures are better known and widely used. The present design will be built from an existing 2^{nd} order Low-Pass converter and a Low-pass-to-band-pass transformation will be applied.

2. Low-Pass prototype

A good approach in designing band-pass modulators is starting with a suitable low-pass structure. The strategy of building a low-pass prototype enables us to take advantage of the stability performance and the noise properties that are well studied for low-pass systems. Once are ensured these properties in the low-pass modulator, we can affront the task of transforming to a band-pass modulator preserving both stability and noise performance. The final band-pass structure must fit the needed requirements for signal band and over-sampling ratio. Once the low pass structure is designed, a low-pass-to-band-pass transformation is applied. This transformation must map the poles and zeros around the $w_0=0$ frequency to their final $w_0=w_f$ frequency. There are two approaches to go ahead with this transformation. Each of them has advantages that must be studied in order to choose the one that fits our needs.

a) **Generalised N-path transformation** is achieved doing $z \rightarrow +/- z^N$. This transformation preserves modulator dynamics but increase the modulator order unnecessarily (N>2) or result in a band-pass centred at $f_s/2$ for $z \rightarrow z^2$ (aliasing problems).

b) **Second order Low-Pass-To-Band-Pass transformations** give full control over the pass-band location but do not preserve modulator dynamics. For this strategy, the transformation:

$$z \rightarrow -z\cdot(z+a)/(a\cdot z+1), \text{ where } -1<a<1 \quad (1)$$

a<0 gives systems closer to DC.
a>0 gives systems closer to $f_s/2$.

When a=0 (1) $z \rightarrow -z^2$ and the result is a Band-Pass structure with $f_s/4$ central frequency.

This way, stability is guaranteed as well as the modulator dynamics. This will then be the approach to be followed in order to build the proposed structure.

In figure 1 is represented the 2nd order Low-Pass prototype. It has been widely studied and, thus, is a good starting point to build that band pass modulator. Once substituting z by $-z^2$, the structure is the one depicted in figure 2. It is clearly seen that integrators (figure 1) are transformed into resonators, but the overall structure is unchanged. In figure 2 is represented the result of this transformation.

3. Characterisation of a low-pass prototype

The first step in the design of a band-pass modulator using the low-pass to band-pass transformation method is to design its low-pass prototype. This low-pass prototype is the one depicted in figure 1. Multiple simulations have been performed to fully characterise its dynamic behaviour. The results of these simulations, using both MIDAS [12] and MATLAB [11], are shown in figures 3, 4.

To accomplish an optimum behaviour we look into the results to build our system using the best coefficients to improve SNDR and its sensitivity to variations of these coefficients, as well as the performance that will be needed in the design of the circuit's building blocks [1, 10].

At this point (functional system simulation) values for bandwidth, maximum input amplitude, op-amp dynamic specifications are all related to a normalised frequency f_s. Once a value for f_s is defined, all the other parameters can be known as absolute values.

Once is defined our low-pass prototype, the z by $-z^{-2}$ transformation is performed.

In figure 4 are represented the values that can be taken to design the opamp. On the x axis is represented the ratio: Ts/(2·TAU). Every curve has been calculated for a SRn, being $SR=SRn \cdot 2 \cdot f_s \cdot V_{sw}$.

4. Band-Pass structure

Several options are available to implement the transformed pass-band modulator. The direct transformation consists in replacing in the low-pass structure the integrators by resonators (figure 2) modifying the second adder to maintain the desired transfer function. Resonators are usually built using two opamps. This is a drawback in the design of low-power circuits. A first alternative is to design a single opamp resonator. This structure, depicted in figure 5, is described in [2]. The use of this structure complicates the clocking scheme, adding 6 extra clocks at half the sampling frequency. In this kind of structures it is extremely important to keep a strict control on clock phases to avoid signal dependent clock feedthrough that will appear inband as an image of the input frequency around $f_s/4$.

Another solution to obtain a band-pass modulator is replacing the resonators by Two-Delay Integrators as drawn in figure 6. In this structure integrators only use addition, that is why both input and output polarities need to be inverted every two delays. This effect is modelled multiplying those signals by the sequence: {1, 1, -1, -1, 1, 1, -1, -1, ...}. As in the case of resonators, two integrators are needed to perform the two-delay integration. In [3] a different solution is obtained to build an equivalent band-pass system as the one in figure 6. The interesting point of this is the possibility of implementing an N^{th} order structure using N opamps. In figure 6 is drawn the block diagram for a one bit modulator (proposed in [3]) that solves the problem using a minimum number of opamps. This consists in down-converting the input signal to its base-band I and Q components. Once the signal is down-converted, it is processed in the base-band region and finally up-converted to its original IF. Looking close we see that while one branch is integrating a variable input, the other one is integrating a "0", that is, that branch remains with a fixed output during that cycle. We can obtain the two-delay integrator with only one opamp that has two integrating capacitors connected. During odd cycles, the first capacitor is integrating while the other is idling (disconnected). During even cycles, the second capacitor is integrating while the first one is idle. This solution has the disadvantage of the degradation of the signal because of path mismatch between the I and Q branches. A solution to obtain a good matching is also proposed in [3].

The solution presented here departs from figure 6 and implements the two-delay integrator blocks using a single opamp, leading to the structure proposed in figure 7. This structure does not down-convert to process I and Q branches (as proposed in [3]) avoiding the problems that are derived from I and Q branches mismatch. This topology is implemented with the single opamp SC circuit drawn in figure 8. To accomplish the two-delay integration, the opamp is provided with 2 capacitors that hold both, I and Q, branches. At every cycle one of the branches is integrating while the other is idle. The problem of gain sensitivity can be neglected due to the low SNDR sensitivity to integration gain of this structure (fig. 9, 10).

Power consumption will be identical than for the Band-Width equivalent Base-Band Sigma-Delta

Modulator and opamp performance remains similar to those needed for Base-Band modulator (Fig. 10). There only remains the disadvantage of the effeet of jitter in band-pass structures that requires a very good clock.

5. Band-Pass simulation

The band-pass structure based upon the circuit of figure 7 has been simulated using MATLAB, and its SC version using CADENCE (Fig. 8). In figures 9,10 is shown the performance expected through simulation.

In figure 10 is depicted the SNDR loss for different values of the Slew-Rate and the BandWidth of the operational amplifiers used to implement the two-delay integrators. The x-axis is normalised to Ts and the SR is normalised to Delta/Ts. These results are similar to those obtained for the opamps used with a low-pass sigma-delta modulator, thus having similar power consumption. Because of this and that we use same number of opamps for band-equivalent low-pass and band-pass modulators, band-pass modulators can accomplish the same power consumption as the latter.

6. Simulations using CADENCE and MATLAB

Once is the band-pass modulator characterised, the structure of figure 7 has been implemented in a SC circuit (figure 8) and simulated with CADENCE (Spectre). In figure 11 is represented the frequency response for both (MATLAB and Spectre) simulations. Differential Opamps have been emulated with an Analog HDL as well as the comparator and voltage doublers. In the final version of this paper fully transistor-level results using Spectre will be included.

Similar parameters were used in both cases:

G1=0.25
G2=0.5
Input signal amplitude= 0.35·Delta
Input signal frequency= 0.6·Signal-Band/2
OSR=256

Ideal conditions were supposed for jitter, comparator and opamp performance.

7. Jitter influence in Band-Pass modulators

In band-pass modulators, where signals are not heavily over-sampled, jitter is a major problem to the frequency response of our system. Clock jitter results in non-uniform sampling and increases the total error power in the quantizer output. An estimation of this error is calculated in [8]. Once the input analog signal is sampled, the jitter has no influence on the system as it behaves as an analog sampled-data computer [1]. If the input data is sampled without jitter, the system will have a correct behaviour even if its internal clocking is affected by jitter. Then, jitter-related problems will appear at the input sample and hold stage. It is proven that under an uncorrelated gaussian random jitter with standard deviation dT, the power of the error signal is:

$S_{jitter} = A^2 \cdot (2 \cdot pi \cdot f_x \cdot dT)^2/2$

Where A is the signal amplitude and f_x is its frequency.

This error will be of interest inside the signal band. Since the jitter is considered white, the power error is reduced by the oversampling ratio (M), which is 4 in the proposed band-pass structure.

$S_{in\text{-}band} < Delta^2 \cdot (2 \cdot pi \cdot dT)^2/(8 \cdot M)$

To evaluate the tolerated jitter, one must calculated the maximum SNR desired at the system's output and limit the SNR of a sampled input signal (with jitter) to that value. If we expect to have a maximum output SNDR of 100dB, the jitter must be limited as to obtain a sampled input signal SNR of more than dB's when jitter is present.

In order to compare the effects of clock jitter in our system some MATLAB simulations have been performed. The jitter that affects the clock has different simulated magnitudes:

a) NULL jitter.
b) 100 ppm.

An input sinusoid signal is sampled using an OSR (Over-sampling Ratio) of 256 for a low-pass modulator and OSR=4 for a $f_s/4$ central pass frequency modulator. Frequency responses after sampling for each case are shown in figures 12, 13. Frequency is related to f_s=1, where f_s is the sampling frequency.

It is clearly seen that the effect of jitter on the spectra is worsened when decreasing the OSR. This makes band-pass modulators much more sensitive to clock jitter than low-pass modulators. This is the major drawback that present band-pass modulators. The next set of simulations shows the dependency of OSR in the effect of jitter. A jitter of 50ppm has been applied for different frequency pure sinusoidal signals. The effect of jitter makes the spectra to loose around 30dB in SNR when moving the working frequency from base-band to $f_s/4$.

These simulations are summarised in figure 16. They show the effect of jitter in both low-pass and band-pass modulators. As expected, the effect on the band-pass modulator is much higher.

8. Conclusions

A two-delay integrator using a single opamp is used to build a band-pass sigma-delta modulator. Only two opamps where needed to implement a 4^{th} order structure with a similar power consumption as equivalent low-pass modulators.

References

[1] "DELTA-SIGMA DATA CONVERTERS, theory, design and simulation". Steven R. Norsworthy, Richard Schreier and Gabor C. Temes. IEEE Press.

[2] "ANALOG CIRCUIT DESIGN..." Willy Sansen, Rudy J. Van de Plasshe and Johan H. Huijsing. Kluwer Academic Publishers.

[3] "A FOURTH-ORDER BANDPASS DELTA-SIGMA MODULATOR WITH REDUCED NUMBER OF OP-AMPS". Bang-Sup Song. IEEE Journal of solid-state circuits. Vol 30, No. 12, December 1995.

[4] "DESIGN OF LOW-VOLTAGE LOW-POWER CMOS DELTA-SIGMA A/D CONVERTERS". Vicenzo Peluso, Michiel Steyaert, Willy Sansen. Kluwer Academic Publishers.

[5] "THE DESIGN OF LOW-VOLTAGE, LOW-POWER SIGMA-DELTA MODULATORS". Shahriar Rabii, Bruce A. Wooley Kluwer Academic Publishers.

[6] "TOP-DOWN DESIGN OF HIGH-PERFORMANCE SIGMA-DELTA MODULATORS". Fernando Medeiro, Angel Perez-Verdu, Angel Rodriguez-Vazquez. Kluwer Academic Publishers.

[7] "MODELING AND HIGH-RESOLUTION SIGMA-DELTA MODULATORS". Louis Albert Williams III, August 1993, Stanford University. ICL93-022

[8] "THE DESIGN OF SIGMA-DELTA MODULATION ANALOG-TO-DIGITAL CONVERTERS". Bernhard E. Boser, Bruce A. Wooley. IEEE Journal of solid-state circuits. Vol SC-23, pp.1298-1308. December 1995.

[9] "SWITCHED-CAPACITOR BANDPASS DELTA-SIGMA A/D MODULATION AT 10.7 MHz". Frank W. Singor, W. Martin Snelgrove. IEEE Journal of solid-state circuits. Vol 30, No. 3 , March 1995.

[10] "A 900-mV LOW-POWER DS A/D CONVERTER WITH 77-dB DYNAMIC RANGE". Vicenzo Peluso, Peter Vancorenland, Augusto M. Marqués, Michiel Steyaert, Willy Sansen. IEEE Journal of solid-state circuits. Vol 33, No. 12 , December 1998.

[11] "SIGNAL PROCESSING ALGORITHMS IN MATLAB". Samuel D. Stearns, Ruth A. David

[12] "MIDAS USER MANUAL". Shahriar Rabii, Louis A. Williams III, Bernhard E. Boser, Bruce A. Wooley
Stanford University, Oct.1997

Figures

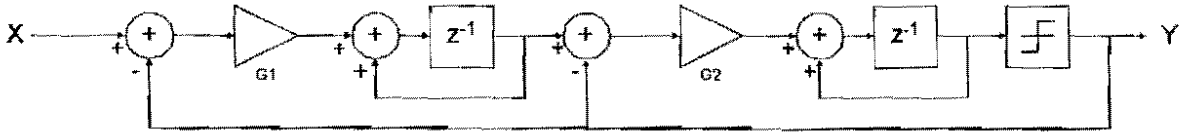


Figure 1. 2nd order Low-pass prototype.

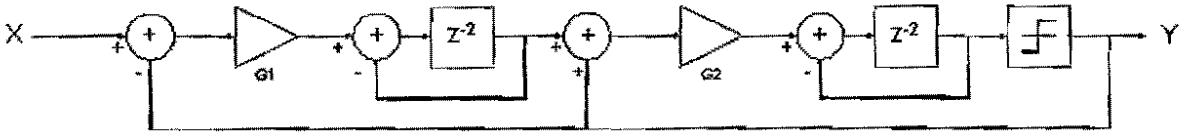


Figure 2. 4th order Band-Pass modulator using resonators.

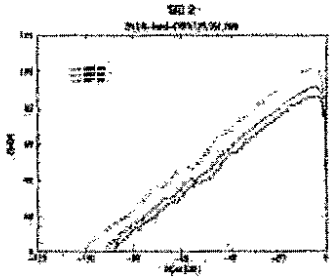


Figure 3. SNDR for a 2nd order LP Strueture

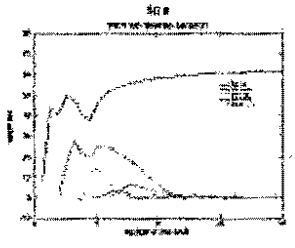


Figure 4. Opamp Specifications for a 2nd order LP structure

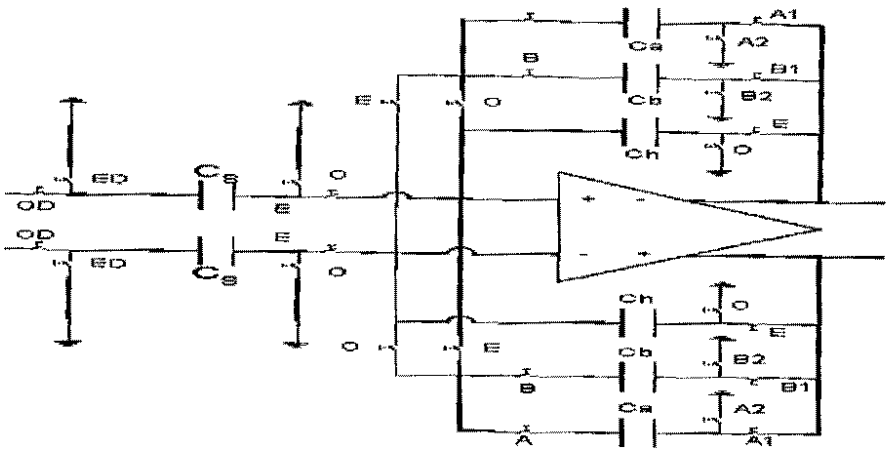


Figure 5. Switched Capacitor implementation of a resonator

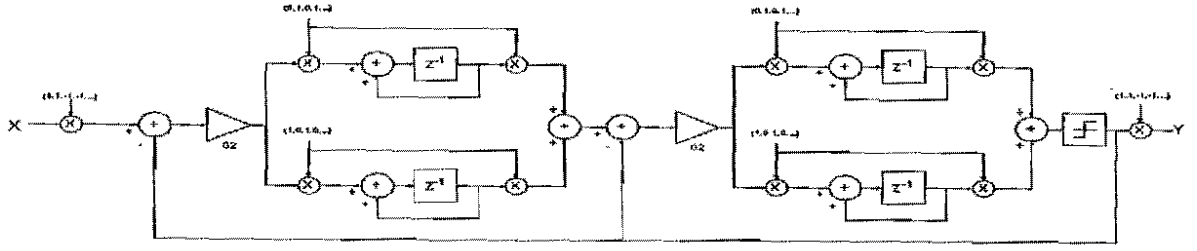


Figure 6. 4th order Band-Pass modulator

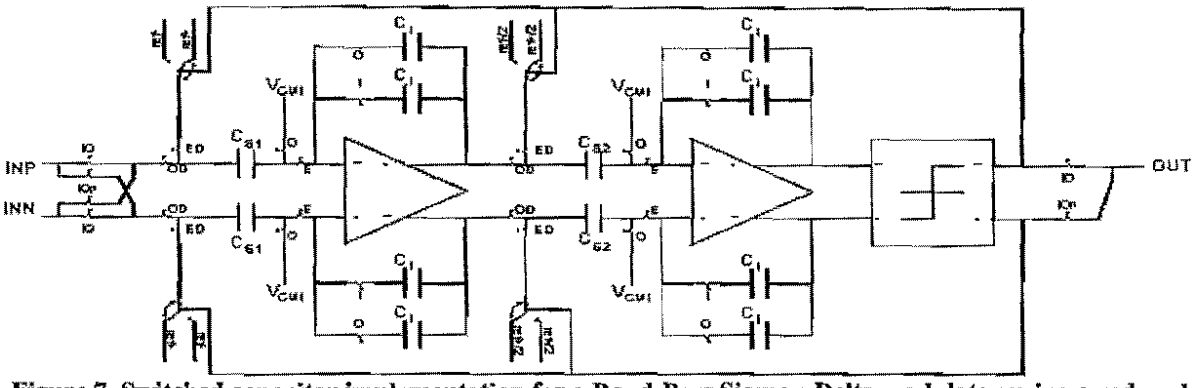


Figure 7. Switched capacitor implementation for a Band-Pass Sigman-Delta modulator using a reduced number of opamps

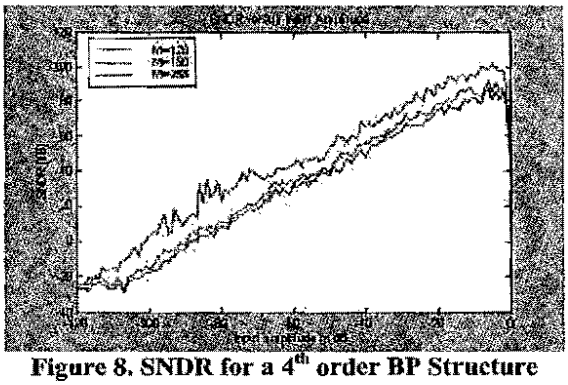


Figure 8. SNDR for a 4th order BP Structure

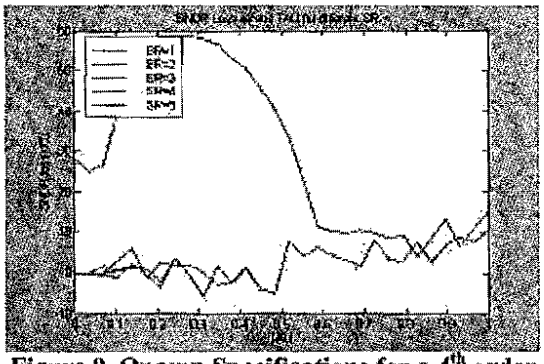
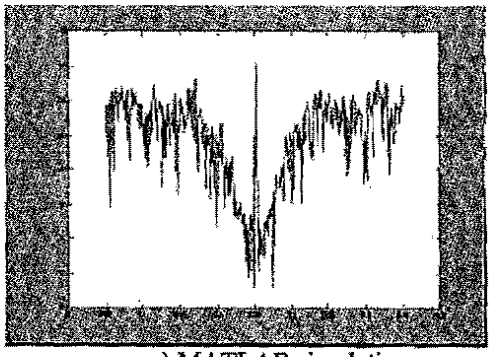
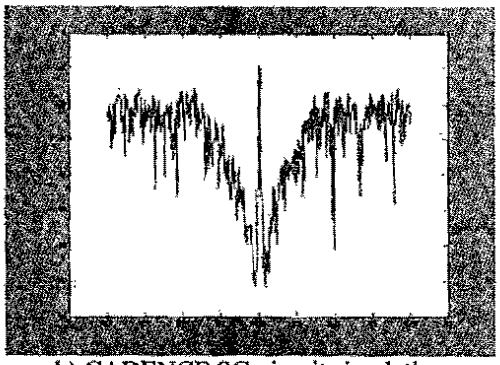


Figure 9. Opamp Specifications for a 4th order LP structure

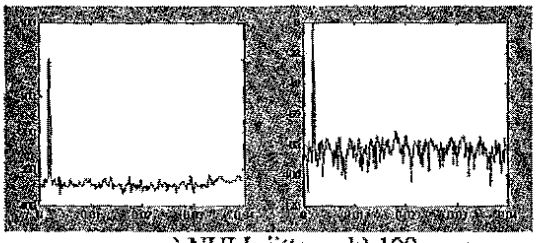


a) MATLAB simulation



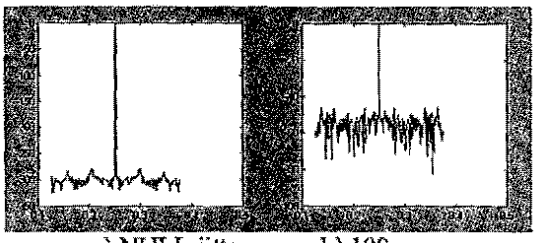
b) CADENCE SC-circuit simulation

Figure 10, 11. Band-pass Frequeucy response



a) NULL jitter b) 100 ppm

Figure 12. Jittery signals for OSR=256



a) NULL jitter b) 100 ppm

Figure 13. Jittery signals for OSR=4

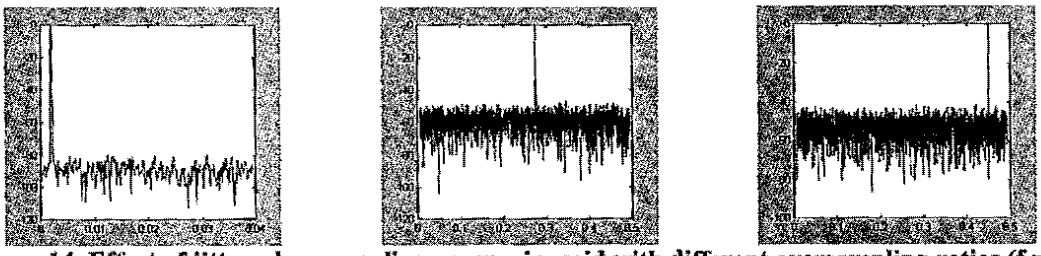
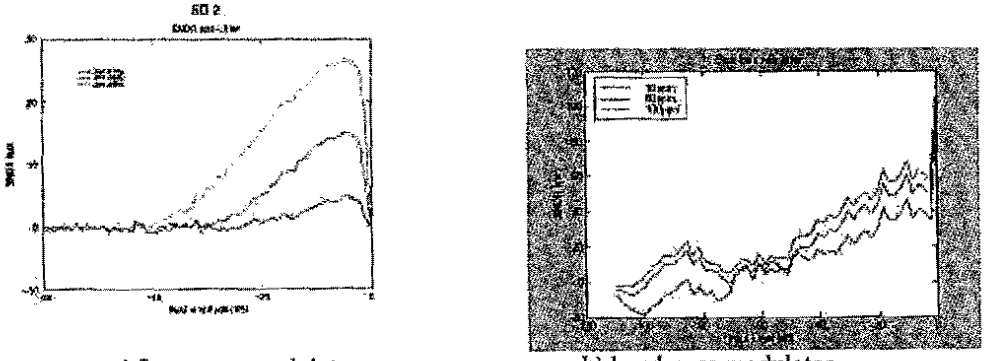


Figure 14. Effect of jitter when sampling a pure sinusoid with different oversampling ratios (f_s=1).



a) Low-pass modulator b) band-pass modulator

Figure 15 Effect of jitter on a) low-pass modulator and b) band-pass modulator.