ASIC implementation of an ARM© - based System on Chip

J. Granado, J. Chávez, F. Colodro, A. Torralba, L. G. Franquelo [1]
E. Ramos, A. Hidalgo, A. Tortolero [2]
F. Ruiz [3]

[1]Dpto de Ingeniería Electrónica, Universidad de Sevilla. Paseo de Los Descubrimientos sn. 41092-Sevilla (SPAIN)
E-mail: torralba@gte.esi.us.es
[2] SAINCO. S.A. de Instalaciones de Control. Dpto de I+DT. Tamarguillo 29. 41006-Sevilla (SPAIN)
E-mail: enrique.ramos@sainco.abengoa.com
[3] SIDSA. PTM. C/ Torres Quevedo 1. 28760 Tres Cantos. Madrid (SPAIN).
E-mail: fede@sidsa.es

Abstract

This paper presents the hardware architecture of a System on Chip (SoC) implemented in an ASIC. It has been designed for a wide range of applications and will be used in a power line modem.

A set of reusable cells based on AMBA standard has been also designed, included memory, interrupt controller and peripherals.

Presented architecture implements an ARM© processor, a 32-bit RISC processor which is becoming a RISC standard.

1. Introduction

A fundamental aspect of today's technology consists of the ever increasing capability of IC manufacturing, that makes possible to design and manufacture programmable components.[1]

In this scenario, System on Chip (SoC) software - hardware codesign is predominant in engineering of tightly coupled systems with hardware and software modules interacting to solve a certain task. [2]

In this paper is presented an ASIC implementation of a SoC.

2. Architecture description

I. AMBA hierarchy overview

The Advanced Microcontroller Bus Architecture (AMBA) specification defines an on-chip communications standard for designing high performance 32-bit embedded microcontrollers.

The AMBA specification has been derived to facilitate the 'right-first-time' development of embedded microcontroller products, minimising the silicon infrastructure and encouraging macrocells migration.

An AMBA-based microcontroller consists of a high-performance system bus, able to sustain the external memory bandwidth plus a narrower bus on which the lower bandwidth peripheral devices are located. This high performance bus, called ASB (Advanced System Bus), supports the efficient connection of processor and both on chip and off-chip external memory interfaces [3].

In the other hand, the APB (Advanced Peripheral Bus) is optimised for minimal power consumption and reduced interface complexity to support peripheral functions with a low bandwidth requirements.

II. ASB Subsystem

This section describes the architecture of the ASB sybsystem selected in our implementation.

ASB uses a clock frequency of 24 MHz. Internal bus data is 32-bit width and address bus 20-bit width.

Figure 1 shows the functional diagram of ASB subsystem. It is composed by the following cells:

ARM7TDMI

This cell is the unique master component in the ASB.

On-chip & Off-chip Memory Controller

These cells are responsible for controlling internal (ROM and RAM) 32-bit memories, and 8-16 bit external memory.

On-chip Memory blocks

The SoC implements embedded 2 KByte ROM and 8 Kbyte RAM memories.

External interface controller

It is in charge of making the interface between the internal AMBA architecture and external interfaces.

Interrupt controller

The Advanced Interrupt Controller (AIC) cell drives interrupt input lines of ARM© processor so as to enable system programmers to have an easy mechanism to control peripherals accesses.

ASB decoder

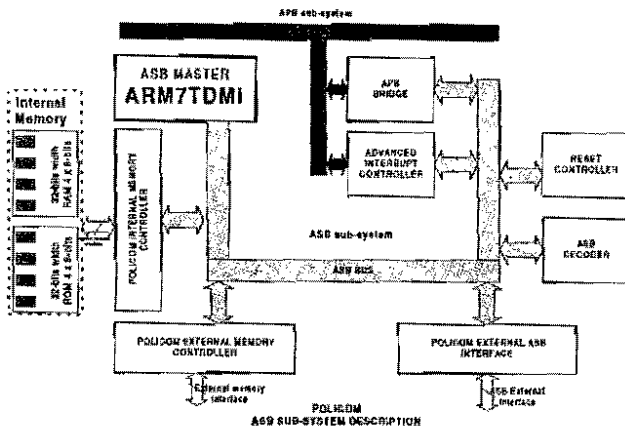The decoder in an AMBA system is used to perform a centralised decoding function.
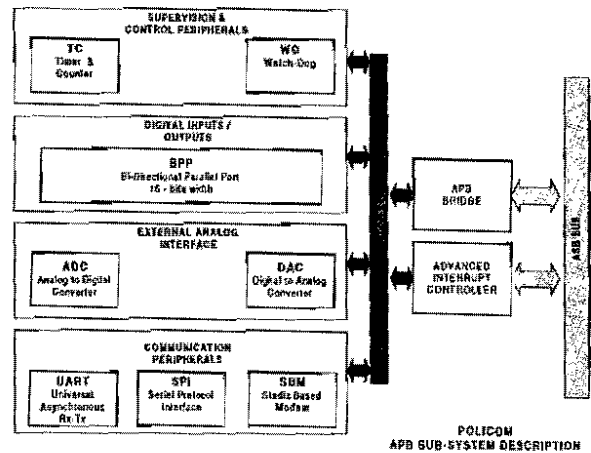
Fig. 1. ASB description

Fig. 2. APB description

APB bridge

The APB Bridge is required to convert ASB transfers into a suitable format for the slave devices on the APB. The Bridge provides latching of all address, data and control signals, as well as further decoding to generate slave select signals for the APB peripherals. The APB Bridge is the only bus master on the APB. In turn, the APB bridge is a slave on the ASB.

Glue logic

It is composed of some cells that implements several minor functions (reset controller, freq. scaler, etc).

III. APB Subsystem

The APB has general purpose cells with an important silicon resources consumption in cells involved in external interfacing and communication (UART, SPI and parallel port, and a base-band FSK-SFSK modulator-demodulator). It also includes analogue conversion interfaces (ADC and ADC), as well as timers and a watch dog cell.

Every ASB and APB cell (exeept the ARM processor and analogue interfaces) have been specially designed for this application.

3. Software architecture description

The embedded processor ARM7TDMI supports software architecture version 4 T defined by ARM Ltd. [1]. This architecture involves execution modes and exception handling.

I. On-chip RAM memory map

The internal RAM is divided in the following areas depending on the functionality (Fig. 3.):
– Interrupt Vector Table (IVT).
– Interrupt Priority Table (IPT).
– Software Interrupt Vector Table (SWVT).
– Reserved Memory Area (RMA).
– User Data Area (UDA).
– User Stack (US)
– Supervisor Stack (SS).
– IRQ Stack (IS).

In our implementation the Internal RAM configuration has been chosen in order to minimise any type of risk, such an IVT over-write error, due to the stack overflow.

The Interrupt Vector Table (IVT)

This table contains the addresses, also called IRQ vectors, of the interrupt attention routines which will serve every IRQ source enabled to interrupt the ARM processor. It is allocated at the bottom of the Internal Ram.

The Interrupt Priority Table

This table is allocated in internal RAM and contains the priority of each interrupt source.

The Software Interrupt Vector Table

The Software Interrupt Vectors allows to know where is the routine which will attend the Software Interrupt invoked by the programmer, using a SWI instruction (Software Interrupt).

Stack model

The model chosen for the architecture can be described, in ARM terminology, as 'full descending'. This stack model has been chosen as it is the unique model allowed in Thumb execution context. The stack area is allocated in the highest position of the internal RAM.

II. On-chip ROM memory

In this prototype, embedded ROM just contains: system code (exception handlers) and test routines (6 routines for self-testing).
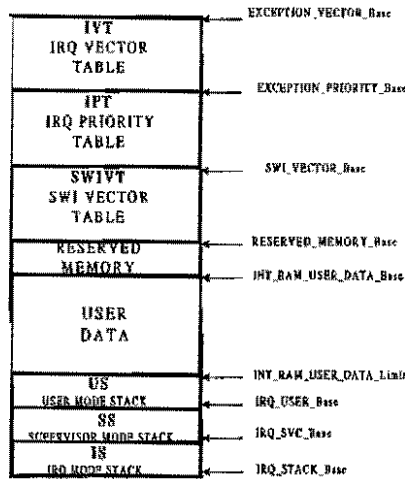
The internal ROM map is shown in figure 4.

Fig. 3. Ou-chip RAM distribution

III. Exception handling

The embedded ARM7TDMI implemented supports the following types of exceptions and has a privilege mode for each type of exception [4]. They are:

-   Reset: this exception is provoked when the processor's reset is asserted.
-   Software Interrupt: The software interrupt instruction (SWI) enters Supervisor mode to request a particular supervisor function.
-   Data Abort: A reset is performed if this exception occurred. It can happen due to an invalid memory access.
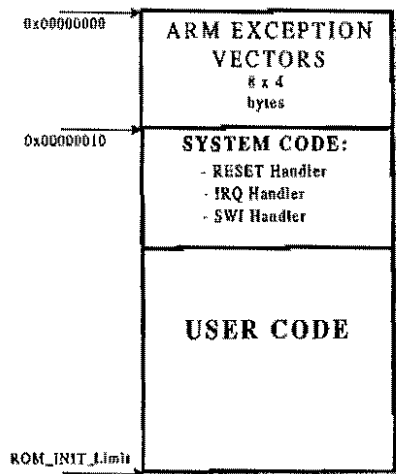-   Two interrupt types have been implemented: IRQ and FIQ.

Fig. 4. On-chip ROM map

4. Chip features

General

Power supply of 3.3 V. with an unique external clock of 24MHz. This frequency is internally divided to obtain 8MHz for the APB bus.

Processor

The embedded processor is an ARM7TDMI which has been clocked at 24MHz . Its 32-bit RISC architecture provides 20MIPS with a low power consumption It is able to access in three different data bus widths (8,16 or 32) and can operate in two execution modes, THUMB® or ARM®, providing a high density codification for embedded software implementation, reducing SoC costs.

The presented architecture implements the embedded ICE™ macrocell, which allows the embedded ARM® core to be deeply debugged [5]. It also provides real time address and data dependant breakpoints, single stepping, full access and control of CPU as well as full access to ASIC system.

On-chip Memory

About 2KByte ROM and 8KByte RAM.

Interrupt management

The AIC cell can drive up to 18 maskable interrupt lines from peripherals to ARM® processor. Priority can be controlled either using hard information or soft information. Interrupts are doubly vectored, with an user programmable Internal Vector Table.

Off-chip Memory Controller

The presented SoC provides an internal cell which allows external memory connection with an user programmable interface (both access time and block configuration). Different types of external memories (EEPROM, RAM, FLASH, etc) can be connected.

Timers and Watchdog

SoC timers support software pre-charge and hardware interrupt generation. Programmable Watch Dog can be used to avoid system control loss, ensuring a correct reset in this kind of situations.

Communications and external interface

One of the key aspects of the SoC presented in this paper is the high performance external interface implemented.

From the point of view of the communication channels, the chip provides a full modem UART (based on PCI6550D, PC compliant) to be connected to an external V.24 interface. In addition, a SPI serial interface is integrated in order to make easier to access to an external SPI-EEPRO's memory. Both serial communication devices are fully programmable, including interrupt generation.

There is also a digital on-chip signal processing cell which is able to demodulate a base band signal provided from an external AFE (Analogue Front End) to perform FSK/SFSK demodulation. As a

consequence, a full Power Line Modem (CENELEC 50065-1, 30KHz-140KHz) can be built if a suitable external AFE is connected.

Programmable parallel ports have also been included to enable easy external interface.

Concerning to the AMBA external compatibility, the internal architecture can control up to 4 external ASB slaves, including external interrupt generation.

Analogue interface

In order to improve chip functionality one 8 bits DAC and 8 bits ADC (100KS/s) have been implemented. These cells are provided from ATMEL library.
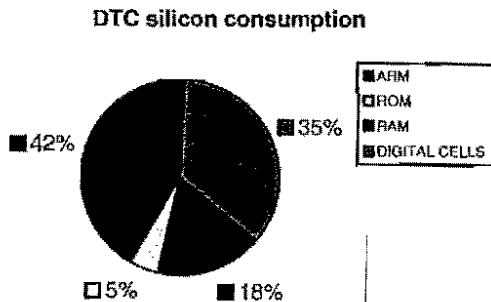
DTC silicon consumption

Fig. 5. Silicon area distribution

5. Results

Figure 6 shows the ASIC. The four main region of the chip have been pointed out: SRAM, ROM, ARM[©] processor and peripheral area. Core area is $25mm^2$ distributed as it is described in figure 5.
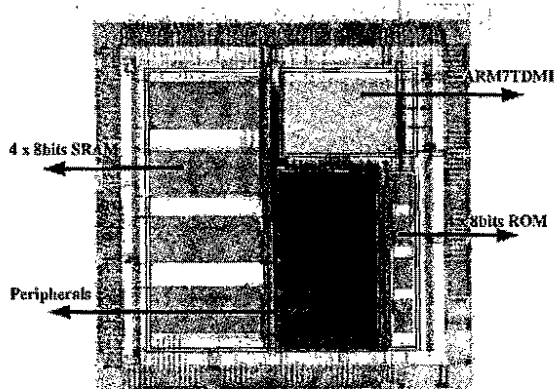
Fig. 6. Lay-out

In order to check the correct operation of the test chip manufactured, a test board has been designed. This test board is depicted in figure 7, and it contains different types of memories (Flash, SRAM and EPROM), external connector (UART, SPI, parallel port, ARM[©] ICE[TM] and analogue interfaces) and several configuration jumpers. This board enables an easy access to the test chip pins by means of connectors.
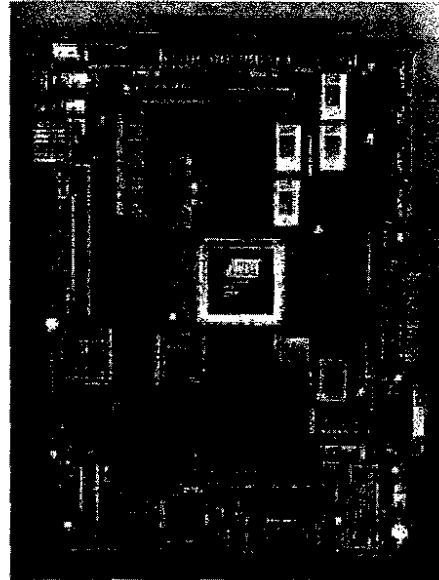
Fig. 7. Test board

The ASIC has been fabricated using the ATMEL-ES2 0.5 µm CMOS technology. First prototype arrived in the late March and chip tests have shown full functionality. The FSK/SFSK modem is the only cell that is still under test.

6. Conclusions

A System On Chip implementation has been described in this paper, pointing out the processor architecture.

A test chip has been fabricated and preliminary tests results show full functionality.

7. Acknowledgement

8. References

[1] F. Balarin, M. Chiodo "Hardware-Software co-design of embedded systems".
[2] J. Rozenblit, K. Buchenrieder. "Codesign: computer aided software/hardware engineering". IEEE Press
[3] AMBA Specificaion. ARM-IHI-0001 D, issue: April 1997.
[4] ARM[©] Arehitecture Reference Manual. ARM-DDI-0100B. ARM[©] Ltd. Dave Jaggar. Prentice Hall 1996. ISBN 0-13-736299-4
[5] Multi-processor EmbeddedICE[TM] Interface Unit. Release 1.3. User Guide. ARM[©] Ltd. Dec. 1998