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A true low voltage class-AB current mirror

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Abstract: Class-AB circuits, which are able to deal with currents which are orders of magnitude larger than their quiescent current, are good candidates for low-power analog design. This paper presents a new, simple, class-AB current-mirror, based on the Flipped Voltage Follower [1]. In the authors knowledge this is the first class-AB current-mirror which operates with a supply voltage smaller than two transistor threshold voltages without an additional clock signal or voltage doubler. Experimental results are provided which show proper operation at 1.5 V in a 0.5 μm standard CMOS technology.

Keywords: analog CMOS integrated circuits, class-AB current mirrors, low-voltage analog design

Classification: Integrated circuits

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1 Introduction

The proliferation of portable and mobile devices has made low power a key requirement in electronic designs. In addition, for digital systems, power consumption is tightly related to voltage supply, so that low power digital systems have a low supply voltage. Although different supply voltages can be used for the analog and the digital parts in a mixed signal design, this is not a convenient solution, as special interface circuits between them are required, and it also complicates the (on-chip and off-chip) design and layout

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of the supply sources.

Class-AB circuits are characterized by low quiescent power consumption and high driving capability, taking power from the supply sources only when the load requires it, making class-AB circuits good candidates for low-power analog design. Class-AB current mirrors have been widely used in analog and digital designs. The classical class-AB current mirror is based on a four transistor translinear loop (Figure 1 a) [2] which accurately determines the bias voltage at the input terminal and the quiescent current through transistors M1 to M4. Unfortunately, this circuit requires a high supply voltage, as two gate-to-source voltages (and two current sources) are stacked between the supply rails. In [3], a true low-voltage CMOS class-AB current mirror (Figure 1 b) was proposed. However, this circuit requires a switched capacitor biasing network with a high voltage clock (the authors claimed that, for low voltage operation, a clock booster could be necessary to properly drive the switches in the biasing network).

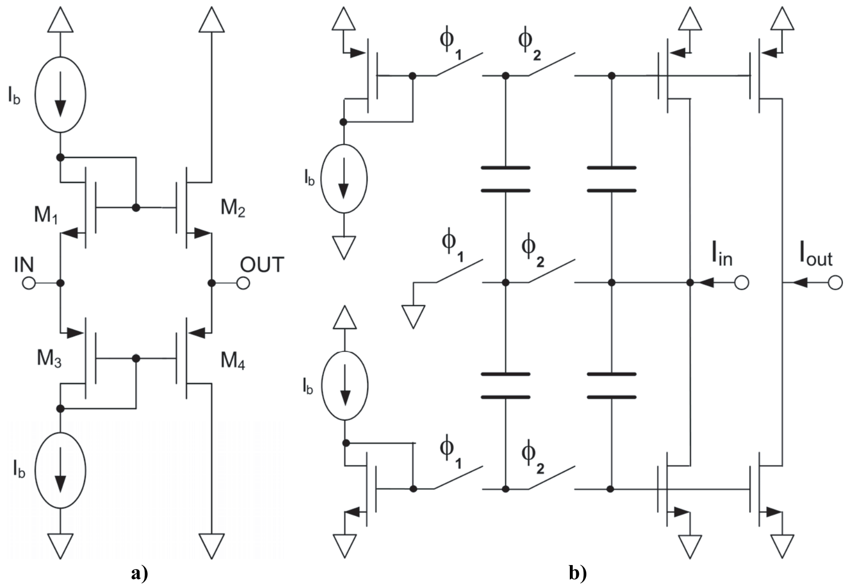

Fig. 1. a) Conventional class-AB current mirror. b) Low-voltage class-AB current mirror in reference [3].

2 Proposed Current Mirror

Figure 2 shows the proposed class-AB current mirror. Suppressing transistors M_1, M_5 and M_6 in the circuit of Figure 2, the resulting circuit constitutes a low-voltage current mirror based on the FVF [1]. To be able to copy a large positive input current $I_{in} = I_{MAX}$, the biasing current sources I_b should be greater or equal than I_{MAX}, precluding a class-AB operation.

However, transistor M_1 is able to sink a large current, allowing I_b to have a small value. The current through transistor M_1 can be copied to the output by means of the current mirror $M_5 - M_6$. The resulting circuit is a low-voltage class-AB current mirror.

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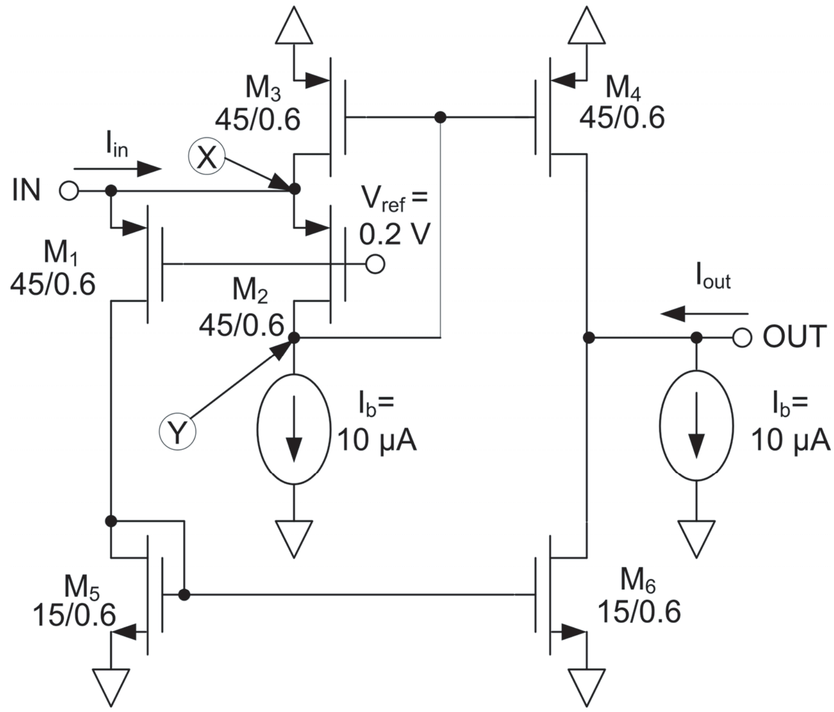

Fig. 2. Proposed class-AB current mirror.

Assuming a capacitive load and an ideal input voltage source, the stability of the proposed current-mirror is determined by the stability of the FVF section [1]. If the current source I_b is implemented by means of a simple current mirror, the stability condition for the FVF section leads to $C_X/C_Y < g_{m2}/(4g_{m3})$, where C_X and C_Y are the equivalent capacitances at nodes X and Y, and g_{mi} is the small-signal transconductance of transistor M_i. This condition is easily achieved by proper sizing of the relative W/L ratio of transistors M_2 and M_3.

Obviously, the output resistance of the circuit in Figure 2 can be increased by means of cascode transistors with normal or active biasing. These techniques are proposed elsewhere and we will not insist on them here.

3 Experimental results

The circuit in Figure 2 has been designed using a 0.5 μm CMOS standard technology. Transistor sizes and biasing currents are shown in the figure. Figure 3 a shows the chip microphotograph. The samples were measured using a 10 KΩ resistor tied to 0.75 V in parallel with an equivalent 18 pF capacitor.

Figure 3 b shows the transient response for a 1 MHz, 100 μA peak-to-peak sinusoidal input signal, showing that the current mirror is able to copy alternate currents with a maximum value which is one order of magnitude superior to its quiescent current. The measured THD for a 100 kHz, 100 μA peak-to-peak sinusoidal input signal was −61 dB, dominated by the third harmonic (Figure 3 c). The −3 dB frequency was located beyond 10 MHz.

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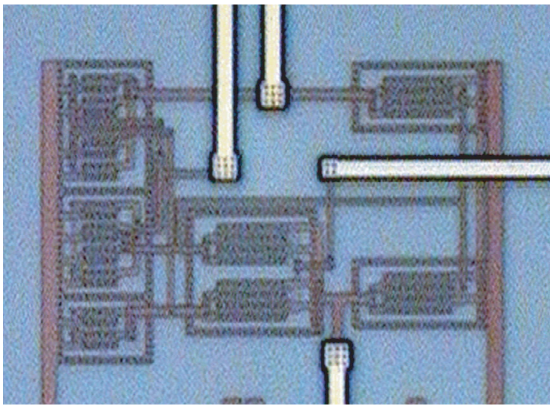
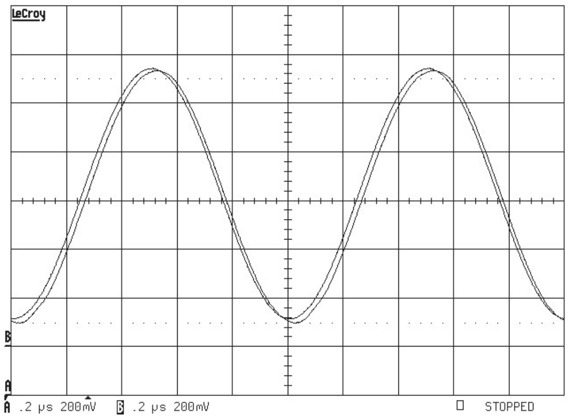
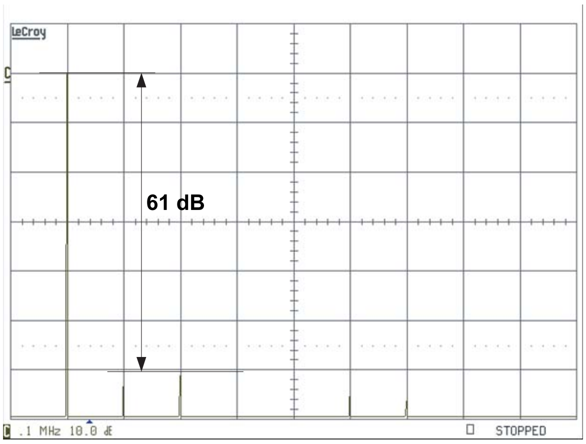


a)



b)



c)

Fig. 3. a) Chip microphotograph. b)Transient response for the proposed class-AB current mirror (1 MHz, 100 μA peak sinusoidal input signal). c) Output signal spectrum for a 100 kHz, 100 μA peak-to-peak sinusoidal input signal.

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4 Conclusion

A new simple low-voltage class-AB current mirror has been shown, based on the Flipped Voltage Follower cell. Experimental results show that this circuit is able to copy currents up to one order of magnitude superior to its biasing current with a 1.5 V supply using a 0.5 μm CMOS process. The current mirror presents a good linearity with a large bandwidth.

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