Unified RTN and BTI statistical compact modeling from a defect-centric perspective

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***Abstract*— In nowadays deeply scaled CMOS technologies, time-dependent variability effects have become important concerns for analog and digital circuit design. Transistor parameter shifts caused by Bias Temperature Instability and Random Telegraph Noise phenomena can lead to deviations of the circuit performance or even to its fatal failure. In this scenario extensive and accurate device characterization under several test conditions has become an unavoidable step towards trustworthy implementing the stochastic reliability models. In this paper, the statistical distributions of threshold voltage shifts in nanometric CMOS transistors will be studied at near threshold, nominal and accelerated aging conditions. Statistical modelling of RTN and BTI combined effects covering the full voltage range is presented. The results of this work suppose a complete modelling approach of BTI and RTN that can be applied in a wide range of voltages for reliability predictions.**

Keywords—CMOS; BTI; RTN; defects; modelling; characterization; Reliability

I. INTRODUCTION

Time-Dependent Variability (TDV) in deeply scaled CMOS technologies has become a serious concern that negatively impact device and circuit performances [1]. TDV includes, among others, transient effects such as Random Telegraph Noise (RTN) [2,3] and Bias Temperature Instability (BTI) [4,5]. Because of the common origin of both phenomena [5], i.e., charge trapping/detrapping in/from defects in MOSFETs, they should be modeled together to improve the accuracy in evaluating circuit reliability [6]. However, the stochastic nature of defects requires that many devices at the same conditions have to be measured to perform complete statistical studies. Moreover, RTN and BTI are strongly dependent of the biasing conditions of the devices, then, a complete characterization of both phenomena requires the measurement of many devices at several biasing conditions. From the above it is concluded that statistical studies of RTN and BTI requires advanced characterization strategies for massive device characterization in reasonable measurement times. The most extended solution for this problem is the use of designed array-based Integrated Circuits (ICs) to parallelize the measurements and drastically reducing the effective time required for the statistical characterization in many devices [7-9]. In this work, we take advantage of the ENDURANCE chip [10] and a flexible characterization setup [11] to measure RTN and BTI from the near threshold until elevated stress voltages. Also, the nominal operating conditions of the devices are included in the study. From the experimental results the interplaying role of RTN and BTI is discussed. Moreover, both phenomena are statistically modeled using a common framework that fully describes the simultaneous impact of both phenomena in a wide voltage range. The physical interpretation of the model parameters and their dependences with the measurement conditions are provided.

II. EXPERIMENTAL CHARACTERIZATION

Devices used for this work were pMOS transistors with W/L=80nm/60nm. First, the I_D-V_G characteristic was measured to obtain the initial threshold voltage of each device V_{th0}. After that, devices were subjected to a Measurement-Stress-Measurement (MSM) scheme [12] (Fig. 1a). The stress phases were applied with duration of t_S=1s, 10s, 100s and 1000s and a gate voltage Vs=-1.2V, -1.5V, -2V and -2.5V while the other terminals were grounded. Although we will refer to the stress phase when we apply the voltage V_S to the device at the gate, because this is the usual nomenclature, however, in the case of V_s = -1.2V we cannot consider that the devices are actually subjected to accelerated electrical stress, since they are polarized under nominal operating conditions. During the measurement phases that follow the stress phases, with a duration of t_m=100s, the drain current was continuously measured applying Vm=-0.6V to the gate and V_D=-100mV to the drain. From this current, the threshold voltage after the stress, V_{thf}, was calculated with the method presented in [11]. To extend the studied range of voltages, the data presented in [10] at VS=-0.6V is also included in our analysis. One of the advantages of our test scheme (i.e. ENDURANCE chip + flexible characterization set-up), whose details are explained in [9], is that the stress phase of many devices can be parallelized, so that the required testing time is drastically reduced. In this work, 200 devices were tested for each VS condition, which means that more than 100 days would have been required without parallelization. However, using our approach, all the measurements were performed in less than one week. For each device, the threshold voltage shift $\Delta V_{th}=|V_{thf}|-|V_{th0}|$ was calculated to evaluate the effect of the stress in the device. Fig. 1b and Fig. 1c show examples of ΔV_{th} as a function of the measurement time, tm, for the cases of V_S=-1.2V (the nominal operation voltage of the considered technology) and V_S=-2.5V. It can be observed that, at V_S=-1.2V, ΔV_{th} alternates between

two different levels, which indicates that RTN is dominating the Vth fluctuations (Fig. 1b); however, for V_S=-2.5V several Vth drops can be observed, which correspond to the emission of charges that have been trapped during the previous stress phases, (Fig. 1c), which is typical of BTI.

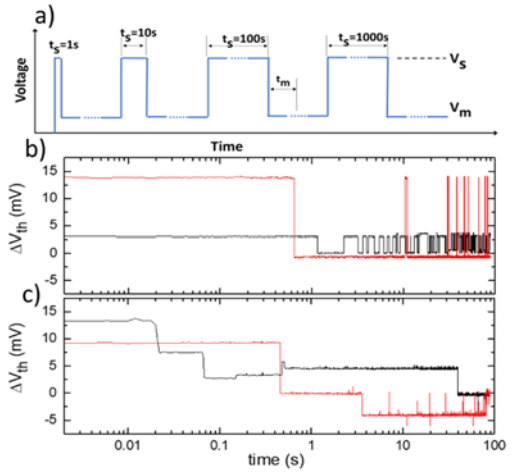

Fig. 1. (a) MSM scheme used to investigate RTN and BTI in pMOS devices. b and c) ΔV_{th} evolution in 2 pMOS devices (W/L=80nm/60nm) measured at V_m = –0.6V, for the cases of (b) V_S = –1.2V and (c) V_S= –2.5V. ΔV_{th} is defined as the difference between $V_{th}(t_m)$ and V_{th} measured on the pristine device.

Results of Fig. 1b and c are illustrative examples of our measurements, however due to the stochastic behavior of defects large spread is expected in measurements performed under nominally identical conditions. Therefore, for a useful modeling of the phenomenology it is convenient to statistically analyze the results. Is for that reason than Fig. 2 shows the ΔV_{th} cumulative distribution functions after tests at V_S= –1.2V and V_S= –2.5V of different duration, t_S. Positive/negative values of ΔV_{th} can be attributed to a net trapping/detrapping process during the test. The symmetry of the distributions at V_S=–1.2V hints at a similar number of trapping and detrapping events, which is consistent with the dominant presence of RTN, as shown in Fig. 1b. Many devices show ΔV_{th}=0, which indicates that either there are no defects in the device or, if there are, they do not effectively change their occupancy state during the measurement. For V_S=–2.5V, ΔV_{th} rapidly increases with t_S because of the larger trapping probability for larger stress times. Trapping also increases (and, thus, ΔV_{th}) with V_S (Fig. 3a). In Fig. 3b, the shift of the distributions to lower values as t_m increases indicates the progressive detrapping of charges that were trapped during the stress. As in Fig. 2, the distributions in Note that for all the ΔV_{th} distributions of Fig. 2 and Fig. 3 ΔV_{th} is negative in the low percentile tails, which implies that a net detrapping is not negligible. Therefore, even for the most aggressive stress conditions applied (V_S=-2.5V) detrapping can be relevant and consequently should be considered for modeling purposes.

III. MODELLING THE VTH DISTRIBUTIONS

To describe all these observations, a simple model, based on the trapping/detrapping of charges in/from defects, is presented below, extending the applicability of our previous approach. The starting point is our previous work [13], where we demonstrated that in near-threshold biasing conditions, ΔV_{th} distributions can be modeled considering eq.1

$$\Delta V_{th} = \sum_{i=1}^{N_0} \eta_{0,i}(oc_i(t_m) - oc_i(t=0) + randn(\sigma) \qquad eq.1$$

where N_0 is the number of active defects in the device before biasing and $\eta_{0,i}$ is the V_{th} shift caused by the trapping/detrapping in the i-th defect. oc_i is the defect occupancy state, which is 1, if occupied, or 0, if empty. The term randn(σ) represents a random number (from a Gaussian distribution with mean value 0 and standard deviation σ), which is included to account for the background noise in the experimental setup. We consider that N_0 and η_0, follow Poisson and exponential distributions respectively [14]. In [13] was demonstrated that V_{th} shift distributions related to RTN can be modeled using eq. 1 considering that the mean values of the N_0 and η_0 distributions are $\langle N_0 \rangle$=1.37 and $\langle \eta_0 \rangle$=3.2mV, respectively. Note that, in that case, low voltages were applied, so that BTI-related trapping was expected to be negligible. However, in the case of the voltage range in this work (that covers from nominal to high stress voltages), eq.1 is not enough to describe the ΔV_{th} distributions, because the trapping probability increases with the applied voltage. Consequently, eq.1 has been modified, adding an additional summation term, to consider this trapping probability increase at larger voltages, leading to eq.2

$$\Delta V_{th} = \sum_{i=1}^{N_0} \eta_{0,i}(oc_i(t_m) - oc_i(t=0)) + \sum_{i=1}^{N_s} \eta_{s,i} + randn(\sigma) \quad eq.2$$

The first and third terms are those already included in eq. 1 (low voltage range), whereas the increase of the trapping probability is accounted for in the second summation term. There, N_S is the number of defects that have been occupied in the device at larger voltages and $\eta_{s,i}$ is the V_{th} shift linked to these defects. As for N_0 and η_0, Poisson and exponential distributions are also assumed for N_S and η_S, with mean values $\langle N_S \rangle$ and $\langle \eta_S \rangle$, respectively. With these assumptions, eq. 2 is able to reproduce the experimental ΔV_{th} distributions in Fig. 3.

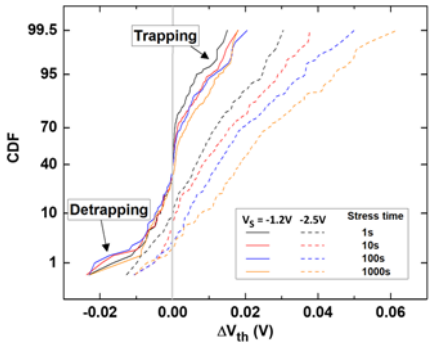

Fig. 2. Examples of ΔV_{th} distributions measured at t_m=100s for different values of V_S and t_S. 200 devices are considered in each distribution.

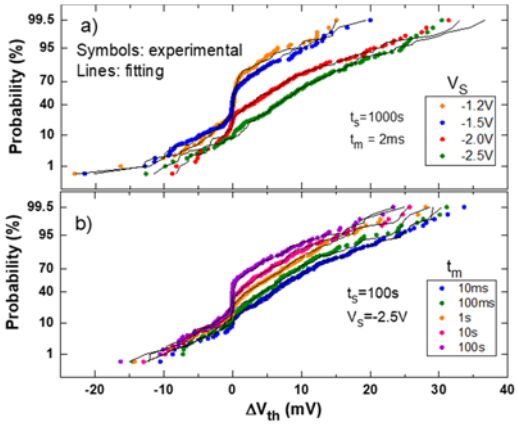

Fig. 3 ΔV_{th} distributions obtained for (a) different V_S and (b) different measurement times, t_m. Lines show the fittings obtained with eq. 2.

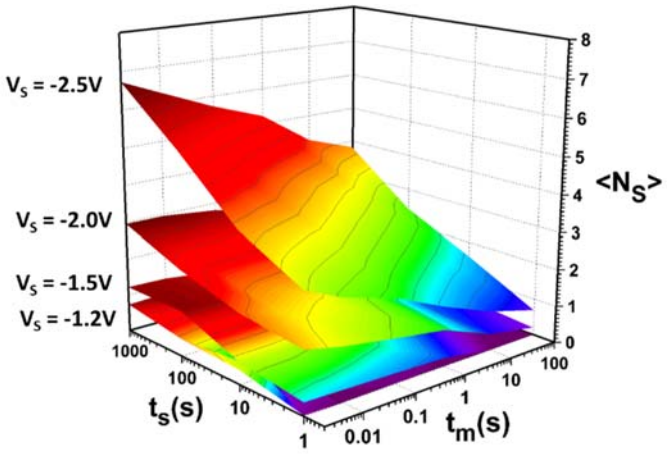

Fig. 4. <N_S> as a function of the stress and measurement conditions V_S, t_s and t_m.

The only fitting parameters here are <N_S> and <η_S>, because the values of <N_0>=1.37 and <η_0>=3.2mV have been fixed to the values determined from the measurements at low voltages [13], since they must be kept unchanged to ensure that eq. 2 is consistent in all the voltage range (high and low voltages). The good fitting of the experimental data demonstrates that the inclusion of the second summation, despite its simplicity, is sufficient to describe the ΔV_{th} distributions measured when RTN and BTI aging are simultaneously active. Then, clearly the effects of stress must be reflected in the N_S and η_S distributions, that is, in the <N_S> and <η_S> parameters.

The full modelling of the ΔV_{th} distributions requires the evaluation of their dependencies on the biasing conditions, so that the voltage dependencies of <N_S> and <η_S>have been analysed. Fig. 4 shows <N_S> as a function of the stress t_s, and measurement, t_m, times for different values of V_S. Note that <N_S> is the only parameter required to describe the statistical distribution of N_S, therefore, the results in Fig 4 are enough to estimate the number of defects that in a device will be charged as a consequence of the stress. In the time range investigated, <N_S> logarithmically increases with t_s, due to charge trapping during the stress, and logarithmically decreases with t_m , due to detrapping of previously trapped charges during measurement at lower voltages. As expected, the number of defects that trap charges increases with V_S. If we compare the results of Fig. 4 with those at lower voltages (i.e., <N_0>=1.37), it is clear that for $|V_S| \leq 1.5V$ the number of defects, <N_S>, is smaller than <N_0>, though the contribution of <N_S> should not be considered negligible. If $|V_S| \geq 2V$, <N_S> is clearly larger than <N_0>, but even in the most aggressive biasing tested condition (VS=-2.5V, ts=1000s and tm=10ms), its value (<N_S>=6.7) is not large enough to consider that the contribution of <N0> is negligible. Then, from this discussion, we can conclude that for the description of the ΔV_{th} in a large voltage range (from near-threshold up to voltages much larger than the nominal), the whole set of active defects should be considered. That is, those defects that would be only observed at low voltages (leading to RTN) and those that will be only activated at the larger voltages (observed as BTI).

In order to provide a simple kinetics model valid for the considered technology, <N_S> has been described using the following semiempirical expression based in the Universal Relaxation Function for BTI [13]

$$< N_S > = \frac{K \cdot (t_S)^{\alpha}}{1 + B(t_m/t_S)^{\beta}} \qquad eq.3$$

Fig. 5a shows the fittings of <N_S> to eq. 3 for t_s=1,000s, while the extracted values of the parameters α, β and B are given in Table 1. Fig. 5b shows that the K parameter fits to a power law with V_S.

$\|V_S\|$ (V)	α	B	β
1.2	0.22	11.49	0.68
1.5	0.26	2.67	0.34
2.0	0.098	2.88	0.32
2.5	0.066	2.01	0.15

Table 1 : α, β and B values of eq. 3 obtained at the different voltage conditions tested.

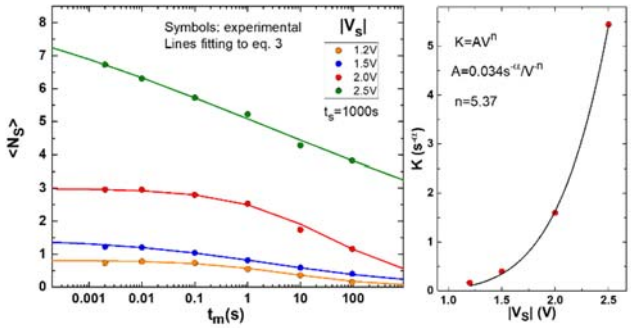

Fig. 5.(a) <N_S> fitting to eq. 3 for t_s=1,000s. (b) The K parameter of eq. 3 follows a power law dependence with V_S.

Finally, we have investigated the dependence of <η_S> with the voltage conditions. It should be remarked that <η_S> is the only parameter needed to evaluate the η_S distribution, therefore it is enough to describe the magnitude of the V_{th} shift at the larger voltages. The symbols in Fig. 6 shows the estimated <η_S> at t_m=2ms and ts=100s for the investigated V_S from the fitting

of the Vth shift distributions. No dependence of $\langle\eta_S\rangle$ on V_S is observed. Interestingly, the values found are similar to those reported in [14] (black line), where a 'manual' analysis of all the temporal traces measured after the stress (as those in Fig. 1) was done to directly assess the ΔV_{th} contribution of individual defect discharges, which supports the validity of our approach. Note also that the $\langle\eta_S\rangle$ values are close to $\langle\eta_0\rangle$. This similarity indicates that the charging/discharging of defects produces a ΔV_{th} that does not depend on the gate voltage in a large voltage range. The results in Fig. 4 and Fig. 6 show that stress (i.e. large voltages) has an impact mainly on the number of active defects but a negligible effect on the magnitude of their associated Vth shift. Therefore, an accurate characterization of $\langle N_S\rangle$ is crucial for an accurate modeling, however, is not enough because the contribution of those defects acting without apply any stress can be relevant.

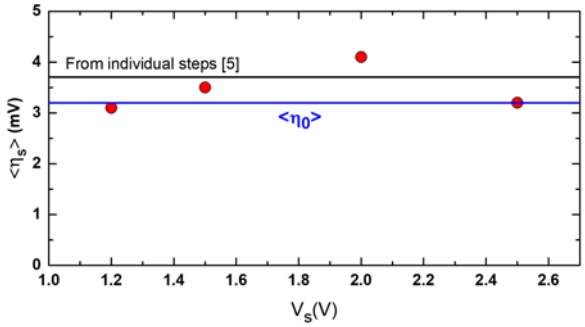

Fig. 5 Symbols: $\langle\eta_S\rangle$ as a function of V_S. The black line corresponds to the reported value in [5], which was obtained from the direct analysis of the experimental traces.

CONCLUSION

The simultaneous impact of RTN and BTI has been statistically investigated in a large range of voltage conditions. The analysis of the experimental data demonstrates that RTN and BTI coexist, though one may dominate over the other depending on the biasing conditions. A simple physics-based model, with a reduced number of meaningful parameters, has been presented. This model describes, in a wide range of biasing conditions, from near threshold to high stress voltage, covering the nominal operation conditions, the ΔV_{th} statistics when RTN and BTI are simultaneously present. The results show that the stress affects only the statistical distribution of the number of active defects, which in our model can be described with a single parameter.

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