Int. J. Electron. Commun. (AEÜ) 156 (2022) 154389

Contents lists available at ScienceDirect

Int. J. Electron. Commun. (AEÜ)

journal homepage: www.elsevier.com/locate/aeue

Regular paper

A high-voltage floating level shifter for a multi-stage charge-pump in a standard 1.8 V/3.3 V CMOS process☆

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A R T I C L E I N F O

Keywords:
Level shifter
Gate driver
CMOS
Charge pump
High-voltage compliance

A B S T R A C T

This paper proposes a high-voltage floating level shifter with a periodically-refreshed charge pump topology. Designed and fabricated in a standard 1.8 V/3.3 V CMOS process, the circuit can withstand shifting voltages from 3 V to 8.5 V with a delay response of 1.8 ns and occupies 0.008 mm^2. The proposed circuit has been used in a multi-stage charge pump for programming its voltage conversion ratio. Experimental results show that the level shifters successfully enable/disable the stages of the charge pump, thus modifying its output voltage between 5.35 V and 12.4 V for an output current of 3 mA.

1. Introduction

Different from conventional level shifters, in which only the high-rail level of the input signal is changed [1,2], floating-level shifters (FLS) slide both the low- and high-rail levels of a digital signal by a voltage V_{SSH}. Hence, if the FLS is driven by a digital signal, *IN*, comprised between ground and V_{DD}, the circuit generates a voltage-shifted version, OUT, which swings from V_{SSH} to $V_{DDH} = V_{DD} + V_{SSH}$. These circuits are typically used for driving power switches [3], as shown in Fig. 1, and in charge-pump circuits [4–6]. In these applications, the shifting voltage V_{SSH} of the FLS is usually not static; the output has to react rapidly to these changes; and the input signal *IN* is usually non-periodical.

A High-Voltage (HV) FLS can be implemented using HV CMOS processes. These processes include devices with thicker gate oxides capable of handling HV operations. This option usually comes at a higher cost than a standard low-voltage (LV) CMOS node. Also, integrating a system's HV components with previously designed LV circuitry is not a simple task. One alternative is to combine LV CMOS processes with innovative circuit solutions to achieve high-voltage-tolerant systems, although here care must be taken to maintain voltages across devices terminals below safe limits in all operation modes [7–9]. This is actually the approach followed in previous charge-pump based floating level shifters (CP-FLS) [10,11] and active/capacitive coupled floating level shifters (AC-FLS/CC-FLS) [3,8,12,13]. Simplified schematics for these solutions are shown in Fig. 2. The basic CP-FLS in Fig. 2(a) can be implemented with LV CMOS processes without the need for a high supply rail. Its output depends on the charge stored in the capacitors that are refreshed when the input signal *IN* changes. If the signal is non-periodic or low in frequency, the leakage currents discharge the capacitors, and the output logic levels are damped [11]. Also, the output cannot track voltage supply variations until the input switches. The HV AC-FLS in Fig. 2(b) uses stacked transistor techniques and requires additional circuitry for generating biasing voltages. Also, they cannot handle a wide range of shifting voltages V_{SSH}. Finally, the HV CC-FLS in Fig. 2(c) does not need bias voltages and can be implemented in LV CMOS processes. However, similar to the HV AC-FLS, it requires an additional charge pump circuit to generate the high supply rail. In this work, a HV CP-FLS with periodic charge refreshing is presented. Its operation is herein demonstrated in a practical application in which the proposed FLS is used for controlling the Voltage Conversion Ratio (VCR) of a multi-stage charge pump circuit fabricated in a standard 1.8 V/3.3 V CMOS process. The paper extends the conference contribution in [14] with new circuit analysis and experimental results. The paper is organized as follows. Section 2 addresses the design and operation of the proposed HV CP-FLS. Section 3 shows experimental results illustrating the operation and performance of the HV CP-FLS implemented in a multi-stage charge pump. Finally, Section 4 concludes the paper.

☆ This work was supported by grant PID2019-110410RB-I00, funded by MCIN/AEI/10.13039/501100011033, Spain; and by grant 310 N00014-19-12156, funded by US Office of Naval Research. David Palomeque-Mangut's work has been supported by the Spanish Government (FPU18/00247).

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https://doi.org/10.1016/j.aeue.2022.154389
Received 20 May 2022; Accepted 15 August 2022
Available online 30 August 2022
1434-8411/

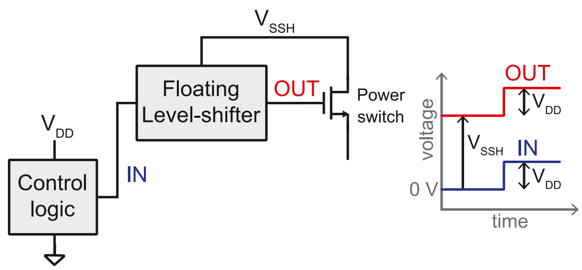

Fig. 1. Simplified representation of a floating level-shifter working as gate driver.

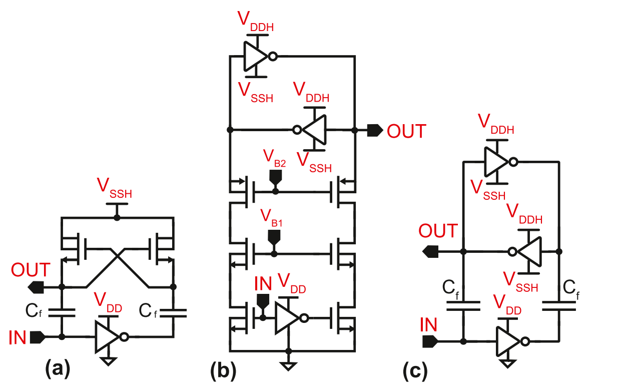

Fig. 2. Three simplified high-voltage floating level shifter (HV-FLS) topologies: (a) charge-pump based FLS, (b) actively-coupled FLS, and (c) capacitively-coupled FLS.

2. Proposed floating level shifter

2.1. Principle of operation

Fig. 3(a) shows the proposed HV CP-FLS as well as the four phases clock generator circuit. The digital signal to be shifted is denoted as *IN*, the shifting level is defined by V_{SSH}, and OUT represents the shifted output voltage. The signal *IN* is assumed to be comprised between ground and V_{DD}. The circuit consists of three main blocks: (1) a local FLS ($C_{1,2}$ and $M_{1,2}$), (2) a basic charge-pump ($C_{3,4}$ and M_{3-6}), and (3) a sample-and-hold (S&H) (transmission gates $M_{7,8}$ and capacitor C_s). Complementary clock signals clk_1 and clk_2 are in-phase with signals clk_3 and clk_4, respectively, with non-overlapping time margins at the rising and falling edges, as illustrated in Fig. 3(b). The clock signals are generated by the circuit shown in Fig. 3(a), where t_d-blocks correspond to the delays introduced by chains of inverters. This way, the non-overlapping time margin is equal to $0.5{\times}t_d$. The clocks frequency is f_{clk}. The local FLS provides the input voltage, V_3, of the S&H circuit. Signal V_3 is in-phase with clk_1 if the FLS input, *IN*, is in high state; otherwise V_3 is in-phase with clk_2. Accordingly, if *IN* is HIGH, $V_3 \approx V_{DD} + V_{SSH}$ and, otherwise, if *IN* is LOW, $V_3 = V_{SSH}$. The charge pump generates two voltage-shifted versions of the clock signals clk_3 and clk_4, named V_5 and V_6, that drive the gates of transistors M_7 and M_8, respectively. Also, it biases the bulk of M_8 and the deep n-wells of DNW-NMOS transistors. When clk_3 is HIGH (alt. clk_4 is LOW), voltage V_3 is sampled in the output capacitor C_s. Otherwise, if clk_3 is LOW (alt. clk_4 is HIGH), the charge stored in C_s is held. Note that the non-overlapping margins between clk_1 and clk_3 (similarly between clk_2 and clk_4) guarantee that signal sampling only occurs when V_3 is established.

During the sampling phase, if the *IN* signal state is LOW (alt. HIGH), C_1 (alt. C_2) stores the voltage level V_{SSH} and C_2 (alt. C_1) pumps charge to C_s. On the other hand, during the holding phase, if the *IN* state is LOW (alt. HIGH), C_2 (alt. C_1) stores the voltage level V_{SSH} and C_1 (alt. C_2) pumps charge to C_s. Regardless of signal *IN* level, the capacitor C_3 (alt. C_4) stores V_{SSH} in the hold (alt. sampling) phase and the capacitor C_4 (alt. C_3) pumps charge in the hold (alt. sampling) phase. Hence, the capacitors are refreshed at a f_{clk} rate. This allows to track time-varying shifting voltages V_{SSH} and handle non-periodic input signals *IN*.

2.2. Circuit sizing

When the input signal *IN* transitions from LOW to HIGH during the sampling phase, the output voltage $OUT(t)$ of the HV CP-FLS can be expressed as

$$OUT(t) = V_{SSH} + V_{DD}\frac{C_{1,2}}{C_{1,2}+C_s}\left(1 - e^{-t/\tau}\right), \tag{1}$$

and, when *IN* switches from HIGH to LOW, as

$$OUT(t) = V_{SSH} + V_{DD}\frac{C_{1,2}}{C_{1,2}+C_s}\left(\frac{C_s}{C_{1,2}} + e^{-t/\tau}\right), \tag{2}$$

where $\tau = R_{on}C_s(C_s/C_{1,2}+1)$ is the time constant of the circuit and R_{on} is the equivalent ON resistance of the transmission gates, given by

$$R_{on} = \frac{1}{\mu_P C'_{ox}\left(\frac{W}{L}\right)_8 V_{ov,8} + \mu_N C'_{ox}\left(\frac{W}{L}\right)_7 V_{ov,7}}, \tag{3}$$

where $V_{ov,x} = |V_{GS,x}| - |V_{TH}|$ is the overdrive voltage of transistors M_7 and M_8.

The total propagation delay of the level shifter $t_{d,LS}$ is given by

$$t_{d,LS} = t_{d,MUL} + R_{on}C_s\left(\frac{C_s}{C_{1,2}} + 1\right) \tag{4}$$

where $t_{d,MUL}$ is the delay introduced by the *IN*-controlled multiplexers in Fig. 3(a).

The circuit elements in Fig. 3 have been sized by making $\tau < 0.125/f_{clk}$, assuming a clock frequency of $f_{clk} = 10\,\text{MHz}$ and that $C_{1,2}$ is 3× larger than C_s. With these requirements, the HV-FLS approximately obtains a 25% settling error in (1)–(2) during a complete sampling phase, while keeping area and power consumption under reasonable levels for the application described in Section 3. Transistors and capacitors sizes are shown in Fig. 3.

Expression (4) only holds if the input signal, *IN*, changes during the sampling phase. However, if *IN* switches in the hold phase, an additional delay $\Delta_H \in [0, 0.5/f_{clk}]$ is introduced. In charge pumps applications, where *IN* typically switches at low speeds compared to f_{clk}, this is not a major issue and no extra measure has been adopted. In other cases where propagation delay aspects are more critical, signal *IN* should be aligned with positive edges of clk_1 to suppress the impact of Δ_H.

2.3. HV compliance in a LV CMOS process

The circuit was implemented in a standard 1.8 V/3.3 V CMOS process with deep n-well devices available. The transistors in the HV floating domain of the proposed CP-FLS can withstand voltage differences up to 3.3 V, but transient peaks during switching can cause differential voltages that exceed the nominal difference between HV supply rails. Accordingly, in the proposed implementation, the amplitude V_{DD} of the digital signal *IN* is kept below 3 V, while transistors can nominally withstand voltage differences up to 3.3 V.

The maximum absolute value of V_{SSH} is limited by the breakdown voltage of the parasitic diodes in PMOS and DNW-NMOS transistors and by the voltage compliance of MIM capacitors. PSUB-DNW and PSUB-NW junction diodes have breakdown voltages of over 13.5 V in the selected CMOS process. However, MIM capacitors have a dielectric layer with about 30 nm thickness and the probability of breakdown increases with the voltage between their terminals. To withstand higher voltages, two series MIM capacitors have been used for implementing C_{1-4} at the price of increasing area occupation.

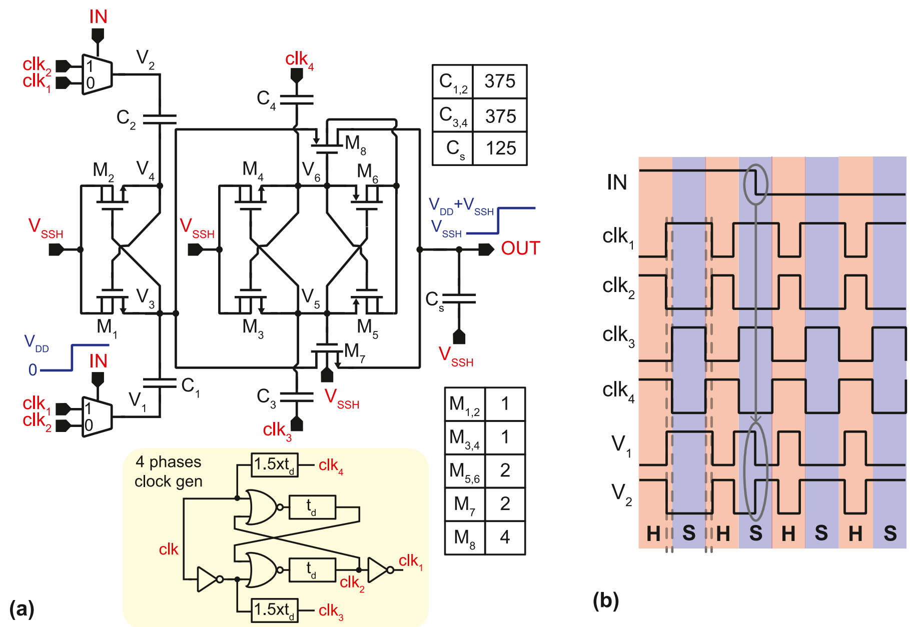

Fig. 3. (a) Schematics of the proposed high-voltage floating level shifter and the four phases clock generator. Transistors are 3.3 V devices and their widths are shown in microns, all lengths are set to 350 nm. All capacitors were implemented as two series-connected MIM structures, and their values are shown in femtofarads. (b) Time diagram of clock signals showing how switching *IN* affects voltages V_1 and V_2.

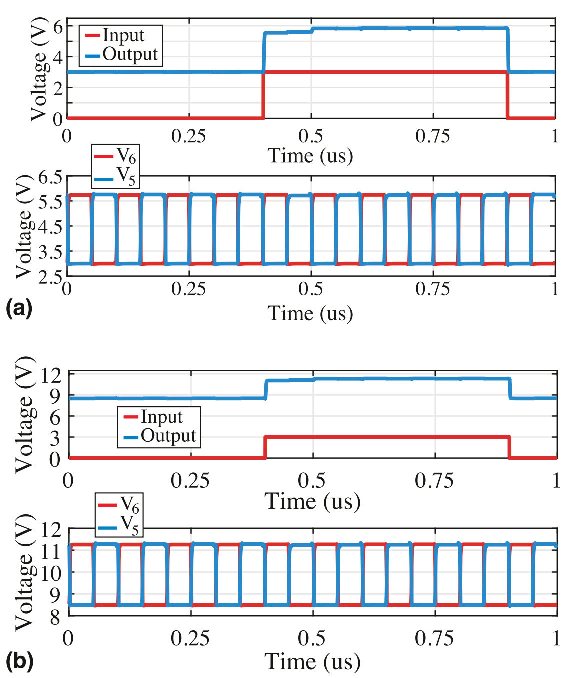

Fig. 4. Signals *IN*, *OUT* and transmission gate voltages, V_5 and V_6, of the HV-FLS.

2.4. Dynamic behavior

A post-layout view of the circuit presented in Section 3 was simulated using the Cadence Virtuoso suite. Fig. 4 illustrates the transient behavior of the proposed HV-FLS for f_{clk} = 10 MHz, V_{SSH} = 3 V (top) and V_{SSH} = 8.5 V (bottom). When *IN* switches from LOW to HIGH, the output voltage raises to a value lower than $V_{SSH} + V_{DD}$ during the first sampling period and then continuously approaches $V_{SSH} + V_{DD}$ during the next periods. This is because the sampling capacitor has no charge when *IN* is LOW and it cannot be fully charged in the first sampling phase due to the capacitive divider formed between $C_{1,2}$ and C_s, as stated in (1)–(2).

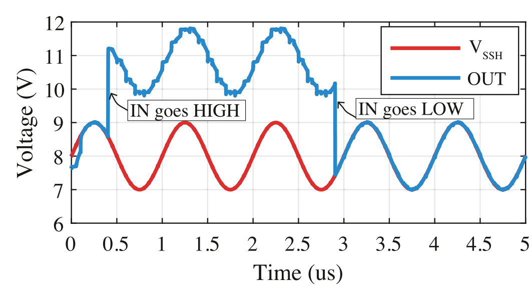

Fig. 5. Output response for a time-varying shifting voltage V_{SSH}.

Fig. 5 shows the circuit's response to a time-varying V_{SSH} signal without switching the digital input *IN*. The shifting voltage V_{SSH} is a tone with DC value of 8 V, amplitude of 1 V, and frequency 1 MHz. Thanks to the charge-refreshing topology, the node *OUT* tracks the variations in V_{SSH} even with no activity at the input *IN*.

Fig. 6(a) plots the propagation delay and the power consumption of the FLS obtained for different values of the shifting voltage V_{SSH}, assuming f_{clk} = 10 MHz. The input *IN* is a clock signal of frequency f_{in} = 1 MHz. Note that the delay is to first-order independent of V_{SSH} and amounts about 1.81 ns. The power consumption increases slightly with V_{SSH}, due to the higher losses in the parasitics of the MIM capacitors. Fig. 6(b) shows the power consumption of the FLS circuit and the non-overlapping clock generator (block not shown in Fig. 3) in terms of the clock frequency, for an input signal with frequency f_{in} = 1 MHz. As expected, the power consumption increases linearly with the clock frequency. As f_{clk} increases above the input signal frequency f_{in}, the power consumption of the clock generator dominates, in agreement with other reported solutions [11].

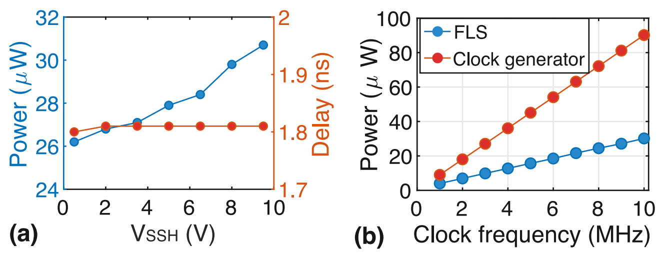

Fig. 6. (a) Propagation delay and power consumption (f_{clk} = 10 MHz, f_{in} =1 MHz). (b) Power consumption (V_{SSH} = 8.5 V and f_{in} = 500 kHz).

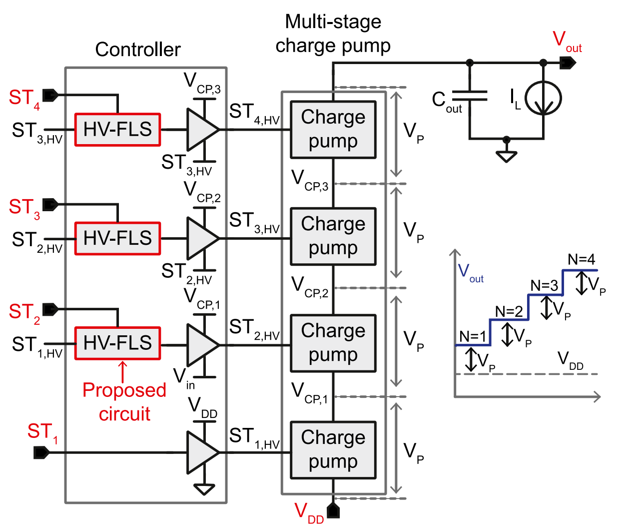

Fig. 7. Simplified diagram of the HV multi-stage charge pump with S for enabling/disabling each stage.

3. Experimental results

3.1. Application of the proposed FLS

The proposed HV-FLS is used as a building block for the voltage conversion ratio controller of a programmable multi-stage charge pump circuit. Fig. 7 shows a simplified circuit diagram. The charge pump cells use a cross-couple topology similar to the proposal in [15]. These cells also employ the proposed HV-FLS; however, in this case the dimensions of the level shifters differ from those in the VCR controller because they have to exhibit smaller settling errors and, hence, larger capacitors C_{1-4} are needed (details are available in [14]).

The controller is used for the selection of the charge pump stages based on the digital control signals ST_{1-4}. These signals take on DC levels 0, for disabling the stage, or V_{DD}, for enabling. A charge pump stage can only be activated if the previous one is enabled and, therefore, only four combinations of ST_{1-4} values are possible. Hence, if the number of active stages is $N = i$, for $i = 1, \ldots, 4$, $ST_j = V_{DD}$, for $j = 1, \ldots, i$, and $ST_j = 0$, otherwise.

The controller is composed of three of the proposed HV-FLS and four floating buffers for driving the charge pumps with the sliding voltages $ST_{i,HV}$. A single non-overlapping clock generator is shared among all HV-FLS. The level shifters are arranged in series so that the output voltage, $ST_{i,HV}$, of the ith FLS becomes the shifting level value V_{SSH} of the i + 1-th block. Table 1 shows for all possible combinations of $ST_{i,HV}$, where N is the number of enabled stages and V_p is the voltage drop across the charge pump stages

$$V_p = V_{DD} - R_{CP} \cdot I_L, \tag{5}$$

Table 1
Voltages $V_{CP,i}$ and $ST_{i,HV}$, depending on the number of stages enabled, N. V_p is defined in (5).

	N = 1	*N = 2*	*N = 3*	*N = 4*
$V_{CP,1}$	$V_{DD}+V_p$	$V_{DD}+V_p$	$V_{DD}+V_p$	$V_{DD}+V_p$
$V_{CP,2}$	$V_{DD}+V_p$	$V_{DD}+2{\cdot}V_p$	$V_{DD}+2{\cdot}V_p$	$V_{DD}+2{\cdot}V_p$
$V_{CP,3}$	$V_{DD}+V_p$	$V_{DD}+2{\cdot}V_p$	$V_{DD}+3{\cdot}V_p$	$V_{DD}+3{\cdot}V_p$
V_{out}	$V_{DD}+V_p$	$V_{DD}+2{\cdot}V_p$	$V_{DD}+3{\cdot}V_p$	$V_{DD}+4{\cdot}V_p$
$ST_{1,HV}$	V_{DD}	V_{DD}	V_{DD}	V_{DD}
$ST_{2,HV}$	V_{DD}	$V_{DD}+V_p$	$V_{DD}+V_p$	$V_{DD}+V_p$
$ST_{3,HV}$	V_{DD}	$V_{DD}+V_p$	$V_{DD}+2{\cdot}V_p$	$V_{DD}+2{\cdot}V_p$
$ST_{4,HV}$	V_{DD}	$V_{DD}+V_p$	$V_{DD}+2{\cdot}V_p$	$V_{DD}+3{\cdot}V_p$

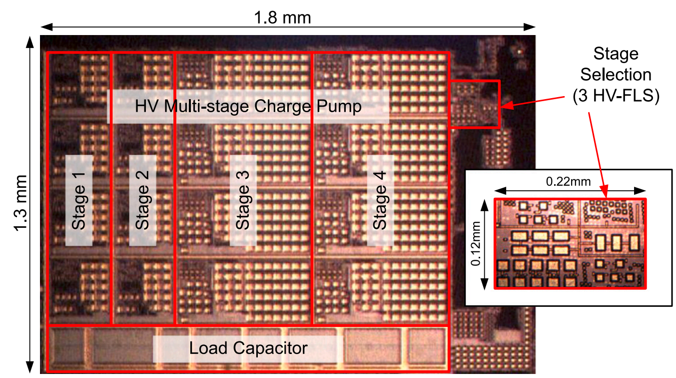

Fig. 8. Microphotograph of the multi-stage charge pump circuit, fabricated in a standard 0.18 μm CMOS process. The zoom details the stage selection unit which comprises three HV-FLS cells.

where V_{DD} amounts 3 V in this implementation, I_L is the load current, and R_{CP} is the equivalent resistance of the charge pump stages [16]. This latter depends on internal parameters and operation conditions and roughly ranges from 166 Ω to 8 kΩ in this design.

3.2. Experimental results

Fig. 8 shows a microphotograph of the four-stages charge pump circuit. The chip has been fabricated in a standard 0.18 μm 1.8 V/3.3 V CMOS process with deep n-well devices and occupies an active area of 1.8 mm×1.3 mm. The zoom shows the stage selection circuit of the charge pump, which occupies roughly 0.03 mm^2, including the three HV-FLS of Fig. 7.

Fig. 9 shows the operation of the multi-stage CP and the HV-FLS for different enabled stages. The input voltage is 3 V, I_L = 3 mA, $R_{CP} \approx 210$ Ω, and $V_p \approx$ 2.35 V. The HV-FLS clock frequency is 6.25 MHz. Fig. 9(a) shows the output voltage of the multi-stage charge pump, when the number of active stages N increases from 1 to 4 at 50 μs intervals. The different voltage levels agree with the values shown in Table 1. Similarly, Fig. 9(b–d) shows the signals V_{SSH} and OUT of the HV-FLS driving the fourth, third, and second CP stages, respectively, for the same time sequence of activated cells. Again, the level shifters update their outputs, $ST_{2-4,HV}$, according to the values shown in Table 1. When N changes, the signals settle after roughly 2 μs. This delay is essentially dominated by the internal dynamics of the charge pumps, which are much slower than the HV-FLS blocks.

Fig. 10 shows the response of the HV-FLS to a varying load current. In this case, N = 4 (all the charge pump cells are enabled), $R_{CP} \approx 210$ Ω, and the load current changes from 0.5 mA to 4 mA within 50 μs. From top to bottom, the oscilloscope screenshot shows V_{out}, $ST_{4,HV}$, $ST_{3,HV}$, and $ST_{2,HV}$. The voltage difference between adjacent signals is always V_p, as discussed in (5) and Table 1. However, V_p, and, hence, V_{out} varies with the load current. Namely, V_{out} changes from 13.6 V – for a load current of 0.5 mA – to 8 V – under a load current of 4 mA –. Even though the digital input of the floating level shifters ST_{2-4}

Table 2
Performance comparison with previously reported charge-refreshing FLS.

Reference	Process	V_{SSH}	Non-periodic *IN* signals	Delay (ns)	Energy/op (pJ)[a]	Area (mm^2)
[17]	0.5 μm HV	95 V	No	0.5	2.5[b]	1.1
[18]	0.18 μm HV	45 V	No	1.9[b]	242[b]	–
[11]	28 nm LV	0.9 V	Yes	9	0.8	0.001
[19]	0.18 μm HV	200 V	No	0.7[b]	8.1[b]	–
This work	0.18 μm **LV**	**3-8.5 V**	**Yes**	**1.8**[b]	**2.9**	**0.008**

[a]Energy/operation, calculated as power/f_{clk}.
[b]Simulation results.

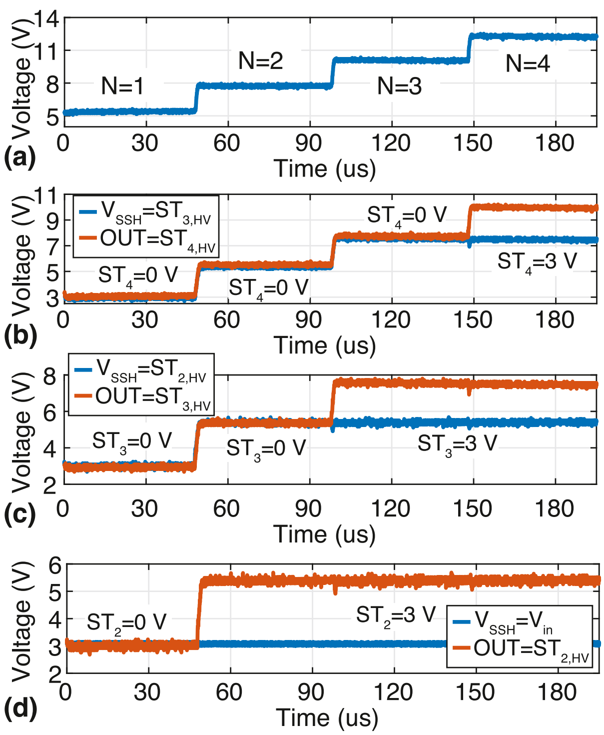

Fig. 9. Experimental measurements on the multi-stage charge pump with V_{DD} =3 V, R_{CP} ≈210 Ω, and I_L = 3 mA. Series-connected stages are successively enabled. (a) Output voltage of the multi-stage charge pump. (b–d) Level shifting voltage V_{SSH} supply and output voltage of the HV-FLS driving the fourth/third/second charge pump stage, respectively.

do not change, thanks to the charge-refreshing topology, the HV-FLS successfully maintain their outputs $ST_{2-4,HV}$ at the correct level.

3.3. State-of-the-Art comparison

Table 2 summarizes the performance of the proposed level shifter and compares it with other charge-refreshing FLS solutions, both in LV and HV CMOS processes, in the literature. The presented HV-FLS is, to the best knowledge of the authors, the only solution demonstrating HV operation in a LV process, intrinsic generation of the HV high supply rail, tracking of variations in the shifting level, and handling of non-periodical digital input signals, *IN*. All the metrics shown for the proposed solution are obtained experimentally, excepting the propagation delay which has been estimated from post-layout simulations.

4. Conclusions

In this paper, we have presented a HV floating level shifter with periodic charge refreshing. The circuit has five distinctive features: (1) it shifts by V_{SSH}, time-varying digital signals *IN* comprised between ground and V_{DD} rails, (2) it intrinsically sets the high supply rail of the output signal to $V_{DD} + V_{SSH}$, (3) it tracks variations of the shifting voltage, V_{SSH}, (4) it can handle static values for signal *IN*, and (5) it allows HV operation with LV CMOS processes.

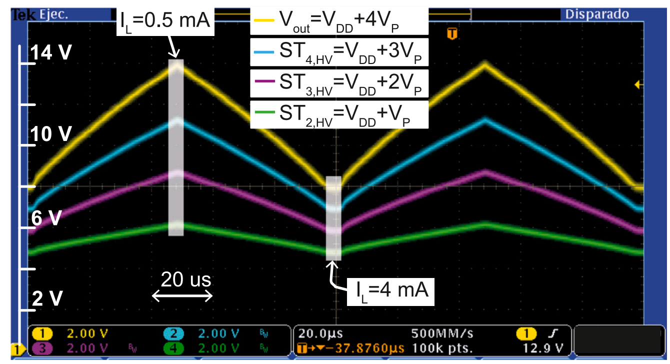

Fig. 10. Transient measurements of the multi-stage charge pump for V_{DD} =3 V and R_{CP} ≈210 Ω. The load current is a 10 kHz triangular wave from 0.5 mA to 4 mA. All stages are enabled.

It has been shown experimentally that V_{SSH} can reach up to 8.5 V, with an energy consumption of 2.9 pJ/op (V_{SSH} = 8.5 V and f_{clk} = 10 MHz). The propagation delay, estimated by post-layout simulations, is 1.81 ns. Even though the operation voltage can almost quadruplicate the nominal voltage of the technology, long-term degradation is mitigated by keeping all voltages across MOS devices' terminals below a safe limit. This is done by guaranteeing that PN junctions do not exceed the breakdown voltage, and by limiting the voltage across MIM capacitors.

As a functional demonstration of the circuit operation, the proposed HV FLS has been used as a building block for the voltage conversion ratio controller of a programmable multi-stage charge pump circuit.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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