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RESEARCH ARTICLE

A 12-Bit Low-Input Capacitance SAR ADC With a Rail-to-Rail Comparator

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ABSTRACT The input capacitance of the SAR ADC is considered a drawback in many applications. In this paper, a 12-bit low-power SAR ADC with low-input capacitance is proposed. The ADC is based on a separated DAC and sample-and-hold blocks (SB) structure. The SB structure suffers from variation in the input common-mode voltage of the comparator, leading to nonlinear input-referred offset and kickback noise. Here, a closed-loop low-power rail-to-rail offset cancellation technique for the comparator, based on body voltage tuning, is proposed. In order to stabilize the closed loop structure, the open loop gain is controlled by adapting the gain of the preamplifier. Using this structure, the rail-to-rail offset is kept lower than 110 μV and the overall power of the comparator is 1 pJ/Conv. Complementary-clocked dynamic branches are exploited at the input of the comparator to decrease the common-mode dependent kickback noise error to less than 1 LSB. The bootstrapped switch's controlling signal is also modified to achieve less than 1 LSB error and 18.9% lower power consumption. The proposed ADC is designed in standard 180 nm CMOS technology with a 1.8 V supply voltage and the input capacitance is reduced to 2 pF, which leads to power consumption of 41 nW in the input voltage supply. Electrical simulations including PVT, Monte-Carlo, and post-layout parasitic extraction were conducted to ensure the effectiveness of the approach. The ADC features an ENOB of 11.1-bit and a sampling rate of 1 MHz with a power consumption of 117.9 μW including the input power supply which are competitive with the state-of-the-art, and demonstrate the virtue of the proposed approach.

INDEX TERMS Successive approximation register (SAR), time-domain offset cancellation, kickback noise reduction, rail-to-rail, bootstrap switch.

I. INTRODUCTION

The Internet of Things (IoT) has provided tremendous opportunities. From point-of-care portable diagnosis devices [1] and smart agriculture realization [2] to safety improvement of transportation systems [3], and buildings [4]. IoT involves the interconnection of billions of sensor nodes, also known as edges. One or multiple environmental parameters can be detected in the edge [5]. The signal may then be transmitted to the data center for further calculations. Due to the wireless design, the nodes mostly operate with low-power constraints. Due to the dominance of digital processing, the Analog-to-Digital-Converter (ADC) is one of the key building blocks of IoT nodes. The specifications of these ADCs may be different but consuming the least amount of power, resolution of 10-12 bit, and sampling rate of more than 100 kHz are common constraints [6], [7], [8]. In this range of applications, SAR ADC is more efficient than other ADC topologies. A SAR ADC typically consists of Sample-and-Hold (S&H), Comparator (CMP), Digital-to-Analog-Converter (DAC), and digital circuits including a Successive Approximation Register (SAR), sub-blocks as shown in Fig. 1.

Fig. 1 (a), illustrates the block diagram of a conventional charge redistribution SAR ADC (CR-SAR) [9]. The capacitive DAC has an important role in the structure

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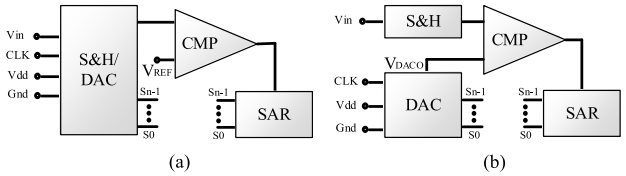

FIGURE 1. SAR structures, a) The Conventional CR-SAR [9], b) The SAR architecture with separate DAC and S&H blocks [10], [11], [12].

of SAR ADC. The overall capacitance of an n-bit DAC (C_T) is in the order of $2^n \times C_u$, where C_u is the unit capacitance. The value of C_u is determined by the maximum acceptable mismatch or kT/C noise criterion. In the CR-SAR, the DAC is used as the sampling capacitance too. Therefore, one of the major drawbacks of the CR-SAR architecture for high resolutions is its relatively large input capacitance [10], [11], [12], [13], [14], [15]. Increasing the input capacitance may decrease the input signal bandwidth [11], [13]. The large input capacitance may also increase the power drawn from the input voltage source.

The power consumed by the input power source is usually not considered in Walden-Figure-of-Merit, FOM_W [14]. It is important to notice that the input voltage source is mostly the sensor readout circuit with limited output resistance [16]. Therefore, an active voltage buffer can be used to increase the bandwidth of SAR ADC [13], [14], [15]. Since the buffer stage drives a large capacitive load, its static power consumption is relatively high [14]. Due to the rail-to-rail characteristics of the input signal [15], this buffer is usually designed with power-hungry rail-to-rail operational amplifiers [17]. This is considered a drawback when designing the overall IoT device, usually with very limited battery life.

To overcome the large DAC capacitance, some layout techniques are proposed to build small unit capacitances with higher matching profiles [18]. However, these techniques require precise post-layout verifications before designing the main SAR ADC to specify the model behavior. Moreover, the low DAC capacitance may also degrade the linearity due to capacitor matching [19]. Some modified switching techniques are also proposed to decrease the total capacitance of the SAR. These techniques can reduce the total input capacitance by a factor of 2-to-4 in exchange for multiple reference voltages [20]. However, adding accurate reference voltage sources increases the complexity and overall power consumption of IoT nodes. Also, the resulting input capacitance may still be large in high-resolution applications.

Another method is to separate the DAC and the sampling blocks in single-ended SAR. This structure, also known as the separated block SAR (SB-SAR), is illustrated in Fig. 1(b) [10], [11], [12]. Here, the input capacitance of the SAR ADC is independent of capacitor mismatch and is restricted only by kT/C noise criterion. Since in higher resolution SAR ADCs, the effect of the mismatch is more dominant in determining the size of the capacitors than kT/C, SB-SAR can be designed with smaller input capacitances. Additionally, SB-SAR can eliminate the need for additional reference voltage if properly designed. However, due to the nonlinear input-referred offset and kickback noise of the comparator, achieving resolutions higher than 8 bit can be challenging in this structure.

In this paper, a low-power 12-bit SAR with low input capacitance and high linearity based on SB-SAR is proposed [21]. The ADC exploits the proposed full-range comparator with the ability of rail-to-rail offset cancellation and kickback noise reduction. In addition, a modified bootstrapped switch is proposed to increase the linearity. The low-input capacitance SAR eliminates the need for power-hungry input buffers and is suitable for low-power wireless IoT nodes where the system-level power consumption is limited.

The paper is organized as follows: Section II studies the effects of comparator offset on SAR ADC structures. Section III provides detailed descriptions of the proposed SAR ADC subblocks and their circuit implementations. The overall SAR ADC structure and the control signals are presented in Section IV. Section V includes the simulation results confirming the ideas, and the paper is concluded in Section VI.

II. EFFECT OF COMPARATOR OFFSET ON SAR ADC

The dynamic comparator offset can be expressed as [22]

$$V_{os} = \Delta V_{th1,2} + \frac{V_{gs} - V_{th}}{2}\left(\frac{\Delta S_{1,2}}{S} + \frac{\Delta R}{R}\right) \qquad (1)$$

where $\Delta V_{th1,2}$ is the difference between the threshold voltages of input devices, V_{gs} is their gate-source voltage, $\Delta S_{1,2}$ is the difference in dimension and ΔR is the difference in the drain load of these devices. In (1), the first and the second terms represent the static and the dynamic offsets respectively. The main difference between the two offset types is that the static one refers to the offset produced by the physical parameters of devices. While the dynamic offset refers to the parameters which can vary with the input common-mode voltage of the comparator (V_{icm}). This type of offset is generated because of a mismatch between the parasitic capacitances of MOS devices [23] or the dimensions of these devices. Since parasitic capacitances vary with V_{icm} [22], any mismatch between them may cause input common-mode dependent offset.

The static offset of the comparator may only cause a linear error in the output of the SAR ADC. As a result, the linearity of the SAR ADC is not affected. Dynamic offset, on the other hand, has a more severe impact on the linearity of the SAR ADC [24]. Therefore, it is beneficial to study V_{icm} in different SAR architectures. The variation range of the DAC output voltage (V_{DACO}) with the conversion cycles (n) for a CR-SAR can be calculated as

$$\frac{2^n - 1}{2^n} V_{ref} < V_{DACO}(n) < \frac{2^n + 1}{2^n} V_{ref}. \qquad (2)$$

Equation (2) illustrates that in a CR-SAR when the number of conversion cycles increases, the final value of V_{DACO} leans toward V_{ref}. Therefore, V_{icm} approaches V_{ref} regardless of the input analog voltage (V_{in}). Since the input-referred offset is negligible at high input differential voltages, as long as the offset is considered, V_{icm} in CR-SAR is fixed at V_{ref}. Therefore, only static offset affects its performance. In SB-SAR, V_{DACO} can be calculated as

$$0 < |V_{DACO}(n) - V_{in}| < \frac{1}{2^{n-1}} V_{ref}. \tag{3}$$

Equation (3) demonstrates that, in SB-SAR ADC, while the conversion cycle (n) rises, V_{DACO} and hence V_{icm} lean toward V_{in} (since $V_{ref}/2^{n-1}$ leans toward zero) causing V_{icm} to vary with time. As a result, the SB-SAR ADC suffers from the dynamic input-referred offset of the comparator block. This problem can be mitigated by using the differential SAR, however, they also suffer from the large input capacitance.

Due to the importance of offset in comparators, a number of offset cancellation (OC) structures have been proposed [25], [26], [27], [28]. One of the common methods is known as auto zeroing, which uses switch capacitors and op-amps in the feedback structure to eliminate the effect of offset. In this method (because the offset cancellation cycle is repeated in every single clock cycle) the dynamic offset along with static offset can be eliminated. However, the power consumption increases due to the static current of op-amps [25].

In contrast with the op-amp based OC techniques, time-domain OC methods can remove the input-referred offset in several consecutive clock cycles. These methods mostly track the change in the outputs while changing a circuit parameter such as capacitive load or body voltage of the input devices to compensate for the offset. Owing to the use of all dynamic blocks, these methods consume less power [26], [27], [28].

In [27], a body-tuned time-domain OC technique is introduced which uses a feedback loop to compensate for the offset voltage. In this design, in addition to the main comparator, the feedback loop is designed with dynamic circuits. However, because the input devices of the comparator turn off at high common-mode voltages, neither the comparator nor the OC feedback loop works properly when the input common-mode voltage varies. In [28], the body-tuned structure is modified to add the rail-to-rail ability to the main comparator. In this structure, two dynamic level shifters are used at the input of the comparator to turn it on at high input voltages. A capacitor bank is also used to control the open-loop gain of the feedback so that closed-loop stability is assured. However, in this method, the residual offset of the comparator is higher than 1 LSB in a 12-bit SAR.

III. PROPOSED SAR SUBBLOCKS

A. COMPARATOR ARCHITECTURE

In this study, a rail-to-rail offset cancellation technique is proposed to satisfy the needs of the 12-bit SB-SAR ADC. The proposed structure improves the offset cancellation structure of [28], shown in Fig. 2, to provide more than one order of magnitude reduction in the input referred offset. The comparator works in two phases of offset cancellation (OC) and Comparison ($\overline{OC}$) which are selected by the enable signal (En). In the $\overline{OC}$ phase, OC blocks are turned off and the circuit works as a dynamic comparator. In the OC phase, the input pair drives three consecutive blocks of a time-domain amplifier (Amp), a phase detector (PD), and a charge pump (CP). These blocks are used for adjusting the body voltage of the input devices in a negative feedback loop to compensate for the input-referred offset. The Dynamic Level Shifter (DLS) blocks are used to keep the Complementary Input Core (CIC) "on" when V_{icm} is near rail voltages and the Main Input Core (MIC) is off.

First, the main drawback of [28] is discussed here by calculating the open-loop gain of OC phase and showing that in low V_{icm} it fails to efficiently reduce the input-referred offset. Then a new idea is proposed to overcome this drawback. The overall open-loop gain, G_T, of the OC phase is essential to assure the stability of the closed-loop scheme. G_T in Fig. 2 consists of three parts including the output delay of V_f^+ and V_f^-, Δt, to the input-referred offset, V_{os}, ($G_1 = \Delta t/V_{os}$), difference of input devices body voltages, ΔV_b, to Δt ($G_2 = \Delta V_b/\Delta t$) and threshold voltage variation to ΔV_b ($G_3 = \Delta V_{th}/\Delta V_b$). Therefore, the overall gain can be written as $G_T = G_1 G_2 G_3$. The first term of gain can be expressed as [28]

$$G_1 = \left(\frac{(V_{dd}).(C_{S1,2})}{I_{cm}^2}\right) \times g_m \tag{4}$$

where, $C_{s1,2}$ is the input capacitance of the second stage of the comparator, $g_m = I_{DM}/V_{os}$ is the transconductance of the preamplifier, and $I_{cm} = (I_{cs1} + I_{cs2})/2$ is the common-mode current passing through $C_{s1,2}$ due to V_{icm}. Substituting $g_m = \sqrt{2I_{cm}\beta}$ in the above equation results in

$$G_1 = \frac{\sqrt{2\beta}(V_{dd})(C_{S1,2})}{(I_{cm})^{3/2}}. \tag{5}$$

And for $I_{\rm cm}$ it can be written

$$I_{cm} = \begin{cases} I_{CIC,cm} : V_{dd} - |V_{thp}| < V_{icm} \\ I_{MIC,cm} + I_{CIC,cm} : V_{thn} < V_{icm} < V_{dd} - |V_{thp}| \\ I_{MIC,cm} + I_{P0_{cm}} : V_{icm} < V_{thn}, \end{cases} \tag{6}$$

where $I_{CIC,cm} = (I_{p3} + I_{p4})/2$, $I_{MIC,cm} = (I_{p1} + I_{p2})/2$, and $I_{p0,\rm cm}$ is the common-mode current passing through M_{p3} and M_{p4} when the DLSs are turned off. Assuming the I-V square law can be applied, for I_{p0} it can be written

$$I_{p0} = \frac{\mu_p C_{ox}}{2}(W/L)_{3,4}(V_{dd} - |V_{thp}| - V_{thn})^2, \tag{7}$$

where μ_p is the mobility of holes, C_{ox} is the gate-source capacitance and $W_{3,4}$ and $L_{3,4}$ are the width and the length of $M_{p3,4}$, respectively. As can be seen, I_{p0} is a constant current with a relatively large value, which is equally added to both sides of the comparator when the input V_{icm} is lower than

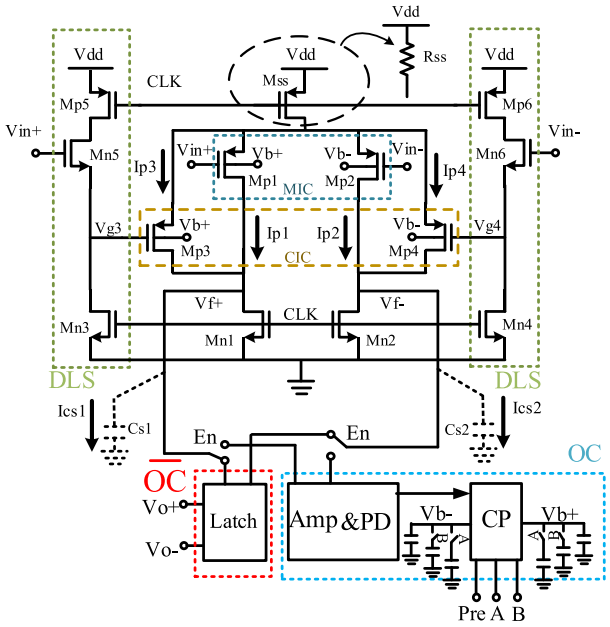

FIGURE 2. Block diagram of the full range offset cancellation proposed in [28].

$V_{th1,2}$. Substituting (6) and (7) in (4), G_1 can be expressed as

$$G_1 = \begin{cases} \lambda\left(\dfrac{\sqrt{\beta_{3,4}}}{(I_{CIC,cm})^{3/2}}\right) : V_{icm} > V_{dd} - \left|V_{thp}\right| \\ \lambda\left(\dfrac{\sqrt{\beta_{1,2}}}{(I_{MIC,cm})^{3/2}} + \dfrac{\sqrt{\beta_{3,4}}}{(I_{CIC,cm})^{3/2}}\right) \\ \qquad : V_{thn} < V_{icm} < V_{dd} - \left|V_{thp}\right| \\ \lambda\left(\dfrac{\sqrt{\beta_{1,2}}}{(I_{MIC,cm})^{3/2}} + \dfrac{\sqrt{\beta_{3,4}}}{(I_{P0,cm})^{3/2}}\right) : V_{icm} < V_{thn}, \end{cases} \tag{8}$$

where $\lambda = \sqrt{2}(V_{dd}).(C_{s1,2})$. Equation (8) shows that, G_1 is highly dependent on I_{cm} and hence on V_{icm}. As illustrated in Fig. 2, in [28], the gain of CP, G_2, is varied by A and B control signals in a reverse direction so that G_T is kept in an acceptable range. However, if due to a low amount of V_{icm}, I_{cm} increases, G_1 significantly decreases. This results in the reduction of the output of G_1, Δt. This is worsened due to excess current I_{p0}. Δt is exploited by the PD to produce proportional pulses which are used by CP to discharge the body voltages. Extremely low Δt cause the output of PD to be too small to turn CP on. Here, increasing the gain of CP does not compensate for the drop in G_1 and as a result, the offset cancellation for low V_{icm} may be disrupted. Here, a scheme is proposed to control the overall loop gain, G_T, by directly controlling G_1.

B. PROPOSED RAIL-TO-RAIL OFFSET-CANCELATION CIRCUIT

Fig. 3 illustrates the proposed rail-to-rail offset-cancelation circuit. As seen in Fig. 3(a), two Main Gain Control (MGC) and Complementary Gain Control (CGC) blocks are exploited to eliminate I_{p0} and its destructive effect on G_1. To accomplish that, CGC cuts the current of CIC when $V_{icm} < V_{dd}/2$. Therefore, I_{cm} can be written as

$$I_{cm} = \begin{cases} I_{CIC,cm} : V_{dd} - \left|V_{thp}\right| < V_{icm} \\ I_{MIC,cm} + I_{CIC,cm} : V_{dd}/2 < V_{icm} < V_{dd} - \left|V_{thp}\right| \\ I_{MIC,cm} : V_{icm} < V_{dd}/2. \end{cases} \tag{9}$$

In addition, the proposed scheme controls the gain of the preamplifier instead of controlling the gain of CP and hence, the need for the capacitor bank in the CP block is eliminated. To study the proposed scheme, the variation of G_1 with input common-mode voltage is first studied. For the sake of simplicity, first the effect of MIC, i.e., M_{p1} and M_{p2}, on G_1 is considered and denoted by $G_{1,MIC}$. Finally, the results are extended to include CIC too. The variation of $G_{1,MIC}$ with V_{icm} can be expressed as

$$\frac{\partial G_{1,MIC}}{\partial V_{icm}} = \frac{\partial G_{1,MIC}}{\partial I_{MIC,cm}} \times \frac{\partial I_{MIC,cm}}{\partial V_{icm}}. \tag{10}$$

Here, for all the common-mode voltage range M_{ss} is in the triode region (since its drain is always greater than $V_{dd} - V_{th}$), and M_{ss} can be modeled with R_{ss}. The input devices are turned on in the saturation region, regardless of the common-mode voltage. For the common-mode current, it can be written

$$I_{MIC,cm} = \beta_{1,2}\left(V_{dd} - 2I_{MIC,cm}R_{ss} - V_{icm} - \left|V_{thp}\right|\right)^2, \tag{11}$$

And therefore,

$$I_{MIC,cm} = \frac{\left(1 + 4R_{ss}\beta_{1,2}\gamma_1 \pm \sqrt{1 + 8R_{ss}\beta_{1,2}\gamma_1}\right)}{8R_{ss}^2\beta_{1,2}}, \tag{12}$$

where $\gamma_1 \triangleq V_{dd} - V_{icm} - \left|V_{thp}\right|$. Assuming $1 + 4R_{ss}\beta_{1,2}\gamma_1 \gg \sqrt{1 + 8R_{ss}\beta_{1,2}\gamma_1}$, variation of $G_{1,MIC}$ with V_{icm} can approximately be written as

$$\frac{\partial G_{1,MIC}}{\partial V_{icm}} \approx \frac{-3/2\sqrt{2\beta_{1,2}}\,(V_{dd})\,.\,(C_{s1,2})}{\left(I_{MIC,cm}\right)^{5/2}} \times \left(\frac{-1}{2R_{ss}}\right), \tag{13}$$

which leads to

$$\frac{\partial G_{1,MIC}}{\partial V_{icm}} \approx \frac{\lambda_1\,(2R_{ss})^{3/2}}{\left(V_{dd} - V_{icm} - \left|V_{thp}\right|\right)^{5/2}}, \tag{14}$$

where $\lambda_1 = 3/2\sqrt{2\beta_{1,2}}(V_{dd}).(C_{s1,2})$. From (14), it can be concluded that in order to control the variation of $G_{1,MIC}$ with V_{icm}, R_{ss} can be set. According to (14) as V_{icm} increases, the denominator decreases, and the value of R_{ss} should be decreased to keep $\partial G_{MIC}/\partial V_{icm}$ constant. The reduction in the value of R_{ss} is implemented by paralleling the tail devices with various dimensions. Similarly, if $\lambda_2 = 3/2\sqrt{2\beta_{3,4}}(V_{dd}).(C_{s1,2})$, the variation of $G_{1,CIC}$ with V_{icm}

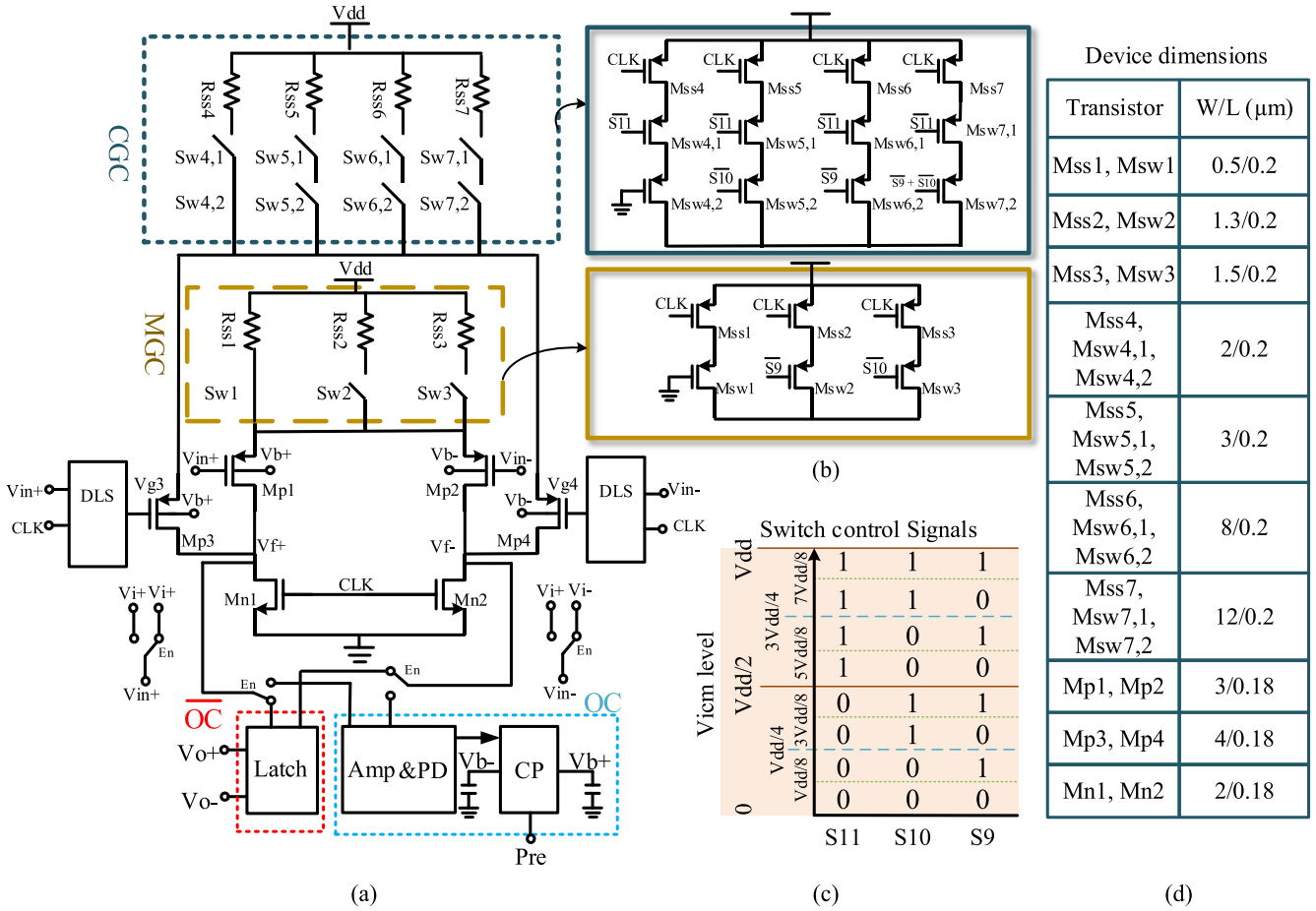

FIGURE 3. a) The proposed structure for controlling the open-loop gain using Main Gain Control (MGC) and Complimentary Gain Control (CGC) circuits in the preamplifier, b) The implementation of the switches and tail resistors, c) controlling signals with input common mode voltage level, d) the dimensions of the MOSFETs.

can be calculated as

$$\frac{\partial G_1}{\partial V_{icm}} = \begin{cases} \dfrac{\lambda_2 (2R_{ss,CGC})^{3/2}}{\left(V_{dd} - V_{icm} - |V_{thp}| + V_{thn}\right)^{5/2}} \\ \qquad : V_{dd} - |V_{thp}| < V_{icm} \\ \dfrac{\lambda_1 (2R_{ss,MGC})^{3/2}}{\left(V_{dd} - V_{icm} - |V_{thp}|\right)^{5/2}} \\ + \dfrac{\lambda_2 (2R_{ss,CGC})^{3/2}}{\left(V_{dd} - V_{icm} - |V_{thp}| + V_{thn}\right)^{5/2}} \\ \qquad : V_{dd}/2 < V_{icm} < V_{dd} - |V_{thp}| \\ \dfrac{\lambda_1 (2R_{ss,MGC})^{3/2}}{\left(V_{dd} - V_{icm} - |V_{thp}|\right)^{5/2}} : V_{icm} < V_{dd}/2. \end{cases} \tag{15}$$

According to (15), in order to keep $\partial G_1/\partial V_{icm}$ low, R_{ss} can be controlled. Here, two sets of four resistances are used as MGC and CGC circuits to implement R_{ss}. V_{icm} is divided into eight equal regions and for each region a specific R_{ss} from R_{ssm1-4}, R_{ssc5-8} is selected. Fig. 3(b) illustrates the implementation of the R_{ss} and switches. As shown, the R_{ss} is the equivalent resistance of the MOSFET switches (M_{swn}) and the tail transistors (M_{ssn}) in triode regime. Here, Msw1, and Msw4,2 are used as always on switches to maintain the symmetry in the layout design.

In the deep triode,R_{ss} can be written as $R_{ss} = 1/(\mu_p C_{ox}(V_{dd} - V_{th})(w/L)_{ss})$ which implies that $R_{ss} \propto 1/(w/L)_{ss}$. Therefore, to change R_{ss}, the aspect ratio (w/L) of representative MOSFETs can be set. S11, S10, and S9 are used as control signals in MGC and CGC which are set based on eight levels of V_{icm}. The value of these signals in relation with V_{icm} are shown in Fig. 3(c). Note that since the switches are implemented with PMOS, the inverted form of the signals is used. The OR logic is used to turn the $M_{sw7,2}$ branch on. This way at the highest input levels an additional parallel branch will be included. This is important to control the R_{ss} at high V_{icm} ranges. Fig. 3(d) shows the dimensions of the MOS devices used in the comparator design.

In order to implement this technique, R_{ss} needs to decrease as V_{icm} increases, i.e., when $V_{icm} \approx V_{dd}$ the overall R_{ss} should be chosen as a minimum. R_{ss} can be decreased by increasing $(W/L)_{1,2}$. However, increasing $(W/L)_{1,2}$ may

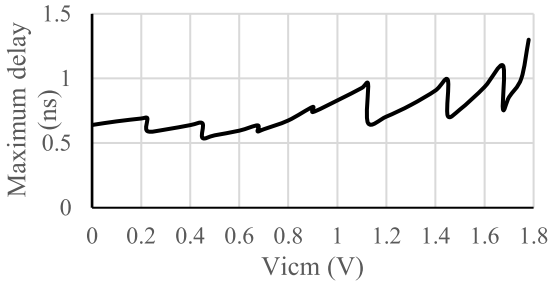

FIGURE 4. Maximum delay of the comparator with the incrementation in input common-mode voltage.

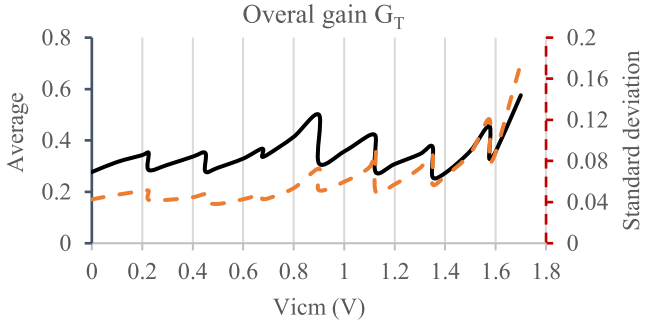

FIGURE 5. The average and standard deviation of the Monte-Carlo simulation results for the overall open-loop gain G_T for 10 samples.

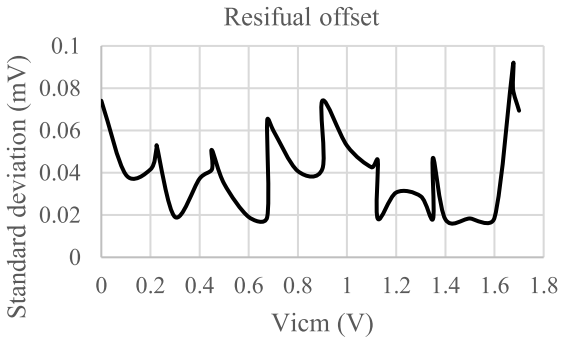

FIGURE 6. The standard deviation of the Monte-Carlo simulation results for the rail-to-rail residual input-referred offset for 50 samples.

increase the share of the subthreshold currents of M_{p1} and M_{p2} from I_{cm} when V_{icm} is high. This can decrease the slope of $V_f^{+,-}$ when M_{p1} and M_{p2} are turned off and result in unnecessary additional variation of G_1 causing a tradeoff that should be dealt with during the design procedure.

Using the proposed design, the comparator is able to properly work when the input common-mode voltage changes from rail-to-rail. Fig. 4 shows the maximum delay of the comparator when a 1 mV differential signal is applied. As can be seen, the maximum delay is well below the frequency of operation of SAR.

The proposed technique effectively limits the variation of G_1 and hence G_T. Fig. 5 shows the average and the standard deviation of Monte-Carlo analysis for 10 samples. In this figure the variation of G_T when V_{icm} varies from rail to rail is shown. Note that, as mentioned earlier, G_T is defined as $\Delta V_{th}/V_{os}$ therefore, the vertical axis in Fig. 5 does not have

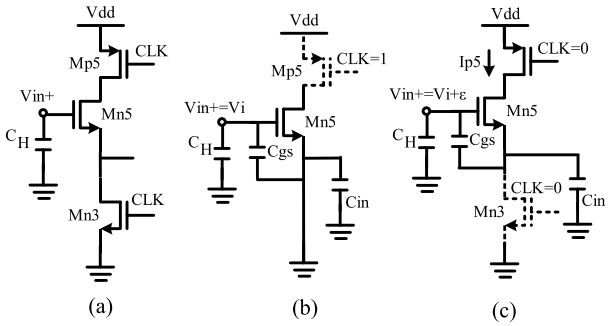

FIGURE 7. a) DLS block connected to the hold capacitance, C_H, b) when CLK = 1, c) when CLK = 0.

TABLE 1. Comparison of the proposed comparator.

Comparator parameters	Proposed		[26]	[27]	[28]
Technology (nm)	180		180	500	180
Power supply (V)	1.8		1.8	5	1.8
Power (pJ/Conv) @ V_{id}=1mV, V_{icm}=0.8	0.98	1.03*	0.094**	23***	0.99
Maximum residual offset (mV)	0.08	0.11*	0.628	0.05	3.80
Input common-mode range OC (%)	100		55	40	100

* Post-layout simulation results
**Does not include OC phase
***Experimental results reported

any unit. Fig. 6 shows the standard deviation of the residual offset of the proposed comparator when V_{icm} varies from rail-to-rail. Fig. 6 is achieved using Monte-Carlo simulation for fifty samples for each 0.1 V step input common-mode voltage increment. As shown, the variation of the input-referred offset is kept under 0.09mV in the worst case which is more than one order of magnitude lower than the offset in [28]. This is sufficiently less than 1 LSB in a 12-bit SAR ADC. The relatively higher offset around 0.9 V corresponds to the higher G_T at this voltage shown in Fig. 5. Table 1 compares the post-layout results of the proposed comparator parameters with similar structures. After post-layout analysis the residual offset in the worst case is kept under 0.114 mV.

C. PROPOSED KICKBACK NOISE REDUCTION (KBNR) TECHNIQUE

The SB-SAR structure suffers from asymmetrical Kickback Noise (KBN). In the SB-SAR, the comparator inputs are fed by unequal input capacitances, i.e., sample-and-hold capacitance (C_H) and the total capacitance of DAC (C_T). Since C_T is several times larger than C_H, the SB-SAR is susceptible to the destructive effects of asymmetric KBN [29]. DLS block connected to the hold capacitance, C_H, is shown in Fig. 7(a). In the sampling phase, the input voltage is sampled on C_H and $V_i^+ = V_i$. The value of V_i^+ in the hold phase affects the decision making in the comparator. In the hold phase, when CLK signal is high, as illustrated in Fig. 7(b), the source of M_{n5} is connected to ground through

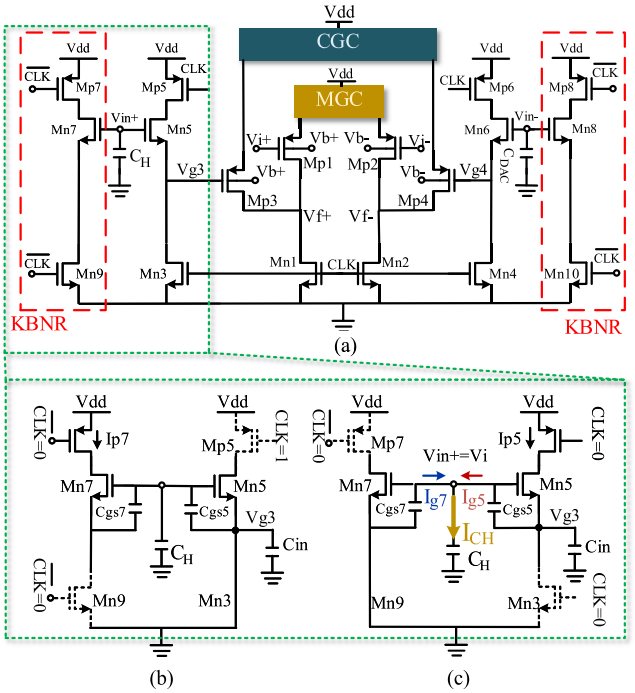

FIGURE 8. a) The proposed preamplifier with the Kickback Noise Reduction (KBNR) circuit. b) When CLK = 1, c) When CLK = 0.

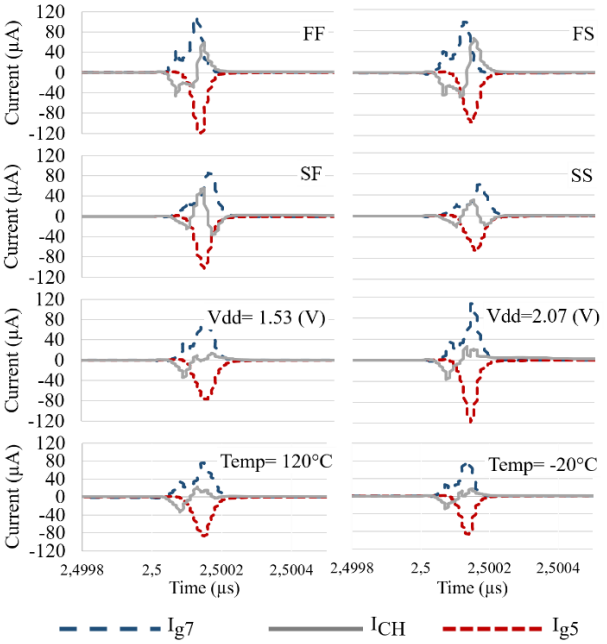

FIGURE 9. Effect of PVT variations on currents flowing through the gate of the input transistors and S&H capacitor.

M_{n3}, and the input voltage is applied to the summation of C_H and C_{gs5}. When clock signal falls, as illustrated in Fig. 7(c), M_{n3} turns off and C_{gs5} is disconnected from ground. Here, M_{p5} turns on in the saturation and starts charging the input capacitance of the next stage (C_{in}) until the gate-source voltage of M_{n5} reaches V_{th}. At this point, M_{n5} turns off and the path to C_{in} is cut. The change in the voltage of C_{in} partially discharges C_{gs5} into C_H, changing its voltage to $V_i + \varepsilon$. For the excess voltage ε it can be written

$$\varepsilon = \frac{C_{gs5}\,(V_i - V_{th})}{C_H}. \tag{16}$$

As can be seen, ε is proportional to the gate-source capacitance of M_{n5} and V_i both of which add to the nonlinear distribution of KBN.

Fig. 8(a) shows the proposed KBN reduction (KBNR) circuit configuration. The proposed KBNR structure is dynamic and only adds dynamic power to the comparator. As discussed, C_{DAC} is significantly larger than C_H therefore the effect of KBN on V_i^- is negligible and only its effect on V_i^+ is studied here. As illustrated due to the input capacitance of M_{p3} (C_{in}), the structure is not symmetric. Besides, the behavior of the comparator at the falling edge of clock is important for proper decision-making. The proposed circuit operates as follows:

Similar to the structure of Fig. 7, the input voltage is sampled on C_H. The comparator starts comparing the input voltages when the sampling ends. In the hold phase when CLK signal is high, the comparator is in the reset cycle and M_{n3} and M_{p7} are on while M_{n9} and M_{p6} are off, Fig. 8(b). Here, the input sampled voltage is stored on the summation of C_H and C_{gs5}. Here, I_{p7} has charged C_{gs7} until M_{n7} turns off, and the voltage over the gate-source of M_{n7} equals V_{th}. In the comparison cycle of the comparator, the CLK signal is low, and therefore, M_{n3} and M_{p7} are off and M_{n9} and M_{p5} are on, Fig. 8(c). Similar to the circuit of Fig. 7 I_{p5} starts charging C_{in}, to $V_i - V_{th}$ generating I_{g5}. Here, on the other hand, the source of M_{n7} is connected to ground, and C_{gs7} is charged by I_{g7} until its voltage reaches V_i. The variation of V_i caused by charging C_{gs7} can be expressed as

$$\delta = -\frac{C_{gs7}(V_i - V_{th})}{C_H}. \tag{17}$$

As can be seen from (16) and (17), the positive additive voltage of ε can be compensated by δ if M_{n5} and M_{n7} are matched. Therefore, the charge of C_{gs5} is discharged into C_{gs7} leaving the sampled voltage intact.

A set of simulations were run to verify the performance of the proposed KBNR circuit. As explained, KBN effect is more important when the DLSs are on, i.e., when the input common voltage is high. Therefore, the simulations are run for high-input common-mode voltage ranges.

Fig. 9 illustrates the current flowing through the gate of the input devices at the falling edge of CLK signal for various technology process, voltage, and temperature (PVT) corners.

Here, a 180 nm standard CMOS process with a 1.8 V supply voltage is considered without loss of generality. In the simulation results, note that the positive current represents the outgoing current from the node. As expected, the excess gate current of M_{n5}, I_{g5}, is well compensated through the gate current of M_{n7}, I_{g7}, in all conditions resulting in a relatively flattened S&H current, I_{CH}. Fig. 10 illustrates the effect of KBN on V_i+, at the same falling edge of CLK. In this

TABLE 2. Comparison of the proposed and conventional BS switches.

Switch parameters	Proposed BS*	Conventional BS*
ENOB	12.65	11.21
Power (nW)	68.74	84.85
Sampling rate (MHz)	1	1
Maximum $V_o - V_i$ (mV)	0.402	0.780
Bootstrap Cap C_{bs} (pF)	2.5	2.5

*Simulated results at full-range input signal

figure,V_i+ is shown with and without the proposed KBN reduction technique for different PVT corners. As shown, the change in the sampled voltage V_i+ is effectively compensated by applying the proposed design in all the corners.

D. SAMPLE-AND-HOLD CIRCUIT, AND THE PROPOSED BOOTSTRAPPED SWITCH

The sample-and-hold circuit plays an essential role in the design of SAR ADC. The linearity of this block can affect the linearity of the overall converter. If the switch is implemented with a single MOSFET device, the variation in its gate-source voltage changes its conductivity. The conventional bootstrapped (BS) switches, as illustrated in Fig. 11(a), keep the V_{gs} of the switch device (M1) constant by using a BS-capacitor, C_{bs}, [30]. C_{bs} is charged to V_{dd} and then applies a constant voltage to V_{gs} of M1 when it turns on.

The conventional bootstrapped switch works well for ADCs with resolutions up to 10 bits [31]. For higher resolutions, some modifications are necessary [32]. One drawback is caused by the variable voltage changes of the gate port of M1 (BS) at the beginning of the hold cycles. As illustrated in Fig. 11(b), the voltage of the BS node varies from $V_i + V_{dd}$ in the sampling cycle to zero in the hold cycle, therefore, its variation is dependent on the input voltage.

This effect, also known as clock feedthrough effect, happens due to the parasitic capacitance of M1 and can be expressed as $\Delta V = WC_{ov}(V_i + V_{dd})/(WC_{ov} + C_H)$ [22], where C_{ov} and W are the overlap capacitance and width of M1 respectively. The additive error ΔV is dependent on the input signal and gets worse with small values of C_H. Here, an effective method is proposed to reduce the input-dependent error. The proposed bootstrapped switch is shown in Fig. 12(a).

Here, similar to the conventional circuit, the gate-source voltage of the switch transistor M1 (BS) in the sample cycle is equal to V_{dd}. However, in the hold cycle, BS is connected to V_i instead of ground.

With this technique, the gate voltage of M1 (BS) varies from $V_i + V_{dd}$ in the sampling mode to V_i in the hold mode. This way, when transitioning from sample to hold, the error voltage coupled to C_H through M1, can be depicted as $\Delta V = WC_{ov}V_{dd}/(WC_{ov} + C_H)$ which does not depend on the input voltage. BS node voltage and the gate-source voltage of the proposed switch, for a full-scale input signal, are shown in Fig. 12(b).

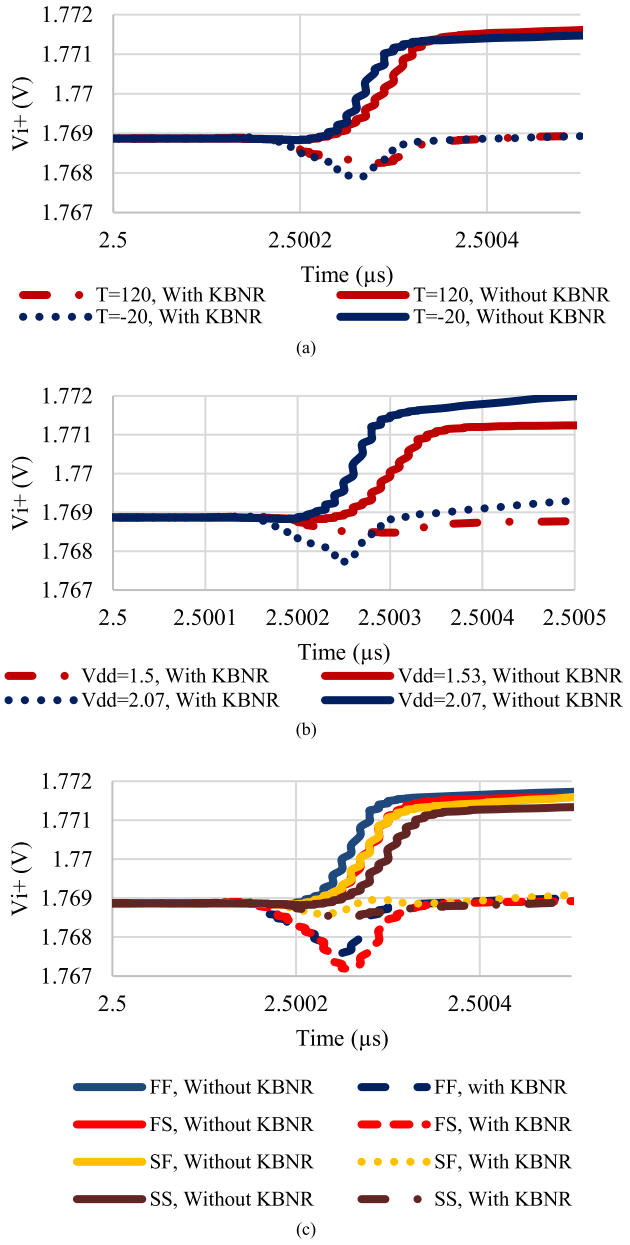

FIGURE 10. The sampled voltage with and without KBN reduction for different a) temperature, b) supply voltage, and c) process corners.

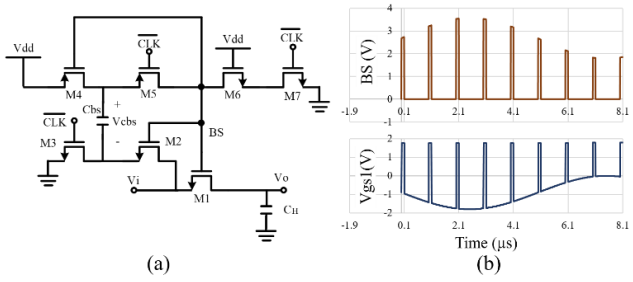

FIGURE 11. Conventional bootstrapped switch, a) schematic, and b) time-domain node voltages [30].

In the proposed bootstrapped switch, switch Sb1 is used to connect BS node to V_i in the hold cycle. Sb1 switch is

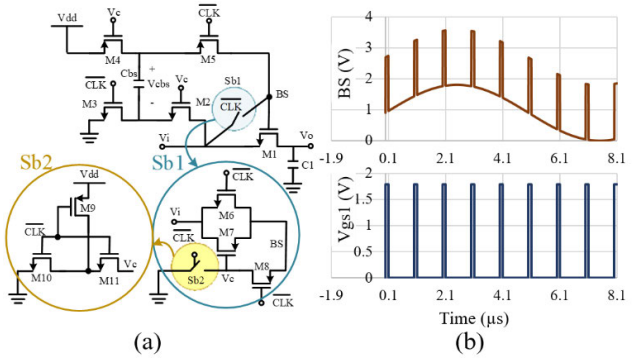

FIGURE 12. Proposed modified bootstrapped switch a) schematic, and b) time-domain node voltages.

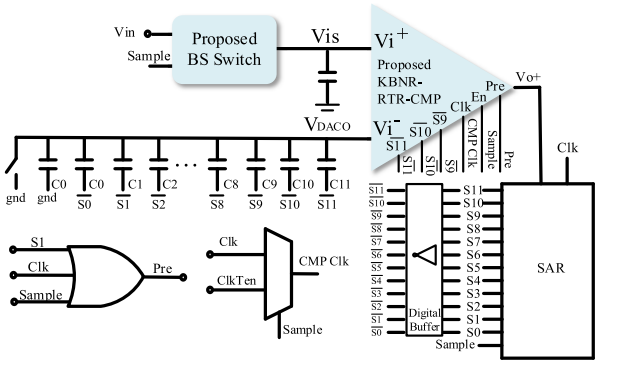

FIGURE 13. The overall BS-SAR ADC including the proposed rail-to-rail OC and KBNR in comparator and the proposed modified BS switch.

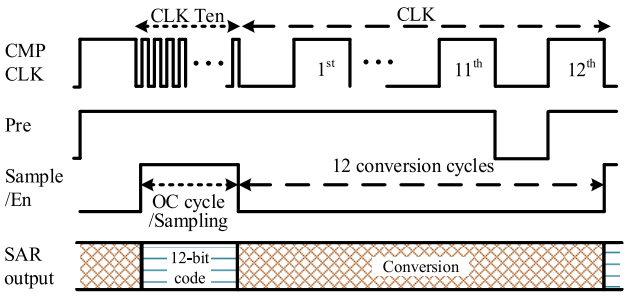

FIGURE 14. ADC control signals.

implemented with a transmission gate so that the parallel structure of NMOS and PMOS can pass low and high levels of the input voltages effectively. Sb1 must be closed during the hold cycle, therefore, $\overline{CLK}$ is connected to the gate of the NMOS assuming that the sampling is done in the positive cycle of CLK. However, because BS node voltage can be higher than V_{dd}, CLK signal cannot be used for turning the PMOS M7 off. A controlling circuit is used for controlling M7. This controlling circuit works as follows: During the hold cycle, when $V_{BS} = V_i$, M7 should be turned on by Sb2. The gate voltage of M7 (V_C) is connected to ground and it is turned on. During the sampling cycle, M7 needs to be off.

Here, Sb2 is turned off and M8 is turned on. Therefore, V_C is connected to the voltage of BS node to turn M7 off. During the hold cycle, $V_{BS} = V_i$ and hence, V_{BS} does not exceed V_{dd} and $\overline{CLK}$ can be used to turn M8 off.

Sb2 is designed to pass low voltages to V_C during the hold cycle, to turn M7 on and it can be realized with an NMOS. During the sampling cycle V_{BS} can get as high as $2V_{dd}$, and NMOS can be stressed by the high drain-source voltage. In order to avoid this, as shown in Fig. 12, Sb2 is implemented by a T-type switch [6] instead of a simple NMOS. During the sample cycle, the T-type switch connects the source of M11 to V_{dd}; therefore, drain-source voltage of neither M11 nor M10 exceeds V_{dd}. The control voltage of V_C is also used for turning M2 and M4 off for similar reasons. Table 2 compares the characteristics of the proposed and conventional bootstrap switches when the sampling frequency is 1 MHz and the input voltage frequency is 10 kHz. Using the proposed scheme decreases the error by 48% while reducing the overall power consumption by 18.9% which is due to the fact that in the proposed bootstrapped switch, BS node voltage variation is limited.

IV. ADC ARCHITECTURE AND CONTROLLING SIGNALS

Fig. 13 shows the implemented BS-SAR ADC structure, exploiting the proposed rail-to-rail OC and KBNR comparator and modified BS switch. The input capacitor is chosen as 2 pF which satisfies the kT/C noise criterion for 12-bit ADC.

Fig. 14 shows the overall ADC design including the control signals. As shown, the "Sample" signal is generated by the logic SAR and is used as the CLK signal in the proposed modified BS switch. The outputs of the logic SAR block are used to control the capacitive DAC. To drive the large capacitive load of DAC, a set of digital buffers is used at the output of the digital SAR. The comparator's offset is canceled at the beginning of each conversion cycle. When the input voltage is being sampled and the output digital word is available, the comparator is free and the offset cancellation phase starts. Therefore, the same "sample" signal is used as "En" in the comparator as well. Here, a multiplexer selects a clock signal ten times the main clock of SAR (ClkTen) for the operation of the comparator in the offset cancellation phase. The comparator architecture is fast enough to handle clock frequency of ClkTen signal [28]. Prior to each offset cancellation, the "Pre" signal resets to zero so that the CP block outputs are pulled up to V_{dd} and the comparator becomes ready for the next OC cycle. The "Pre" signal is generated at the last conversion cycle using "S1", "CLK", and "Sample" signals to make it synchronous with SAR cycles. In practice, mostly the input voltage frequency is sufficiently lower than the conversion rate of the ADC ($f_{in} < 10 f_{nyquist}$). Here, the three topmost valuable bits of SAR from the last conversion cycle are used as the controlling signals in the rail-to-rail comparator (S9, S10, and S11). This is due to the availability of these signals during the sampling phase. Three topmost valuable bits can represent the value of V_{icm} with three bits resolutions.

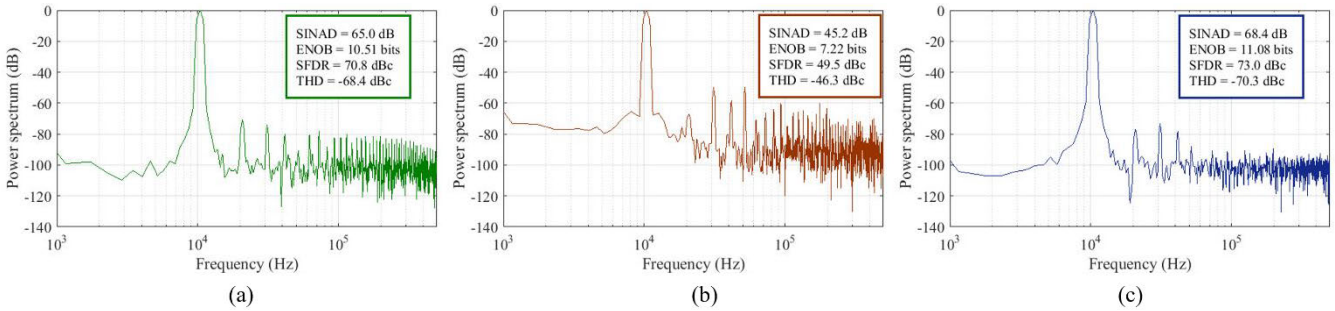

FIGURE 15. ADC Power Spectrum, a) perfectly matched input devices without KBN reduction, b) mismatched input devices with KBN reduction and OC disabled, c) mismatched input devices with KBN reduction and OC enabled.

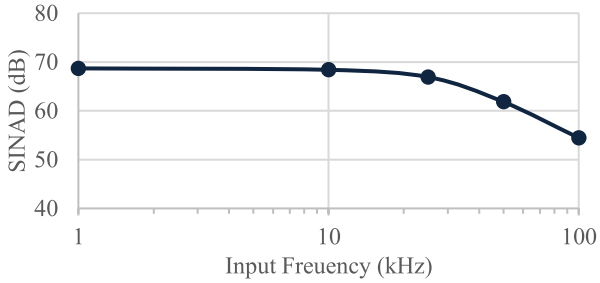

FIGURE 16. SINAD of the SAR ADC for different input frequencies.

these signals can estimate the commonmode voltage at the next conversion. Using the three topmost significant bits to estimate the level of V_{icm} can decrease the complexity of the controlling circuits by eliminating the need for common-mode detection circuits, and hence, can reduce the overall power consumption. In cases where the whole Nyquist band is needed, additional common mode detection circuits can be used to properly address the controlling ports at the beginning of the OC phase. In addition to the low input capacitance, due to the rail-to-rail structure of the comparator, the proposed SAR ADC eliminates the need for additional reference supply voltages. Here, instead of feeding the additional reference voltage to the DAC, V_{dd} is directly used as the reference voltage. This is highly appreciated since designing a PVT robust, noise-free reference voltage that can drive the rather large DAC capacitor can be challenging and adds to the overall power consumption and design complexity.

V. SIMULATION RESULTS

The proposed SAR ADC was simulated in a 0.18 μm standard CMOS technology with a 1.8 V supply voltage and the reduced input capacitance of 2 pF, which sufficiently satisfies the kT/C noise criterion. In order to calculate the dynamic parameters, the ADC is simulated with a 10.3 kHz input sine wave and a sampling rate of 1 MHz.

To verify the effect of each block on the dynamic characteristics of the overall ADC, three scenarios are considered and illustrated in Fig. 15. In the first scenario, Fig. 15(a), the comparator has perfectly matched input devices, however, it suffers from the kickback noise. Here the obtained SINAD and ENOB were 65 dB and 10.5-bits respectively.

In the second scenario, Fig. 15(b), the circuit with mismatched input devices is considered to study the effect of the dynamic offset on the ADC's performance. Here, the kickback noise reduction circuit is used but the rail-to-rail offset cancellation is disabled. The input devices suffered from a 17% mismatch applied to dimensions which was calculated based on the worst-case scenario obtained by the Monte-Carlo simulations. The results showed that the SINAD deteriorated to 45.2 dB and ENOB being as low as 7.2-bit. Finally, in the third scenario, Fig. 15(c), the SB-SAR exploiting the proposed offset cancellation and KBNR circuits are considered. Here, the input devices have the same amount of mismatch as in the second scenario. SINAD and ENOB of the designed scheme despite the presence of uneven mismatches and KBN were improved to 68.4 dB and 11.1-bits respectively. This improvement is achieved due to the rail-to-rail OC and KBNR structures. Fig. 16 shows the SINAD of the proposed SAR against input frequency. As expected SINAD and ENOB decrease as the input frequency increases due to using the last conversion results (s11, S10, and S9) to control the open-loop gain. If the full Nyquist band is required, an input common-mode detector circuit can be added to increase the bandwidth.

Fig. 17 shows the static parameters of the SAR. The DNL and INL of the proposed ADC when the OC is disabled are shown on the left while the results with OC enabled are shown on the right. As illustrated, the peak DNL for the case when the OC is disabled is $+1.0/-1.25$ LSB, and the peak INL is $+15.75/-12$ LSB. After enabling the OC in each conversion cycle the peak DNL and INL were improved to $+0.5/-0.5$ LSB and $+1.5/-1$ LSB respectively which show a remarkable improvement in terms of linearity achieved by circuits proposed in this paper. The proposed SB-SAR consumes a total power of 117.9 μW when clocked at 1 MHz. This power consumption also includes the input voltage source which conventionally is not reported neither in the power consumption of the SAR ADCs nor in the Walden-Figure-of-Merit (FOMW) [14]. The simple binary weighted DAC which is used to emphasize the effectiveness of the SB-SAR is responsible for a high proportion of power consumption which can easily be reduced to half using

TABLE 3. Comparison with similar state-of-the-art structures.

SAR parameter		This work	*ASSCC 09* [11]	*APCCS 12* [12]	*JSSC 10* [31]	*TCASI 16* [32]	*TCASII 16* [33]	*JSSC 18* [34]	*TCASI 19* [6]	*ISCAS 19* [35]	*TCASI 19* [36]	*TCASI 21* [37]
Topology		**SB-SAR**	SB-SAR	SB-SAR	Mono	H. Lin.	Co-fine	Redist.	UL-Vdd	Redist.	TI-SAR	PL-SAR
Technology (nm)		**180**	180	180	130	180	180	90	180	180	130	28
Supply voltage (V)		**1.8**	1	1.8	1.2	1.8	0.8	0.5	0.25	0.7	1.2	1.05
Input range (V)		**1.8 (100%)**	1 (100%)	NA	2 (DM) 83%	NA	NA	NA	0.25 (100%)	NA	NA	NA
Input Cap (pF)		**2**	1.28	1.2	2.5	15.8	NA	NA	1.6	2.5	0.48	3
Power (μW)	Including input power	**117.9**	6.15	10.3	NA	NA	NA	NA	NA	NA	NA	NA
	Without input power				826	820	0.2	0.81	0.001	0.73	105000	4260
Sampling rate (MS/s)		**1**	0.4	1	50	10	0.2	0.1	0.0005	0.1	3200	60
Resolution (Bit)		**12**	8	8	10	12	10	12	10	12	8	14
ENOB (Bit)		**11.1**	7.1	7.2	9.1	10.8	9.1	10.7	8.1	10.4	5.7	10.4
FOM_W (fJ/Conv-step)	Including input power	**54.4**	97	67	NA	NA	NA	NA	NA	NA	NA	NA
	Without input power				29	44.2	1.8	4.82	8.6	5.6	640	54.2
2^(ENOB)/C_{in} (Output levels/pF)		**1097**	107	122	219	113	NA	NA	171	540	108	450
No. of reference voltages		**No**	No	No	No	2	1	2	1	2	1	1
Area (mm^2)		**0.218**	0.062	0.205	0.052	0.359	0.105	0.109	0.024	0.083	1.1	0.368

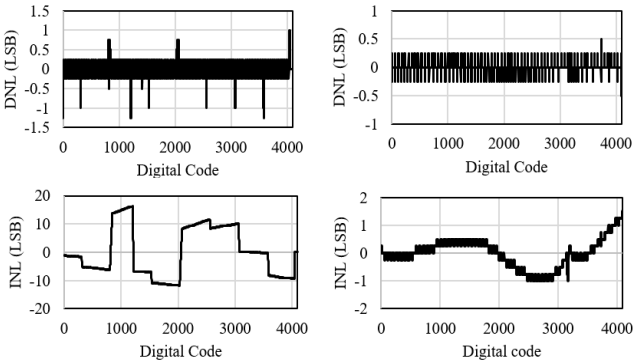

FIGURE 17. Static parameters of the proposed ADC with mismatched input devices when OC is disabled, left side, and when OC is enabled, right side.

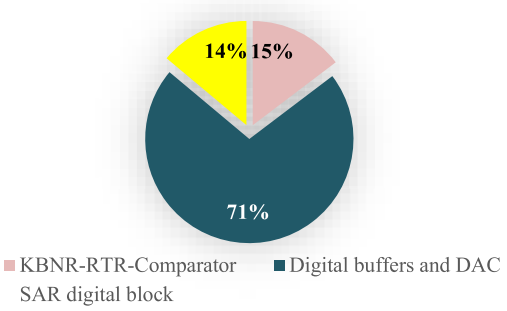

FIGURE 18. ADC power breakdown.

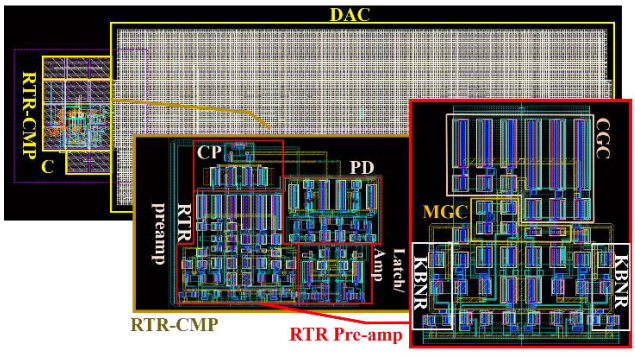

FIGURE 19. The layout of the proposed SAR.

available switching techniques. Since the structure benefits from the rail-to-rail comparator structure, the need for the reference voltage is eliminated. Here, the output of the digital block is used for addressing the capacitance DAC. A set of digital buffers is used to drive the DAC. The power consumption from the same 10 kHz input voltage supply is 41 nW which is obtained due to the small input capacitance of the SB-SAR. The power consumption share of each SAR sub-block is shown in Fig. 18.

As shown, the power consumption of the digital buffers used for driving the DAC capacitances (71%) accounts for a large share of total power consumption followed by the comparator (15%) and the digital blocks (14%). The layout of the proposed circuit is shown in Fig. 19. Post-layout simulations showed a 16% increase in the power consumption of the proposed circuit. The SINAD of the proposed SAR was 68.9 dB which lead to 11.2-bit ENOB. The slightly higher ENOB from the post-layout simulation is due to the perfectly matched structure of the input devices of the comparator. The parameters of the proposed SAR are summarized in Table 3. Table 3 includes a comparison between this work and similar

studies. As can be seen, in comparison with similar structures with low input capacitance, the proposed circuit achieves the highest ENOB. In the proposed structure, similar to [12] the power consumption and the FOM_W include the input power source. In order to emphasize this, the power consumption and FOMW rows in this table are divided into two sections with and without input power source power. The overall circuit occupies a die area of 260×840 $(\mu m)^2$. In aadition, since the input capacitance is conventionally related to the 2^(ENOB), in order to fairly compare these two parameters in the low-power SAR ADCs, the term $2^{(ENOB)}/C_{in}$ is added to Table 3 to illustrate the effectiveness of the proposed design. This coefficient represents the relation between the input capacitance in SAR and the effective number of bits.

VI. CONCLUSION

A 12-bit low input capacitance SAR ADC was presented in this paper. The ADC benefits from the long-existing SB-SAR architecture to reduce the input sampling capacitance to 2 pF. Conventional SB-SAR structure forces dynamic offset and uneven KBN to the ADC's output which deteriorate the ENOB and linearity parameters. However, the proposed structure exploits a modified comparator with the ability of rail-to-rail OC and KBNR. The modified rail-to-rail comparator also eliminates the need to use an additional reference supply voltage in the ADC structure.

The proposed structure was able to achieve 11.1-bit ENOB with mismatched input devices. To achieve these performances, an improved version of BS switch was proposed resulting in the reduction of voltage error and power consumption of the S&H switch by 48% and 18.9% respectively. The circuit techniques presented in this paper allow the reduction of the input capacitance in SAR ADC which results in the reduction of the power consumption from the input power supply to 0.04 μW. This has subsequent benefits in terms of energy saving in power-hungry input buffers used by conventional SAR ADCs opening the doors to further reducing the power consumption in portable IoT devices with limited battery life.

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