0.35-V SR-Enhanced Bulk-Driven OTA for Loads up to 10 nF

Andrea Ballo, *Member, IEEE*, Ramón G. Carvajal, *Fellow, IEEE*,
Alfio Dario Grasso, *Senior Member, IEEE*, Clara Luján-Martínez, *Senior Member, IEEE*,
Salvatore Pennisi, *Fellow, IEEE*, and Chiara Venezia

***Abstract*— This study presents a low-voltage bulk-driven CMOS operational transconductance amplifier (OTA) operating in the subthreshold region designed to drive loads up to 10 nF, which is the largest value for this class of amplifiers. To meet this goal, the solution exploits the body terminal of various active devices leveraging local positive feedback to enhance the input transconductance gain and implementing dynamic threshold voltage control in the output transistors. This, along with a Slew Rate Enhancer section, significantly improves the OTA current driving capability. Experimental measurements conducted on a prototype, implemented in a 60-nm technology and supplied from 0.35 V, confirm the expected performance demonstrating a SR of 1.1 V/ms for a 10-nF load with a limited quiescent current consumption of 1.4 µA.**

***Index Terms*— Bulk-driven, CMOS analog integrated circuits, low-voltage, operational transconductance amplifier.**

I. INTRODUCTION

The growing demand for ultra-low-voltage, ultra-low-power integrated circuits (ICs) in portable, wearable, and implantable electronics, [1]-[3], necessitates the exploration of novel circuit topologies and design methodologies aimed to preserve the performance characteristics of well-established complementary metal-oxide-semiconductor (CMOS) solutions while optimizing, particularly in the analog domain, input/output voltage swing and minimizing required supply voltage.

To this end, the application of body-driven (BD) techniques has attracted considerable attention among circuit designers in recent years [4]-[8]. This interest stems from the advantageous absence of a threshold voltage when driving MOS field-effect transistor (MOSFET) devices via their body terminals. The suitability of the BD approach has been proven, specifically in the realization of Operational Transconductance Amplifiers (OTAs) operating under supply voltages as low as 250 mV [9]-[29].

Notably, this methodology facilitates the attainment of the widest common-mode input range, approaching the rail-to-rail limit. Additionally, it often results in overall quiescent current consumption of a few microamperes or less, achieved through suitable biasing of MOSFETs in their sub-threshold region.

A severe limitation arises when comparing BD CMOS OTAs with standard gate-driven counterparts, wherein the constrained body transconductance, constituting a fraction of the gate transconductance, leads to a simultaneous reduction in overall voltage gain, gain-bandwidth product (GBW), and an increase of the equivalent input noise. Addressing this challenge is a prevalent trend in the current literature and involves the design of solutions aimed at improving the OTA's small signal performance, encompassing parameters such as gain, gain-bandwidth, and settling time. Techniques such as gain-boosting, partial positive feedback, quasi floating gate, and current recycling have been adopted [12], [15], [18], [20] concurrently accompanied by an effort in reducing quiescent current consumption [13], [14], [17]. Another issue with BD structures is the need to prevent the body-source junction from turning on. Fortunately, this is not a significant concern when the supply voltage is below 500 mV [6].

It is noteworthy that the adoption of extremely low supply voltages, on the order of a few hundred millivolts, mandates an equivalent maximum OTA output voltage swing, consequently rendering slew rate (SR) performance a matter of marginal interest in initial implementations which also targeted GBW limited to a few kilohertz. Nonetheless, as mentioned above, recent research has focused on endowing circuits with larger GBW and off-chip driving capabilities, prompting investigations into OTAs that demonstrate closed-loop stability with capacitive loads in the range of several tenths of picofarads [21], [22]. In this context, SR emerges as an important limiting factor in the amplifier's time response. Particularly, for class A but also class AB solutions, the combination of substantial load capacitance (hundreds of picofarads) and limited standby current (a few microamperes or less) may yield insufficient SR performance. Experimental observations have often indicated unbalanced positive and negative SR values in these scenarios. In light of this, a (limited) number of studies have delved into SR enhancement techniques, as exemplified by the findings detailed in [20] which showcased the feasibility of a 91-nA OTA effectively driving a 15-pF load and achieving a

Corresponding Author: S. Pennisi, salvatore.pennisi@unict.it.
A. Ballo, A.D. Grasso, S. Pennisi and Chiara Venezia are with the DIEEI (Dipartimento di Ingegneria Elettrica Elettronica e Informatica), University of Catania, I-95125 Catania, Italy (e-mail: andrea.ballo@unict.it; alfiodario.grasso@unict.it; salvatore.pennisi@unict.it, chiara.venezia@phd.unict.it).

R. G. Carvajal and C. Luján-Martínez are with the Electronic Engineering Department, University of Sevilla, Camino de los Descubrimientos s/n E-41092, Sevilla, Spain (e-mail: carvajal@us.es; cilujan@us.es).

noteworthy SR of 8.6 V/ms. Other examples of class AB BD OTAs can be found in [12], [19], [22], [25]

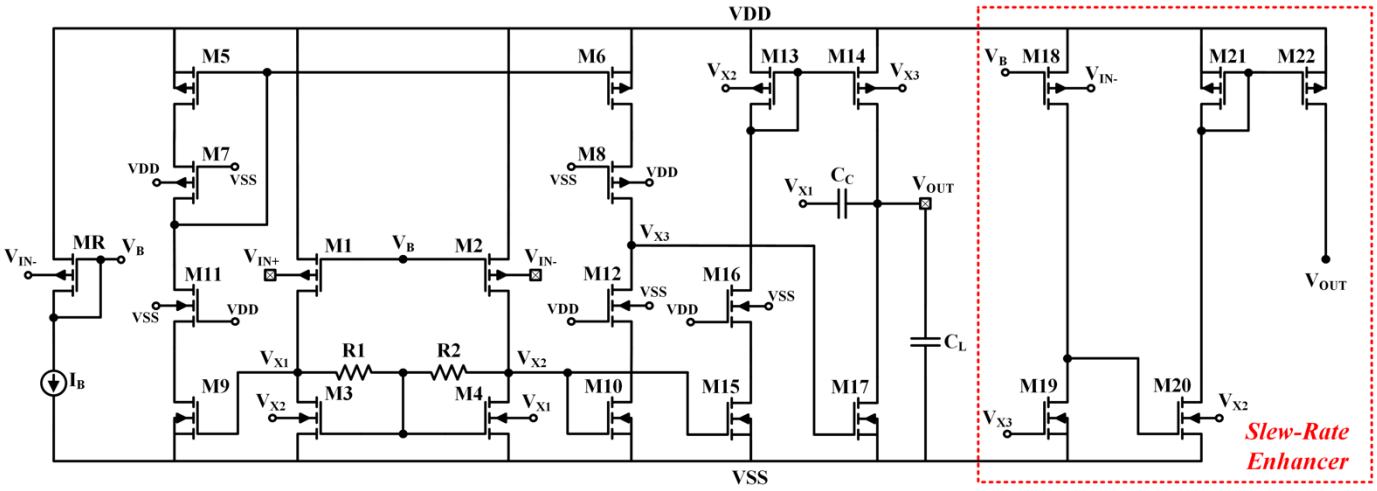

Fig. 1. Schematic diagram of the proposed BD OTA.

This manuscript delves into design solutions aimed at improving the SR performance of a tail-less BD OTA. Our approach involves leveraging the body terminal of various transistors, particularly those in the output stage's class AB section, to implement dynamic threshold voltage control. This strategy, combined with the integration of a SR Enhancer (SRE) subsection, enables the OTA to effectively drive load capacitors of up to 10 nF. Notably, the SRE operates in an off state under quiescent conditions, enhancing the output current in the weaker pull-up driving path. This contributes to an overall improvement in SR performance without a significant increase in quiescent current consumption. It is important to highlight that, amplifiers capable of driving large capacitive loads, even in the nanofarad range with kilohertz bandwidth, are required in many applications, such as line drivers, low-dropout regulators (LDOs), LCD column drivers, micro-electro-mechanical systems (MEMS) sensors, headphone drivers, etc., [31]-[34].

The paper is organized as follows. The presented solution is described in Sec. II, where particular focus is directed towards elucidating the primary novel design solutions and fundamental design equations. Section III delves into the simulations conducted to assess the proposed solution, while Section IV discusses the experimental results obtained. The paper is concluded with the authors presenting their findings and drawing conclusions.

II. The Proposed Solution

The proposed solution was derived from the configuration presented by the same authors in a prior work [22], which provided effective quiescent current control and demonstrated also excellent small signal and large signal performance metrics. In the present study, we have incorporated several SR-enhancement techniques onto this established framework, thereby seeking further refinement in the amplifier's dynamic response characteristic even under lower quiescent current and larger capacitive load.

A. Topology, biasing, and large signal operation

The simplified schematic diagram of the proposed OTA is depicted in Figure 1. The input stage is realized through transistors M1 and M2, constituting a tail-less body-driven p-channel transistor pair. The quiescent current of this pair is established by I_B and diode-connected transistor MR. Consequently, the quiescent current flowing through M1 and M2 is determined by I_B multiplied by the mirror ratio $(W/L)_{1,2}/(W/L)_R$. Note that, owing to the OTA's input virtual short, these transistors share at DC the same body voltage and hence the same threshold voltage.

The active load for the input stage is formed by transistors M3 and M4, incorporating negative-feedback resistors R1, R2 crucial for the differential-mode gain. Moreover, this load configuration imparts differential capability to the inherently pseudo-differential pair [12]. Notably, local positive feedback is introduced by cross-connecting the body of M3 to the drain of M4 and the body of M4 to the drain of M3, thereby enhancing the equivalent input-stage transconductance [22].

The second stage, providing cascoded high-output-impedance and differential-to-single-ended conversion, is implemented by transistors M5-M12. The quiescent current in this stage is determined by the mirroring action between the pair M3, M4 and M9, M10, because, at DC, no current flows through resistors R1-R2, rendering M3 and M4 as diode-connected devices. Note that being $V_{BS3,4} = V_{GS3,4}$ while $V_{BS9,10} = 0$ this current mirror gain is found to be

$$\frac{I_{D9,10}}{I_{D3,4}} = \frac{(W/L)_{9,10}}{(W/L)_{3,4}}\left[1-\frac{\gamma\left(\sqrt{2\phi_F+V_{GS3,4}}-\sqrt{2\phi_F}\right)}{V_{GS3,4}-V_{Tn0}}\right]^{-2} \quad (1)$$

where the threshold voltage of a nMOS is expressed usual by

$$V_{Tn} = V_{Tn0} + \gamma\left(\sqrt{2\phi_F+V_{BS}}-\sqrt{2\phi_F}\right) \quad (2)$$

and being V_{Tn0} the zero-bias threshold, ϕ_F the Fermi potential and γ the body effect parameter. As a result, the current mirror ratio in (1) is lower than that of a conventional current mirror in which the factor in the square brackets equals 1.

The output stage, which drives the load capacitor C_L, is made up of common-source transistor M17, complemented by active

load M13-M16. The quiescent current of the output branch is regulated by the current mirror gains of M3,4 to M15 and of M13 to M14. It is noteworthy that the pull-down output current supplied by M17 may exceed the quiescent value, akin to the pull-up current provided by M14, albeit to a lesser extent. Therefore, both M14 and M17 operate in class AB, but the positive-going output step exhibits a slower response than its negative-going counterpart owing to the diminished maximum possible variation of voltage V_{X2} (*i.e.*, the gate-source voltage of M15) compared to V_{X3} (*i.e.*, the gate-source voltage of M17) in Fig. 1.

To improve the positive SR of the basic solution, a first modification involves a dynamic adjustment of the gain in the current mirror formed by transistors M13-M14, dependent upon the required current level to be delivered. This objective is achieved by connecting the body of transistor M13 to the drain of M4 and the body of transistor M14 to the drain of M8 (M12), as illustrated in Fig.1. This configuration exploits the dependence of the threshold voltage of M13 and M14 to variations in V_{X2} and V_{X3}. Specifically, when the output stage is tasked with supplying current, an increase in V_{X2} and a corresponding reduction in V_{X3} occurs, thereby incrementing the threshold voltage of M13 and decrementing that of M14 and increasing in turn the current mirror gain.

As an illustration of the process involved, consider Fig. 2a, wherein a p-channel current mirror analogous to M13-M14 in Fig. 1 is implemented using transistors MC1-MC2. These transistors share identical aspect ratios of 40/0.5 and have bulk voltages V_{B1} and V_{B2}, respectively. The current mirror attains a unitary gain provided that the bulk voltages are equal (in our case $V_{B1} = V_{B2} = V_{DD}$−0.15 V). Figure 2b depicts the current gain of the mirror in response to a variation in V_{B1}−V_{B2}. Notably, a substantial current gain increase, reaching up to a factor of five, is evident for $V_{B1} > V_{B2}$. Conversely, a current gain decrease is observed for $V_{B1} < V_{B2}$.

The second improvement is accomplished by the inclusion of a Slew-Rate Enhancer (SRE) section made up of transistors M18-M22. The objective of the SRE is to augment the current supplied by the OTA to the load, as done for instance in [27]. Essentially, it introduces an additional driving branch operating in parallel to transistor M14 and functions as follows. Transistor M18 serves as a constant current source, mirroring the current from MR, I_B, with a gain reduction determined by the ratio $(W/L)_{18}/(W/L)_R$. Note that the bulk of M18 is tied to IN− only to provide an accurate and predictable current mirror matching with MR. Concurrently, transistor M19, matched in V_{GS} with M17, is dimensioned such that under DC conditions, the nominal current through M17 multiplied by $(W/L)_{19}/(W/L)_{17}$ surpasses I_{D18}. Hence, under quiescent conditions, this configuration maintains a low drain voltage across M19, consequently deactivating transistors M20 and, in turn, M21 and M22. Under large signal conditions, when V_{IN+} increases and a similar increase in V_{OUT} is required, V_{X2} rises augmenting the current in M15 and M14, while V_{X3} decreases turning off M16. This action results in an elevation of the drain voltage across M19, turning on M20. Subsequently, through the mirror M21-M22, M22 contributes its drain current in parallel with that of M14, thereby reinforcing the current supplied to the load capacitor C_L. It is worth noting that the SR enhancement performance is further empowered by driving the bulk of M20 by V_{X2}, so that the threshold voltage of M20 decreases when I_{D20} must increase.

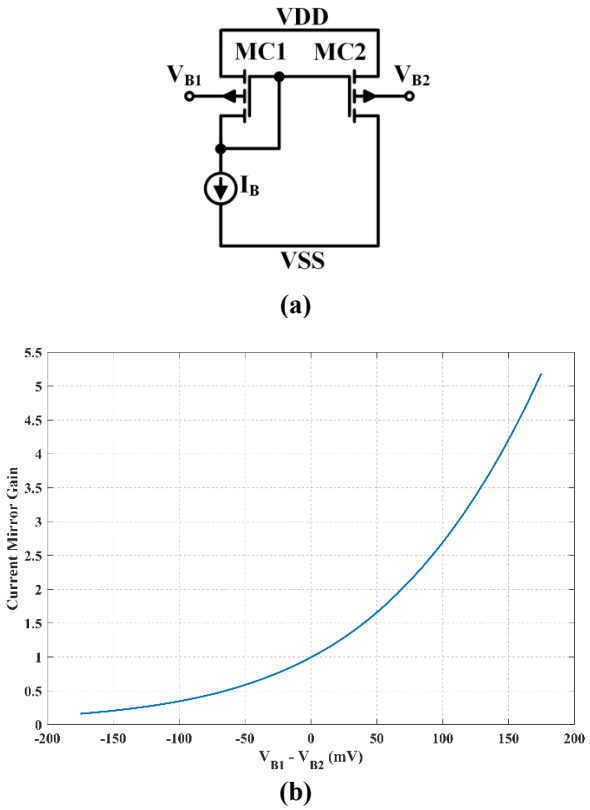

Fig. 2. Variable-gain current mirror: a) Schematic diagram, b) DC current-mirror gain I_{DC2}/I_{DC1} as a function of V_{B1}-V_{B2}. Transistors dimension is 40/0.5 with the models of a 60nm CMOS technology.

A concluding remark concerns the connection of the body of MR, and thereby of M18, to the inverting input, IN−. This configuration is simpler compared to connecting these terminals to the common-mode input voltage, a step necessary in theory to nullify the common-mode gain of the input stage. This method eliminates the need for extracting the common mode of the two inputs.

B. Small-signal analysis

The overall OTA differential gain is given by

$$A_0 \approx G_{mb} r_{o1} g_{m9,10} r_{o2} g_{m17} r_{o3} \tag{3}$$

where g_{mi} is the gate transconductance of the i-th transistor and where r_{o1}, r_{o2} and r_{o3} are the output resistances of the first, second, and third stage, respectively equal to $R_{1,2}//r_{d1,2}//r_{d3,4}$, $(g_{m12} r_{d12} r_{d10}) // (g_{m8} r_{d8} r_{d6})$, and $r_{d14}//r_{d17}$. Moreover, G_{mb} is the equivalent input transconductance expressed by

$$G_{mb} = \frac{g_{mb1,2}}{1 - g_{mb3,4} r_{o1}} \tag{4}$$

where $g_{mb1,2}$ and $g_{mb3,4}$ are the bulk transconductances of

transistors M1-M2 and M3-M4, respectively.

As already mentioned, (4) shows that the differential-mode transconductance of the first stage is increased through positive feedback from the bulk-drain cross-connection of transistors M3 and M4. This result is similar to that found in [22]. During the design phase, careful attention should be given to ensuring that the denominator in (4) remains consistently positive across all process corners and temperature conditions. In summary, the strategy to achieve gain increase involves setting the denominator of (4) to be substantially less than 1 to avoid instability issues, as described in Sec. III.

Concerning frequency compensation, it is important to note that we follow the approach outlined in [22]. In this strategy, the dominant pole is established by Miller capacitor C_C for lower values of C_L (typically in the range of a few picofarads). However, compensation is shifted to the output pole for larger C_L values. This ensures OTA closed-loop stability over a wide range of load conditions. In this context, the dominant-pole angular frequency is found to be

$$\omega_{p1} \approx \frac{1}{g_{m9,10} g_{m14} r_{o1} r_{o2} r_{o3} C_C + r_{o3} C_L} \tag{5}$$

where the effect of C_C and C_L in the frequency compensation is apparent. The gain-bandwidth product, GBW, is of course given by the product of (3) and (5).

The proposed OTA was designed using a 65-nm CMOS bulk technology provided by TSMC and accessed through EUROPRACTICE. Component dimensions and bias elements are summarized in Table I. Supply is set to 0.35 V and the bias current I_B is 200 nA. A deliberately chosen lower overall current, compared to [22], is employed to accentuate the improvement in SR, albeit resulting in a lower GBW.

TABLE I
STEP DIMENSION OF ACTIVE AND PASSIVE COMPONENTS AND BIAS ELEMENTS

Device	W/L (µm/µm) × Multiplicity	Device / Parameter	W/L (µm/µm) × Multiplicity / Value
MR, M1, M2	(50 / 0.5) × 1	M17	(50 / 2) × 3
M3, M4	(60 / 4) × 1	M18	(2 / 0.5) × 1
M5, M6	(50 / 1) × 4	M19	(50 / 2) × 1
M7, M8	(50 / 0.5) × 2	M20	(20 / 0.5) × 1
M9, M10	(60 / 4) × 4	M21, M22	(50 / 0.5) × 2
M11, M12, M16	(60 / 4) × 3	V_{DD}	0.35 V
M13	(40 / 0.5) × 1	I_B	200 nA
M14	(40 / 0.5) × 14	R1, R2	250 kΩ
M15	(20 / 4) × 5	C_C	6.1 pF

III. DESIGN AND SIMULATION RESULTS

Some results of preliminary post-layout simulations are discussed in this section. The open loop frequency response (magnitude and phase) of the OTA with C_L = 300 pF is shown in Fig. 3 in nominal transistor conditions (TT case) and in the four process corners. The nominal DC gain is equal to 55.6 dB and the GBW is equal to 23 kHz. Phase margin (PM) is equal to 60° and the gain margin is equal to 8.9 dB. Note that $g_{mb3,4}r_{o1}$ was set about equal to 0.4, hence providing a 1.7 boost in the transconductance, as anticipated by (4). Stable performance is demonstrated also across the process corners from the same Fig. 3.

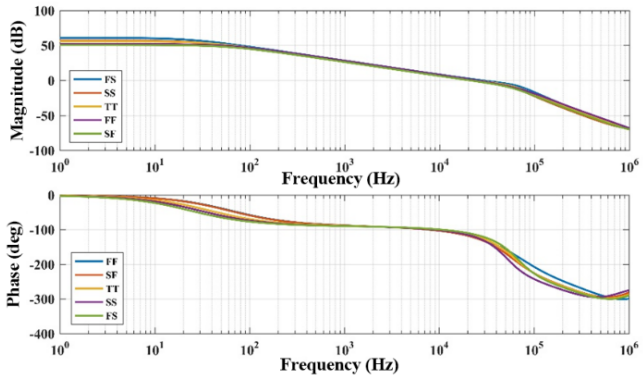

Fig. 3. Bode plots of OTA loop gain (magnitude and phase) across corners.

The robustness against process and mismatch variations was validated through Monte Carlo simulations, comprising 1000 iterations, as depicted in Fig. 4(a), (b), and (c) for DC gain, GBW, and PM, respectively, whose standard deviations are 2.17 dB, 2.07 kHz, and 4.67 degrees, respectively.

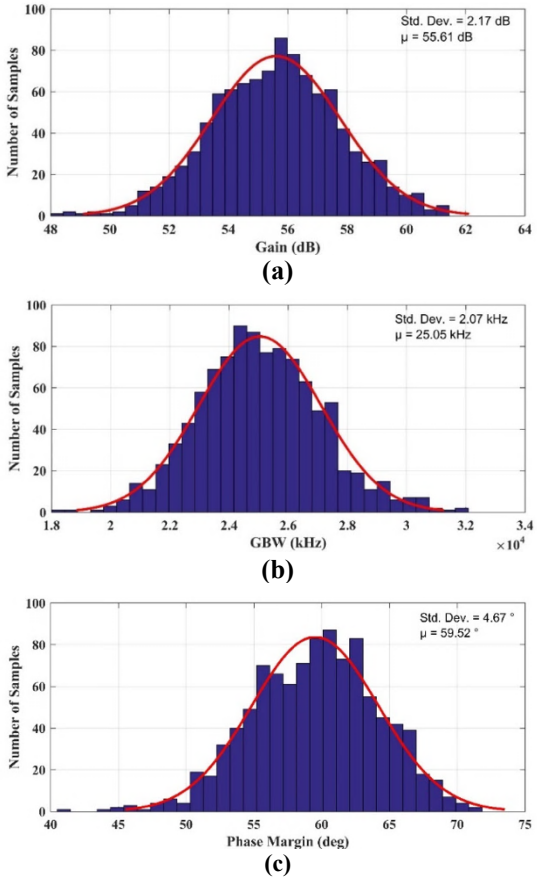

Fig. 4. Montecarlo simulations of OTA DC gain (a), GBW (b), and PM (c).

Temperature-induced variations of the DC gain, GBW, and PM are simulated within the typical process model across a temperature span ranging from 0 °C to 100 °C. The summarized findings are presented in Table II, revealing nearly

constant values of GBW with marginal variations in DC gain. Although PM exhibits a 24-degree variation, it remains within acceptable bounds, indicating satisfactory stability.

The simulation also included an assessment of the Common Mode Rejection Ratio (CMRR). The DC value achieved is 58.1 dB, representing a more than 15-dB improvement compared to the findings in [22]. Additionally, a Monte Carlo simulation of CMRR was performed, indicating a standard deviation of 1.73 dB, as depicted in Fig. 5.

TABLE II
DC GAIN, GBW AND PM IN THE TYPICAL CORNER AT DIFFERENT TEMPERATURE VALUES

Temp. (°C)	0	27	60	80	100
DC gain (dB)	55.1	55.6	56.2	55.6	51.9
GBW (MHz)	0.023	0.023	0.026	0.026	0.025
PM (deg)	52	60	68	72	76

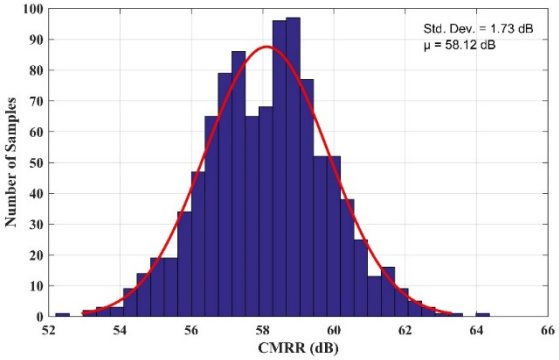

Fig. 5. Montecarlo simulations of the CMRR.

The simulated input noise spectral density is shown in Fig. 6, at 1 kHz it is around 829 nV/√Hz (white noise).

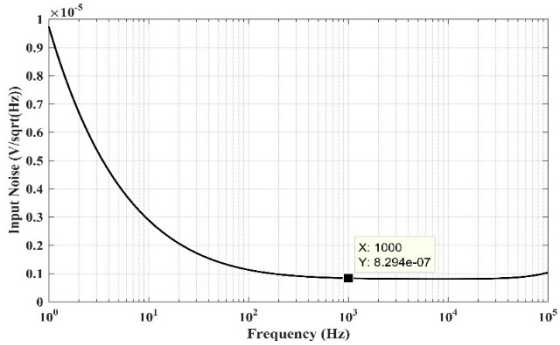

Fig. 6. Equivalent input noise.

Figure 7 shows the response to a 200-mV$_{p\text{-}p}$ input step of the proposed SR-enhanced OTA in buffer configuration, compared to a version of the same OTA that does not include SR enhancement strategies, both driving 300 pF. In other words, with reference to Fig. 1, the latter case does not include the SRE section and transistors M13-M14 have their bulks conventionally tied to V_{DD} whereas M19 to V_{SS}. Evidently, the positive-going output step exhibits a slower response compared to the negative-going counterpart. The application of the SR enhancement techniques markedly enhances this performance. Specifically, the positive SR without SRE is found to be 5 V/ms, while the positive SR value with SRE is notably improved, more than 4 times, to 23 V/ms.

The time response across the five fundamental process corners and under the identical conditions detailed above is illustrated in Fig. 8. The main outcomes are succinctly outlined in Table III. Remarkably, the SRE techniques render the positive Slew Rate (SR+) nearly insensitive to variations across the different corners.

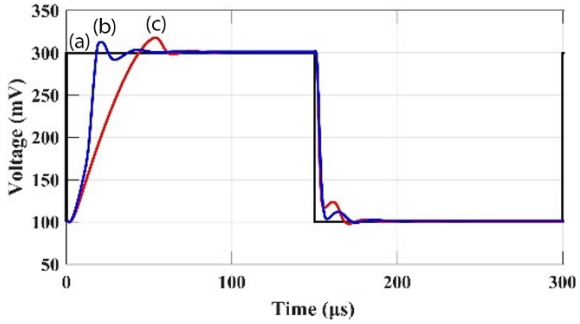

Fig. 7. Simulated time response of the OTA in buffer configuration (C_L = 300 pF): input 200-mV$_{p\text{-}p}$ step (curve a), output with (curve b), and without (curve c) SRE techniques.

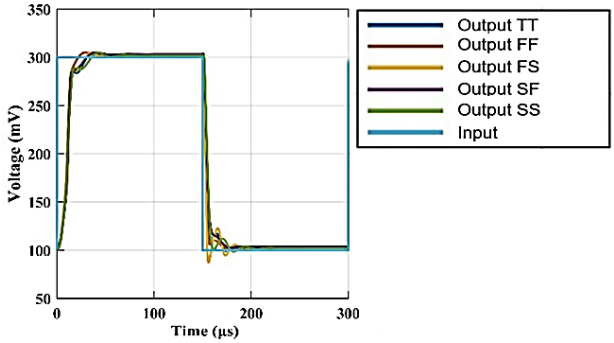

Fig. 8. Simulated output response of the OTA in unity gain to a 200-mV$_{p\text{-}p}$ input step over five basic corners (C_L = 300 pF).

TABLE III
STEP RESPONSE OF THE OTA IN BUFFER CONFIGURATION OVER CORNERS (C_L = 300 PF)

Corner	TT	FF	FS	SF	SS
SR+/SR− (V/ms)	23/−51	22/−61	21/−76	22/−33	18/−32
1% Settling Time (pos/neg) (μs)	37/34	30/22	36/33	40/45	41/52

IV. MEASUREMENT RESULTS AND COMPARISON WITH PRIOR ART

The micrograph of a fabricated prototype of the proposed circuit is illustrated in Fig. 9. The occupied area is 223 μm × 235 μm with the SRE accounting for approximately 13% of the total area. It is apparent that no area optimization technique was adopted for this prototype. The circuit is supplied with 0.35 V and the measured current consumption is 1.4 μA. Fig. 10 depicts the gain magnitudes of the OTA in buffer configuration with 300-pF and 10-nF load capacitors. The −3dB frequency is around 16 kHz and 650 Hz, respectively.

The Total Harmonic Distortion (THD) of the output voltage

versus frequency with the OTA in unity gain and with C_L = 300 pF, for different input amplitudes is shown in Fig. 11. THD below 1% is achieved for inputs below 200 mV_{p-p} and 500 Hz.

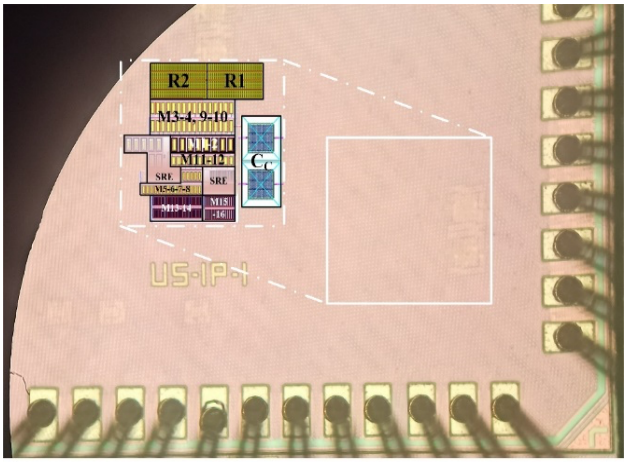

Fig. 9. Chip micrograph.

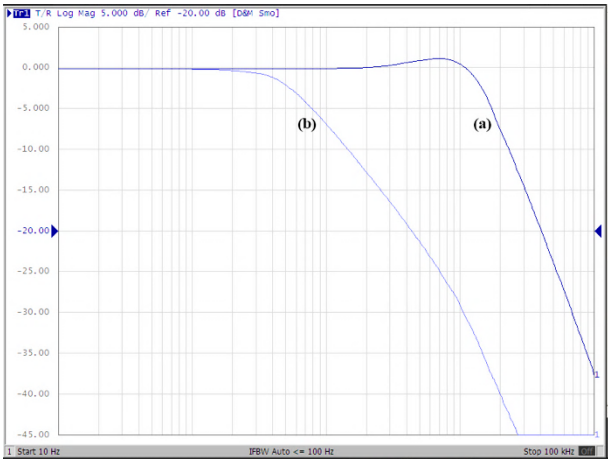

Fig. 10. Measured gain magnitude of the OTA in buffer configuration with C_L= 300 pF trace (a), and with C_L = 10 nF trace (b).

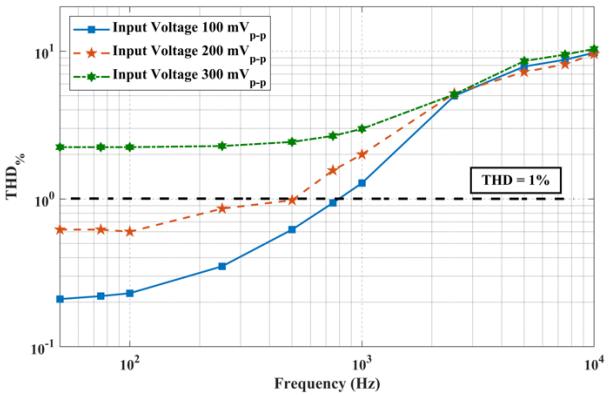

Fig. 11. Measured THD (%) versus frequency of the OTA in buffer configuration (C_L=300 pF) for three different inputs.

Fig. 12 shows the response to a 200-mV_{pp} step of the OTA in unity gain driving a 100-pF load. To highlight the effect of the adopted SR-enhancing techniques, Fig. 13 compares the response to the same input step of the OTA in unity gain loaded by 10 nF with and without the SR enhancer (traces b and c, respectively). The positive-going part of trace b is clearly improved, and it is now comparable with the negative going one. SR+ and SR− are 1.1 V/ms and 1.4 V/ms, respectively.

The main OTA performance parameters, with C_L = 300 pF, are summarized in Table V. Measurement results match well with simulations. SR is large although slightly lower than what anticipated.

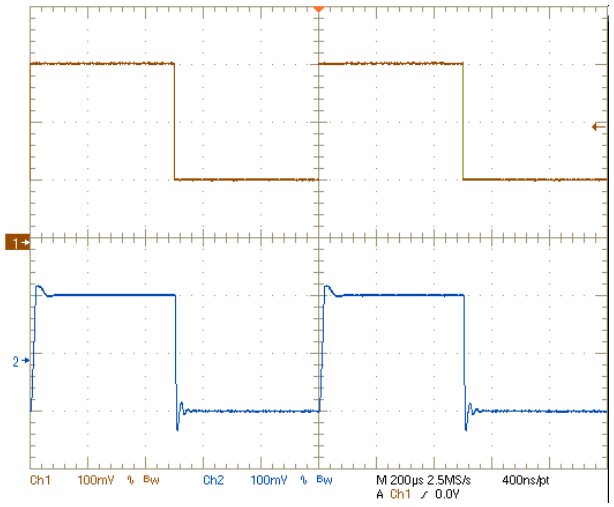

Fig. 12. Measured step response of the OTA in unity gain with C_L = 100 pF: 200-mVpp input step (upper trace) and output signal (lower trace).

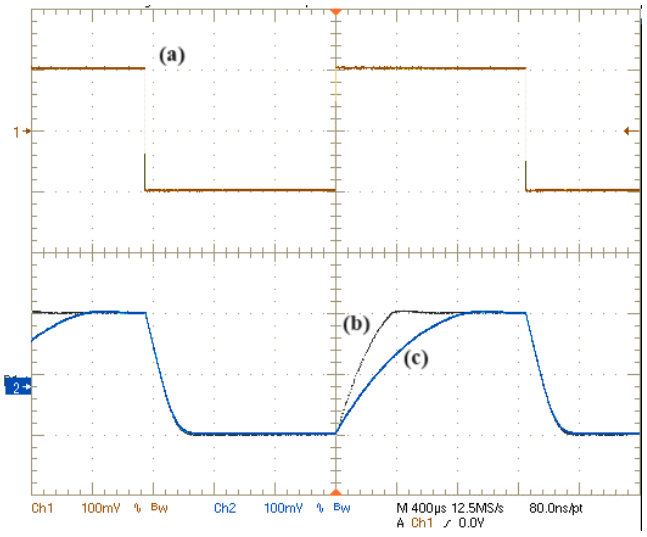

Fig. 13. Measured step response of the OTA in unity gain and with C_L = 10 nF: 200-mV_{p-p} input step (trace a), output (trace b) and output without SRE (trace c).

Finally, Table VI compares the proposed OTA with the state

of the art. It is apparent that our design is the sole to be able to drive up to 10 nF and with very good current efficiency, given the maximum value of the figure of merit $IFOM_L$ (equal to $SR \cdot C_L/I_Q$) achieved. A very good $IFOM_S$ is also observed. It is noteworthy, however, that this metric is not optimized intentionally through the utilization of an exceedingly low quiescent input stage current. As a principal drawback, the OTA is characterized by the largest silicon area occupation. Indeed, while the SRE does not occupy a significant portion of the area, the OTA necessitates transistors with large overall aspect ratios to effectively drive the intended load capacitance. This aspect adversely affects our design when considering the figures of merit, $IFOM_{AS}$ and $IFOM_{AL}$, as shown in the last two rows of Table VI.

TABLE V
OTA MAIN PERFORMANCE (C_L = 300 PF)

Parameter (unit)	Value
Supply Voltage (V_{DD}−V_{SS}) (V)	0.35
DC Current (μA)	1.4
Offset maximum (mV), 5 samples	6.4
Input Common-Mode Range	>90%(V_{DD}-V_{SS})
Max Input Current* (nA)	0.224
DC Gain (dB)*	>50 dB
GBW (kHz)	15.4
Phase Margin (deg)	65
Gain Margin (dB)	8.9
SR+/SR− (V/ms)	14.4/21.4
CMRR*@DC (dB)	58
PSRR$^{+,-}$*@DC (dB)	26.5
Input Ref. Noise* @1kHz (nV/√Hz)	829
THD@500Hz, 200mV_{p-p} (%)	0.98

*Simulated values

TABLE VI
PERFORMANCE COMPARISON OF SUB-1V AMPLIFIERS

Ref.	[28] Qin	[12] Cabrera	[29] Grasso	[13] Kulej	[15] Kulej	[16] Woo	[22] Ballo		[26] Della Sala	Proposed		
Year	2016	2016	2017	2018	2020	2020	2023		2023	2024		
Op. mode*	GD	BD	GD	BD	BD	BD	BD		BD	BD		
Tech. (nm)	180	180	350	180	180	65	65		130	65		
***Area* ($mm^2 \times 10^{-2}$)**	1.82	1.98	1.43	0.82	0.98	0.23	0.106		0.234	5.2		
V_{DD} (V)	0.5	0.7	0.7	0.3	0.3	0.25	0.3		0.3	0.35		
I_Q (μA)	0.14	36	27	0.056	0.043	0.104	8.5		0.11	1.4		
C_L (pF)	40	20	10	20	30	15	50	150	35	300	1000	10000
DC gain (dB)	77	57	65	63	98.1	70	38		87	55		
***GBW* (MHz)**	4 10^{-3}	3	1	2.8 10^{-3}	3.1 10^{-3}	9.5 10^{-3}	1.65	0.81	10.3 10^{-3}	15.4 10^{-3}	6.48 10^{-3}	6.54 10^{-4}
***PM* (°)**	56	60	60	61	54	88	70.3	71.3	58.3	65	73	82
***PSRR* @DC (dB)**	52	52	50	62	61	38	44.7		46.6	26.5		
***CMRR* @DC (dB)**	55	19	45	72	60	62.5	39.8		57.8	58		
SR (V/μs)**	2 10^{-3}	1.8	0.25	6.4 10^{-3}	4.2 10^{-3}	2 10^{-3}	0.11	0.07	2.5 10^{-3}	14 10^{-3}	10 10^{-3}	1.1 10^{-3}
***IFOM$_S$* (MHz·pF/μA) (1)**	1.14	1.67	0.37	1.00	2.16	1.37	9.71	14.29	3.3	3.3	4.63	4.67
***IFOM$_L$* (V/μs·pF/μA) (2)**	0.57	1.0	0.09	2.29	2.93	0.29	0.65	1.24	0.80	3.0	7.14	7.85
***IFOM$_{AS}$* (MHz·pF/(μA·mm^2)) (3)**	62.64	84.34	25.87	121.95	220.41	595.65	9160.4	13481	1410.3	63.46	89.04	89.81
***IFOM$_{AL}$* (V/μs·pF/(μA· mm^2)) (4)**	31.32	50.51	6.29	279.27	298.98	126.09	613.21	1165.81	341.88	57.69	137.31	150.96

* GD: gate-driven; BD: bulk-driven; ** The minimum between SR+ and SR−.

(1) $IFOM_S = \frac{GBW}{I_Q} C_L$, (2) $IFOM_L = \frac{SR}{I_Q} C_L$, (3) $IFOM_{AS} = \frac{GBW}{I_Q \cdot Area} C_L$, (4) $IFOM_{AL} = \frac{SR}{I_Q \cdot Area} C_L$

V. CONCLUSION

The paper builds upon a previously introduced low-voltage CMOS OTA that employs MOSFETs in the subthreshold region. The authors strategically leverage the body terminal of various active devices to enhance large signal performance. In addition to implementing local positive feedback for improved input transconductance, the paper introduces dynamic threshold voltage control in the output transistors. This, combined with a Slew Rate Enhancer section, enables the OTA to efficiently drive a load capacitor (C_L) up to 10 nF, the largest reported for this class of amplifier. The frequency compensation scheme uses Miller compensation for low C_L and shifts to dominant-pole compensation for high C_L. Experimental measurements on a prototype in a 60-nm technology, powered by 0.35 V, confirm the expected performance providing the best large-signal figure of merit ($IFOM_L$).

VI. ACKNOWLEDGMENT

This work was developed under project SAMOTHRACE (ECS00000022) funded by European Union (NextGeneration EU), through the MUR-PNRR, and under projects PID2021-

127712OB-C22 and TED2021-131075B-I00 funded by MCIN/AEI/ 10.13039/501100011033 and, as appropriate, by the "European Union NextGenerationEU/PRTR" and the "ERDF A way of making Europe".

The authors would like to thank Dr. José María Hinojo for his support during design.

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Andrea Ballo was born in Catania, Italy, in 1990. He received the Laurea degree (summa cum laude) and the Ph.D. degree in electronic engineering from the University of Catania, in 2016 and 2020, respectively. Since 2021, he has been a Research Fellow and an Adjunct Professor of electronic devices with the University of Catania. His current research interests include low-voltage low-power analog circuit design and analog and mixed electronics for energy harvesting applications. He is an Associate Editor of the Journal of Circuits, Systems and Computers, a member of the editorial board of Journal of Electronics and Electrical Engineering (Universal Wiser Publisher), and a member of the topical advisory panel of different journals, such as Applied Sciences (MDPI) and Electronics (MDPI).

Ramón Gonzalez-Carvajal, received the M.Sc. degree in electrical engineering and the Ph.D. degree from the University of Sevilla, Sevilla, Spain, in 1995 and 1999, respectively. He was an Invited Researcher with the Klipsch School of Electrical Engineering, New Mexico State University (NMSU), Las Cruces, NM, USA, in 1999 and from 2001 to 2004, and also with the Department of Electrical Engineering, Texas A&M University, College Station, TX, USA, in 1997. He was an Adjunct Professor with the Klipsch School of Electrical Engineering. Since 1996, he has been an Associate Professor with the Department of Electronic Engineering, School of Engineering, University of Seville, where he has been Professor, since 2002. He has authored over 150 papers in international journals and 200 in international conferences. His current research interests include low power and low voltage analog and mixed design, energy efficient embedded systems, the Internet of Things (IoT) for smart cities, and automotive applications.

Alfio Dario Grasso (Senior Member, IEEE) was born in Catania, Italy, in 1978. He received the Laurea degree (summa cum laude) and the Ph.D. degree in electronic engineering from the University of Catania, Catania, in 2003 and 2006, respectively. From 2006 to 2011, he was a Freelance Engineer in electronic systems. From 2009 to 2010, he was an Adjunct Professor in electronics with the Kore University of Enna, Italy. In 2011, he became a Researcher (an Assistant Professor). In 2015, he was appointed as an Associate Professor with the University of Catania. In 2017, he received the Italian National Scientific Qualification for the position of a Full Professor. He teaches graduate courses on advanced VLSI digital design, microelectronics, and basic electronics. He has coauthored more than 120 papers in refereed international journals and conference proceedings. His current research interests include low-voltage low-power analog circuit design and analog and mixed signal processing for energy harvesting applications. He is a member of the editorial board of Sensors (MDPI). He is an Associate Editor of the IET Electronics Letters and the International Journal of Circuits Theory and Applications (Wiley).

Clara I. Luján-Martínez received the B.Sc degree in Telecommunications Engineering and the Ph.D degree from University of Sevilla, Sevilla, Spain, in 2007 and 2009, respectively. She joined the Electronic Engineering Department in 2007, where she is Associate Professor. In 2008, she was a visiting scholar at Imperial College (UK), and in 2011, visiting researcher at NXP Semiconductors (The Netherlands). Her main research interests include low power and low voltage analog and mixed-signal microelectronic design and Internet of Things.

Salvatore Pennisi was born in Catania, Italy, in 1965. He graduated in electronic engineering in 1992 and received his Ph.D. degree in electrical engineering in 1997, both from the University of Catania, Italy. In 2016 he was appointed Full Professor at the University of Catania, where he holds undergraduate and graduate courses in electronics and microelectronics. He is also coordinator of the master's degree course in Electronic Engineering. His main research interests include circuit theory and analog design with an emphasis on low voltage techniques, multistage amplifiers, data converters, high frequency distortion analysis, driver circuits for liquid crystal displays and micro-energy harvesting. He has published more than 115 articles in international journals (62 of which in IEEE journals), more than 120 contributions in conference proceedings and is co-author of the books CMOS Current Amplifiers (1999), Feedback Amplifiers: Theory and Design (2001) both published by Kluwer Academic Publishers, and Liquid Crystal Display Drivers Techniques and Circuits (Springer 2009). Dr. Pennisi is a member of the IEEE CASS Analog Signal Processing Technical Committee and was Associate Editor of IEEE Transactions on Circuits and Systems-Part II: Express Briefs and of the Wiley International Journal of Circuit Theory and Applications.

Chiara Venezia received the B.S. and M.Sc. degree in Electronics Engineering from the University of Catania, Italy, in 2018 and 2020, respectively. She earned the Ph.D. in Electronics Engineering and the title of Doctor Europaeus in November 2023. She was a Visiting Ph.D. Student at Universidad de Sevilla, Spain (2022-2023) and she had also undertaken an Internship for the M.Sc. degree thesis and an Internship during the Ph.D. program both in cooperation with STMicroelectronics. Her main research activity was focused on the design of CMOS low-current and low-voltage analog building blocks particularly voltage references and Operational Transconductance Amplifiers. Since September 2023, she has joined Analog Devices as a Senior Analog Design Engineer working on the design of a buck-boost DC-DC controller involving GaN-based power devices.