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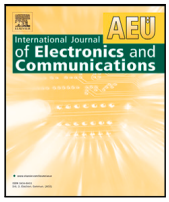

Regular paper

A 4.2–13.2 V, on-chip, regulated, DC–DC converter in a standard 1.8V/3.3V CMOS process☆

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ABSTRACT

This paper presents a fully on-chip HV-regulated DC–DC boost converter for the power management unit of an electrical neural stimulator. The core of the DC–DC converter consists of a 4x4 array of individually-configurable charge pumps. The rows and columns of the array can be dynamically enabled or disabled, thus extending the range of suitable output voltages and load currents. Additionally, the converter includes a feedback loop for output voltage regulation which allows responding to abrupt changes in the load current within a few microseconds. The circuit has been designed in a standard 180 nm 1.8V/3.3V CMOS process and occupies an active area of 2.1 mm^2. An exhaustive experimental characterization of the proposed circuit was carried out. Experimental results demonstrate that, for an input voltage of 3 V, the DC–DC converter's regulated output ranges from 4.2 V to 13.2 V under load currents of 0.1–4 mA. Maximum delivered power is around 48 mW. The power efficiency of the converter at the highest achievable output voltage under a 4 mA load current is higher than 65% for input voltages above 2.4 V.

1. Introduction

Electrical modulation using implantable devices with arrays of stimulating electrodes is an emerging therapy for neurological diseases. Some examples of neuromodulation devices include prostheses for spinal cord injury; cochlear auditory implants; retinal and cortical visual prostheses; vagus nerve stimulators for epilepsy and depression; or deep brain stimulators for essential tremors and Parkinson's disease. These devices are often combined with a neural recording section for evaluating, and eventually adapting, the stimulation on the tissue, thus resulting in a closed-loop architecture, as shown in Fig. 1. Further, neural implants are often supplied by a wireless power transmission (WPT) mechanism to avoid the use of bulky batteries [1–4].

The efficacy of these implants ultimately depends on their ability to trigger a functional response in the target tissue by inducing a flow of current between two or more electrodes. This is typically done by applying a series of biphasic current pulses with cathodic and anodic phases whose amplitudes and durations are adjusted to result in an overall zero net charge in the tissue [5,6]. A major concern in the implementation of stimulators is the impedance at the Electrode-Tissue Interface (ETI). Such impedance depends on the geometry and materials of the electrodes; the physiological parameters of the tissue; and the degree of electrical contact at the stimulation zone [5]. Further, the interface is not stationary in nature, and the impedance changes throughout the life cycle of the implant. These factors make that the stimulation currents practically range from some tens of μA up to some mA and that the voltage compliance of the current drivers varies from a few volts up to over 10 V [7–10].

To withstand such a broad range of current/voltage values, it is fundamental that the power management unit of the implant, on which this work focuses, includes a programmable DC–DC converter with adjustable Voltage Conversion Ratio (VCR) to guarantee that the stimulator operates under safety limits without excessive power dissipation [11], particularly, when the ETI equivalent impedance and/or the stimulation currents are large. Additionally, to relax the power transfer specifications of the WPT mechanism, the efficiency of the DC–DC converter should reach its peak for large stimulation currents for which the availability of electrical power is more demanding. According to our simulations, the WPT link, currently under design [4], is capable of providing supply voltages around 2.7 V, therefore, the DC–DC converter should operate correctly at those input voltage levels. Last but not least, the DC–DC converter should react rapidly under variations of the load current as occurs in electrical neurostimulation, and use no external component to reduce the form factor of the implant.

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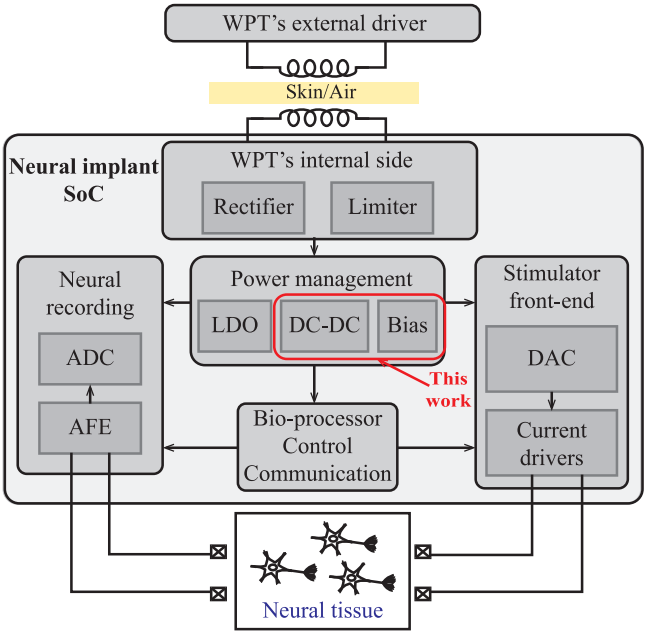


Fig. 1. Block diagram of a neural implant.

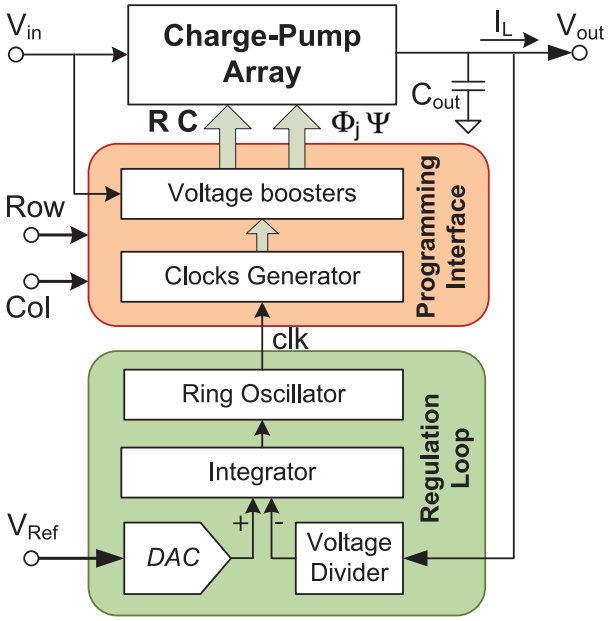


Fig. 2. Simplified schematic of the proposed HV regulated DC–DC boost converter.

These aspects are addressed in this work, where a versatile fully on-chip High-Voltage (HV) DC–DC boost converter for neuromodulation applications is proposed. Instead of using an HV CMOS node, the converter is implemented in a standard 1.8V/3.3 V 0.18 µm CMOS process to allow for a single-chip neural implant integration, along with other elements already designed in this technology [12]. The use of standard processes for the generation of voltages above the nominal supply of the technology demand for circuit solutions that guarantee that voltage drops across devices are safely below the breakdown limits. The approach has been also followed in previous contributions [9,13–18]. However, these solutions present some drawbacks such as the lack of output voltage regulation [14], usage of off-chip capacitors [14,18], generation of a fixed output voltage [9,18], low load current driving capability [14,15,17,18], or low VCR [16].

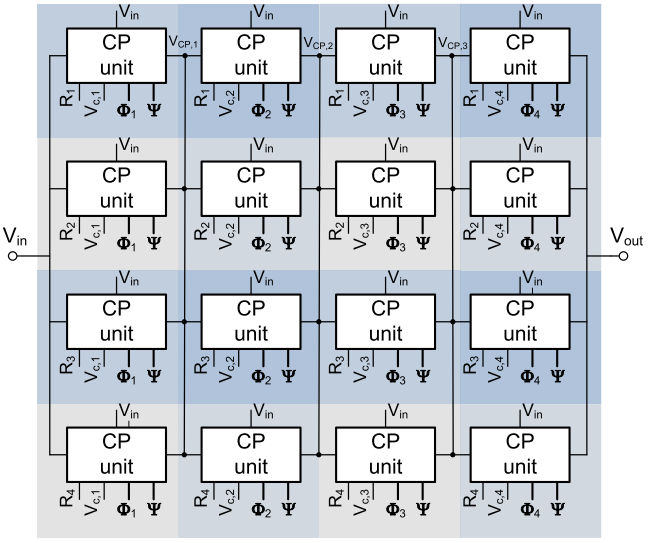


Fig. 3. Block diagram of the charge-pump array. Signals $V_{c,j}$ are voltage-shifted versions of C_j which are distributed per column in the array.

The architecture, components, and operation modes of the proposed DC–DC converter, described in Section 2, have been specifically designed to overcome these shortcomings. This is illustrated in Section 3, where experimental results are presented and discussed. The paper concludes with some remarks in Section 4.

2. System architecture and circuit design

Fig. 2 shows the proposed HV-regulated DC–DC converter. It consists of three main blocks: (1) an $M \times N$ array of charge-pumps (CP) driven by the input voltage V_{in}, (2) a Voltage-Controlled Oscillator (VCO) based feedback loop which regulates the output voltage of the CP array V_{out} against variations of the load current I_L by adjusting the pumping clock frequency clk, and (3) a programming interface for enabling/disabling rows or columns in the array and for generating a set of clock phases from clk. The output of the array is loaded with a 125 pF Metal-Oxide-Metal (MOM) capacitor C_{out} to attenuate voltage ripples. The feedback loop and the programming interface are supplied at $V_{DD} = 1.8V$. The logic high of the clocks driven the CP array, $\mathbf{\Phi}_j$ and $\mathbf{\Psi}$, and the row/column cell selection variables, $\mathbf{R}$ and $\mathbf{C}$, are boosted from V_{DD} to V_{in} by means of conventional level shifters based on differential cascode voltage switch logic [19].

2.1. Charge-pumps array and programming interface

In the proposed implementation, the array comprises 16 structurally identical CPs distributed in a 4 × 4 architecture ($M = 4$, $N = 4$), as shown in Fig. 3. The outputs of all the CPs in the same column are connected together. Active rows and columns are enabled using the $\mathbf{R} = \{R_i\}, i = 1,\ldots,4$, and $\mathbf{C} = \{C_j\}, j = 1,\ldots,4$, configuration bits, respectively (see Fig. 2). All possible row combinations, 16 in total, are possible. However, a column can only be activated if the previous one is enabled and, therefore, only 4 combinations are possible. Extensions for different numbers of rows, M, or columns, N, is straightforward, whenever the breakdown voltages of the CMOS process are not exceeded.

In the selected process, the parasitic pn-junctions of PMOS and DNW-NMOS transistors have breakdown voltages above 14 V, and transistors can withstand voltage differences of up to 3.3 V. Consequently, the number of columns in the presented design has been set to $M = 4$ and the maximum input voltage has been set to 3 V, to give some margin against transient spikes during switching.

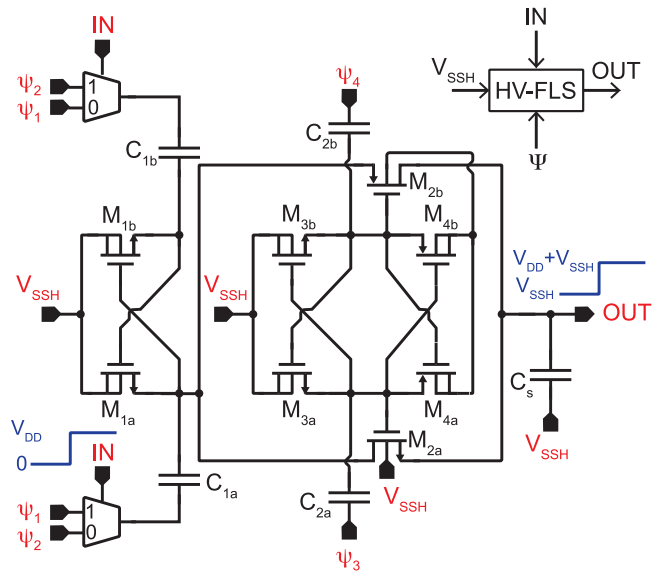


Fig. 4. Schematic and symbol of the floating level-shifter for sliding configuration bits.

The voltage levels of **R** and **C** have to be adjusted according to the cell position in the array. Namely, it has to be guaranteed that the transformed variables are comprised between the input $V_{CP,j-1}$, and the output, $V_{CP,j}$ of the cell (by construction, $V_{CP,0} = V_{in}$, i.e., the input voltage of the array). This is done by means of High-Voltage Floating Level Shifters (HV-FLS) [20,21]. The schematic and symbol of an HV-FLS are shown in Fig. 4. Assuming the control signal *IN* is comprised between ground and V_{DD}, the circuit generates a voltage-shifted version, OUT, which swings from V_{SSH} to $V_{DD} + V_{SSH}$. As capacitors $C_{1x} - C_{2x}$ (x stands for a or b) are periodically refreshed with $\mathbf{\Psi} = \{\psi_k\}, k = 1, \ldots, 4$, the circuit can tolerate non-periodical *IN* signals or variations of the shifting voltage, V_{SSH} – see [21] for more details. Fig. 5(a) shows the timing diagram of clock $\mathbf{\Psi}$, which is generated at the programming interface from the clk output of the regulation loop (see Fig. 2). Clock $\mathbf{\Psi}$ is made 8× slower than $\mathbf{\Phi}$ by means of a clock divider to save power consumption.

Fig. 6 shows the schematics of the CP core. It follows a cross-coupling architecture [22,23]. Besides the main charge pumping stage ($M_{1x} - M_{2x}$ and C_{1x}), it includes two auxiliary charge-pump circuits ($M_{3x} - M_{4x}$ and $C_{2x} - C_{3x}$) for boosting the conductivity of the core transistors; one HV-FLS integrated within the CP cell for level-shifting the selection bits R_i and C_j to $V_{cell,ij}$; and switches ($M_{5x} - M_{6x}$). The flying capacitors ($C_{1x} - C_{3x}$) nominally have a capacitance of $C_{fly} =$ 12.5 pF. They are implemented with a single metal–insulator–metal (MIM) structure in the cells located in the first and second columns of the array; however, the CPs in the third and fourth columns use two series-connected MIM capacitances to support higher voltages. Deep n-well NMOS transistors were employed in the CPs.

Fig. 7 shows the cascade circuit used for implementing the voltage-shifted column selection signals $V_{c,j}$ from the configuration bit $C_j, j = 1, \ldots, 4$. The circuit is implemented outside the CP array and, similar to the clocks in Fig. 5, a level shifter is placed at the output.

The clock signals $\mathbf{\Phi}_j = \{\phi_{j,k}\}, k = 1, \ldots, 4$ employed by the CPs are shared by columns. They are derived from the non-frequency-divided clock $\mathbf{\Phi}$ represented Fig. 5(a) using the circuit shown in Fig. 5(b). Note that the phases $\phi_{j,k}$ depend on the configuration bits C_j. Using the Delta blocks shown in Fig. 5(b), the phases $\phi_{j,k}$ are defined as:

$$\mathbf{\Phi}_j = \begin{cases} \{\phi_1, \phi_2, \phi_3, \phi_4\} & , C_j = 1 \\ \{0\ , 0\ , \phi_1, \phi_2\} & , C_j = 0 \end{cases} \tag{1}$$

Also note that because of the cascaded synthesis of the clocks $\mathbf{\Phi}_j, j = 1, \ldots, 4$, they are slightly time delayed each other, regardless of the C_j values. This avoids flying capacitors being charged at the same time, thus smoothing the current demand of the DC–DC converter [24].

Depending on whether the row and column of the CP cell are enabled or disabled, three different operation modes, denoted as PUMP, BYPASS, or DISABLED, can be defined. They are illustrated in Fig. 8 (only core transistors $M_{1x} - M_{2x}$ are shown for clarity).

- **PUMP**. In this mode (Fig. 8(a)), the row and column of the cell are enabled, $V_{cell,ij} = V_{CP,j-1}$ and $V_{c,j} = V_{CP,j-1}$. Hence, the cell operates as a cross-coupled CP in which core transistors ($M_{1x} - M_{2x}$) are switched on and off as illustrated in the figure, and switches ($M_{5x} - M_{6x}$) are off. The voltage $V_{pump,j}$ pumped to the following *j-th* column of the array is given by

$$\begin{aligned} V_{pump,j} &= V_{CP,j} - V_{CP,j-1} \\ &= V_{in} - \frac{I_L}{2M_a f_{clk} C_{fly}} \end{aligned} \tag{2}$$

  where C_{fly}, M_a, $V_{CP,i-1}$, V_{in}, f_{clk}, and I_L are, respectively, the value of the flying capacitor C_{1x}, the number of active rows, the cell's input voltage, the input voltage of the DC–DC converter, the pumping frequency, and the load current. Since the cells of the CP array are equally sized, the charge pumped from the input voltage source to the load is equally distributed among the flying capacitors, thus resulting in a constant pumping voltage, V_{pump}, across all cells. As V_{pump} decreases, the conduction resistance of M_{2x} increases, thus increasing the charge transfer time constant formed with the flying capacitors. When this time constant is comparable to the pumping clock period, the charge is not fully transferred to the next stage, and the output voltage cannot be properly regulated. In the proposed design, this performance limit is observable when $V_{pump,j}$ drops below roughly 1 V.
- **BYPASS**. In this mode (Fig. 8(b)), the row of the cell is enabled but the column is disabled. This is done by permanently setting M_{2x} on and by alternatively switching M_{1x} on and off. In this case, $V_{cell,ij} = V_{CP,j-1}$ and $V_{c,j} = V_{c,j-1}$. If the previous stage is in PUMP mode, $V_{c,j} = V_{CP,j-2}$, otherwise, if it is in BYPASS mode, $V_{c,j} = V_{c,j-2}$. Note that the flying capacitors are tied to the cell output node to reduce voltage ripples.
- **DISABLED**. In this mode (Fig. 8(c)), the row of the cell is disabled, and, regardless of the C_j value, the cell's input and output voltages are isolated, and flying capacitors contribute to reducing the ripple. In this case, $V_{cell,ij} = V_{CP,j-1} + V_{in}$, and if the column is enabled, $V_{c,j} = V_{CP,j-1}$, otherwise $V_{c,j} = V_{c,j-1}$.

Assuming a general $M \times N$ array architecture and neglecting conduction and switching losses in the CPs, the output voltage V_{out} of the DC–DC converter follows a saw-tooth waveform with period $T_h = T_{clk}/2$ given by

$$V_{out}(t) = V_0 - R_{eq} I_L + \left[1 - \left(\frac{t}{T_h} - \left\lfloor \frac{t}{T_h} - 1 \right\rfloor\right)\right] \frac{I_L}{C_{eq}} \tag{3}$$

where $\lfloor \cdot \rfloor$ represents the floor function, $V_0 = (N_a + 1)V_{in}$, N_a is the number of active columns in the array, and

$$R_{eq} = \frac{N_a}{2M_a f_{clk} C_{fly}} \tag{4}$$

$$C_{eq} = \left[2M(N - N_a + 1) - M_a\right] C_{fly} + C_{out} \tag{5}$$

Note that during the time interval $[0, T_h]$, $V_{out}(t)$ can be interpreted as the voltage drop across an equivalent $R_{eq} - C_{eq}$ series circuit, with the capacitor having an initial voltage V_0, which is discharged by a current load I_L. From (3), the average output voltage, $V_{out,avg}$, and the output ripple, ΔV_{out}, of the converter are, respectively, given by

$$V_{out,avg} = V_0 - \left(R_{eq} + \frac{1}{4 f_{clk} C_{eq}}\right) I_L \tag{6}$$

$$\Delta V_{out} = \frac{I_L}{2 f_{clk} C_{eq}} \tag{7}$$

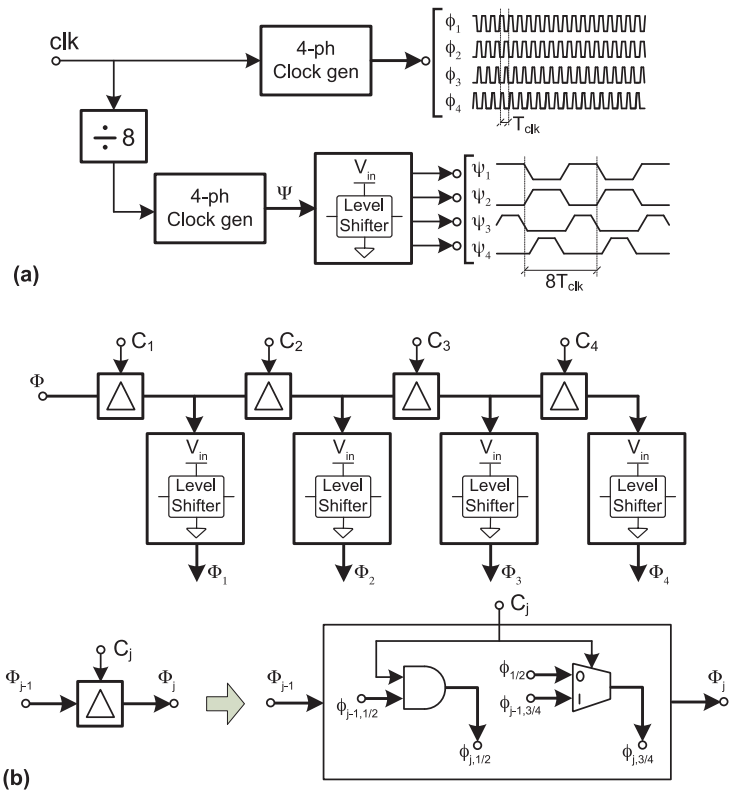


Fig. 5. Timing diagram of the 4-phase clock signals $\mathbf{\Phi}$, $\mathbf{\Phi}_j$ and $\mathbf{\Psi}$. All the circuit elements are supplied at V_{DD}, excepting the clock drivers that are biased at V_{in}.

For a given flying capacitance C_{fly} and output capacitor C_{out}, (6) shows that the voltage conversion ratio $VCR = V_{out}/V_{in}$ is mainly determined by N_a, however, it also depends on M_a and f_{clk}. Similarly, the output voltage ripple also depends on N_a, M_a and f_{clk}, according to (7). This reliance on multiple parameters is key to expanding the operating range of the DC–DC converter, as well as allowing different configurations for a given target. This is illustrated in Fig. 9 which shows the operation range segments (thick lines) for four different M_a and N_a combinations in the V_{pump} vs. $V_{out}(0)$ plane for an arbitrary case where $V_{in} = 3.0\,\text{V}$ and $I_L = 0.5\,\text{mA}$. The combinations are $M_a = N_a = \{1, 2, 3, 4\}$. From (2) and (3), the segments follow the expression

$$V_{pump} = \frac{V_{out}(0) - V_{in}}{N_a} \tag{8}$$

and the upper and bottom boundaries of each are obtained from (2) for the maximum and minimum values of the pumping clock frequency f_{clk} generated by the regulation loop. As mentioned, the lower boundaries cannot be decreased below approximately 1 V. Note from Fig. 9 that the segments cover different operation ranges, and there are output voltages that can only be accessed with one configuration. For instance, an output voltage of 4.3 V is only achievable if $M_a = N_a = 1$, as shown in the plot. It can also be observed that the segments overlap for given output voltages. For instance, an output voltage of $V_{out} = 11.3\,\text{V}$ can be generated both with $M_a = N_a = 3$ and $M_a = N_a = 4$. This paves the way to select one configuration or another for a target output voltage based on considerations like power efficiency or voltage ripple.

This is further illustrated in Fig. 10 which shows the accessible output voltage regions of the converter in terms of the load current and the number of activated rows $M_a = \{1, 2, 3, 4\}$, assuming $N_a = 4$ and $V_{in} = 3\,\text{V}$. The overlaps between the different regions are clearly observable and it can also be seen that some operation points are only accessible from a single configuration. For instance, $M_a = 1$ is the only possibility for generating a target output voltage $V(0) = 10.5\,\text{V}$ for load currents down to 0.1 mA. This illustrates the advantages that row programming offers for extending the operating range of the converter – a non-programmable $M_a = 4$ implementation would have required a load current of 0.5 mA for the same output voltage–.

The power losses of the array, not considered in (3), depend on the number of active cells and the $f_{clk}{\cdot}C_{fly}$ product as [25],

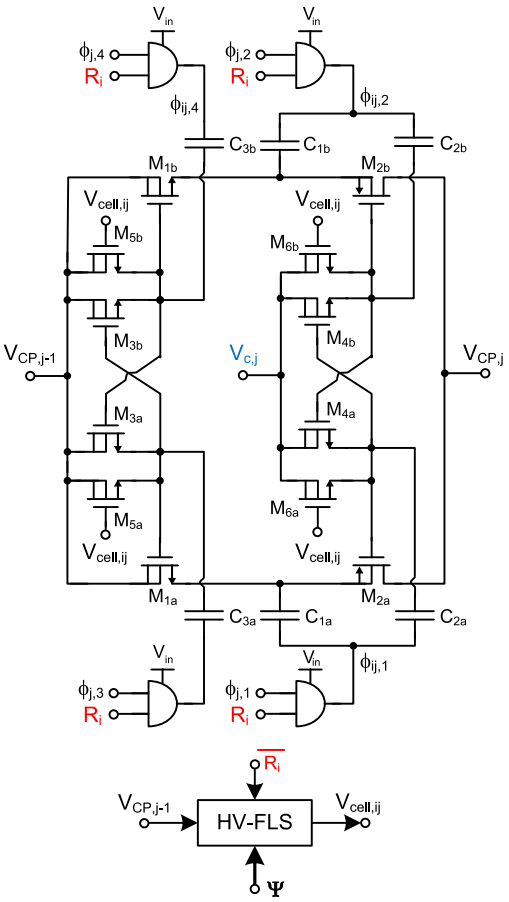
$$P_{loss,tot} = f_{clk}{\cdot}C_{fly}{\cdot}(2{\cdot}\beta{\cdot}V_{in}^2 + K_{inv}){\cdot}M_a{\cdot}N_a. \tag{9}$$

where the first sum term accounts for the switching losses due to the parasitic capacitances of the flying capacitors (they are estimated as a fraction β of the C_{fly} nominal value), and the second term represents the short-circuit losses of the flying capacitor drivers. This loss is modeled by the parameter K_{inv} which depends on circuit dimensions and increases with the square of the input voltage, V_{in}.

Eq. (9) reveals that power losses increase with the pumping frequency. However, from (4) and (7), the equivalent output resistance and the output voltage ripple are both inversely proportional to f_{clk}. Hence, there is a trade-off between power efficiency, achievable output voltage, and voltage ripple. A similar trade-off also holds if the number of active rows increases, i.e., power efficiency lowers but the converter output is smoother. Referring back to the graphical representation in Fig. 9, if a given target output voltage can be generated from two or more configurations, the one for which the operating point is closer to the lower limit of its feasibility segment gets a better energy efficiency. On the contrary, the configuration with an operating point closer to the upper limit obtains a better ripple behavior. These trade-offs will be further illustrated in Section 3.

2.2. Regulation circuit

It consists of a negative feedback loop that generates a clock signal that locks when the difference between a 1/10 scaled version of the DC–DC converter output and an internal voltage reference cancels out. Voltage scaling is implemented using a string of diode-connected PMOS transistors from the converter output to ground, and the voltage reference is obtained from a 4-b NMOS-based thermometer DAC. The



M_1	M_2	M_3	M_4	M_5	M_6	C_1	C_2	C_3
48	96	0.5	0.5	4	8	12.5	0.6	0.6

Fig. 6. Proposed cross-coupling charge-pump (CP) cell with enhanced conduction main transistors. The dimensions of the transistors and capacitors are given in μm and pF, respectively. All the transistors have a length of 0.35 μm.

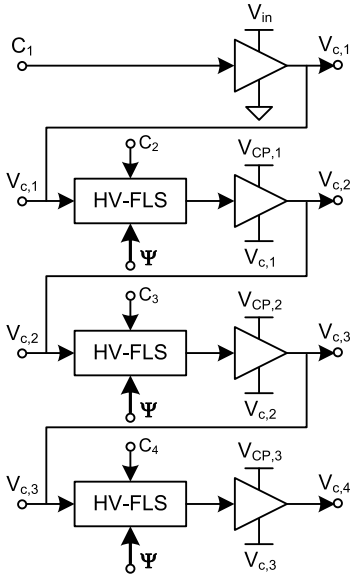


Fig. 7. HV-FLS based generation of voltage-shifted column selection signals $V_{c,j}$ from the configuration bit $C_j, j = 1, \ldots, 4$.

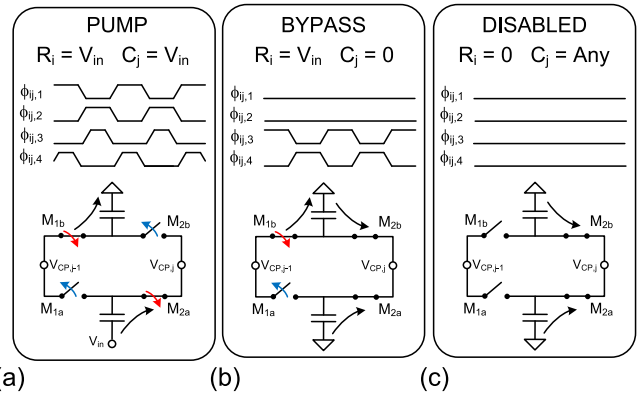


Fig. 8. Simplified schematic of the proposed CP cell in its different states: (a) PUMP, (b) BYPASS, (c) and DISABLED. Clock phases are also shown.

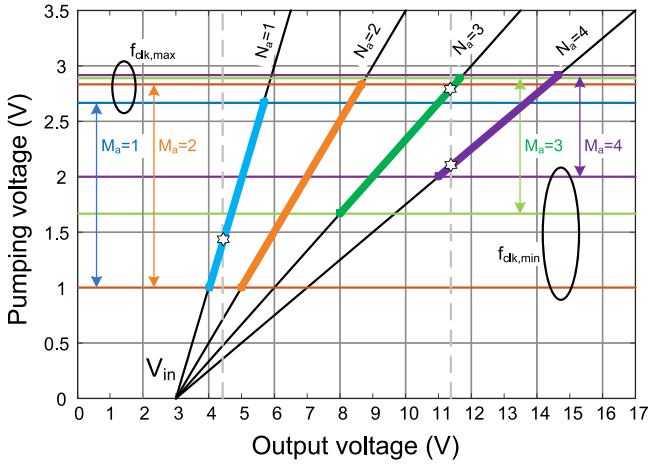


Fig. 9. Graphical representation of the converter operation range for different row/column configurations, assuming $I_L = 0.5\,\text{mA}$, $V_{in} = 3.0\,\text{V}$. Top (alt. bottom) horizontal colored lines represent the achievable pumping voltage at maximum (alt. minimum) f_{clk} for $M_a = 1, 2, 3, 4$. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

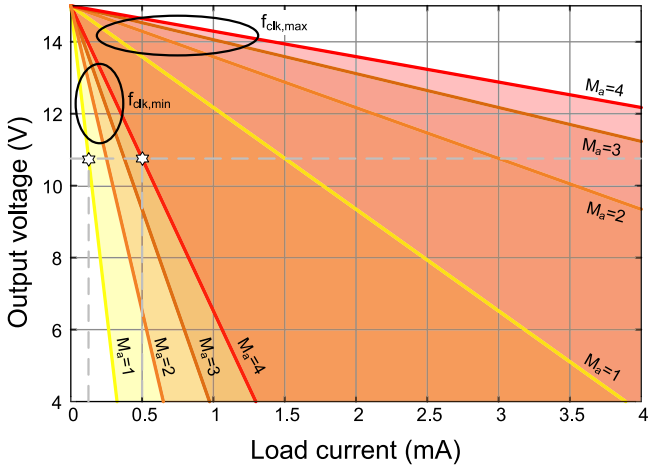


Fig. 10. Graphical representation of the converter operation range in terms of the load current and the number of activated rows for N_a=4, V_{in}=3 V.

DAC output is comprised within the range from 0.42 mV to 1.32 V at 60 mV steps, and can be selected using the input word V_{ref} (see Fig. 2). A resistor-less bandgap provides the DAC Ref. [26].

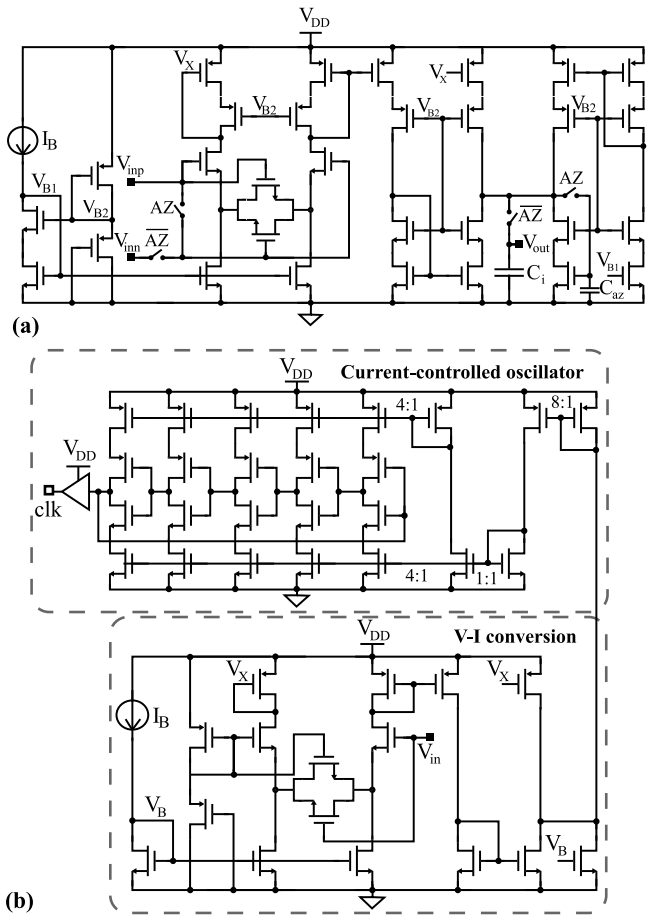


Fig. 11. Regulation loop circuit. (a) G_m-C integrator with a current auto-zeroing circuit for offset compensation. (b) VCO.

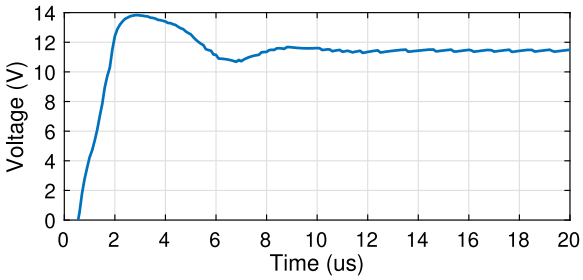


Fig. 12. Simulation of the startup of the DC–DC converter. The output settles at a 11.5 V output voltage in roughly 12 µs.

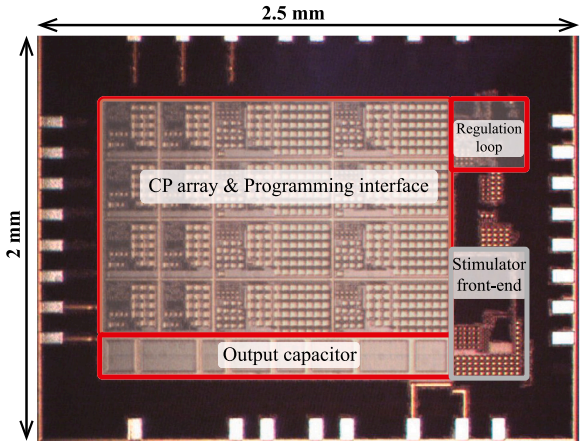


Fig. 13. Microphotograph of the fabricated chip. The DC–DC converter occupies an active area of 2.1 mm^2.

Additionally, the feedback loop comprises a G_m-C integrator, and a VCO. Both are powered at 1.8 V, and biasing currents are obtained from an integrated self-biased 25 nA current Ref. [27].

The G_m-C integrator is shown in Fig. 11(a). It consists of a single-ended current-mirror transconductor with input source-degeneration for enhancing linearity, and a 110 fF MIM integration capacitor, C_i. The integration time constant is about 160 µs. A current auto-zeroing circuit is used for offset-compensation [28]. During auto-zero (AZ = '1'), the feedback loop is opened, the inputs of the transconductor are shorted together to the DAC output, and the offset current is sampled in a 780 fF MIM capacitor, C_{az}. In this phase, which lasts 15 µs, the integration capacitor C_i is disconnected from the transconductor and drifts at a rate of roughly 2 mV/ms. This, however, has a negligible impact on the pumping frequency f_{clk} and, hence, on the converter output. When the transconductor is enabled (AZ = '0'), C_{az} is disconnected from the transconductor output, and the stored offset current is subtracted from the output current. Montecarlo simulations with PVT variations on extracted layout showed that the standard deviation of the transconductor input-referred offset decreased from 38.2 mV down to 61 µV through auto-zero. The storage capacitor C_{az} discharges during the hold phase (AZ = '0') at about 0.2 mV/m and has to be refreshed through auto-zeroing at a minimum frequency of 200 Hz to maintain the transconductor offset below 1 mV. This deviation carries a converter's output decrease of 10 mV, which is deemed acceptable for the intended application.

Fig. 11(b) shows the VCO. It uses a source-degenerated OTA for voltage-to-current conversion and a current-starved ring oscillator for current-to-frequency conversion. The negative input of the OTA is set to mid-rail, and the output current range is shifted from $[-I_{out,max},\ I_{out,max}]$ to $[0,\ 2{\cdot}I_{out,max}]$. In this range, the frequency of the VCO output, clk, approximately sweeps from 5 MHz up to 60 MHz.

The regulation loop allows a fast settling of the output voltage even at startup. Fig. 12 illustrates the operation of the DC–DC converter at startup for a target operating point with V_{out} = 11.5 V, I_L = 1 mA, M_a = 3, and N_a = 4. As can be seen, the desired output voltage is reached after about 12 µs.

3. Experimental results

Fig. 13 shows a micro-photograph of the proposed regulated DC–DC converter, fabricated in a standard 0.18 µm 1.8V/3.3 V CMOS process. The circuit occupies an active area of 2.1 mm^2 and can be programmed through an internal SPI module. No external components are needed.

Depending on the experiment, the load current is generated either with an off-chip voltage-controlled current source (for the static characterization of the circuit) or with the on-chip neural stimulator (for evaluating the dynamic behavior of the converter). The on-chip neural stimulator delivers current pulses with amplitudes up to 2 mA, pulse widths as low as 50 µs, and frequencies up to 1 kHz. In this case, a micro-controller is used for implementing a look-up table (LUT) which automatically maps the 128 combinations of the 16 target output voltages and 8 target load currents –0–2 mA range divided into 8 intervals– to the number of active rows and columns. This LUT was generated from the insights given by Fig. 9, Fig. 10, and (3). Given that the microcontroller also shapes the current stimulation pulses, the DC–DC converter can be precisely programmed to adapt the number of active rows and columns to the stimulation current.

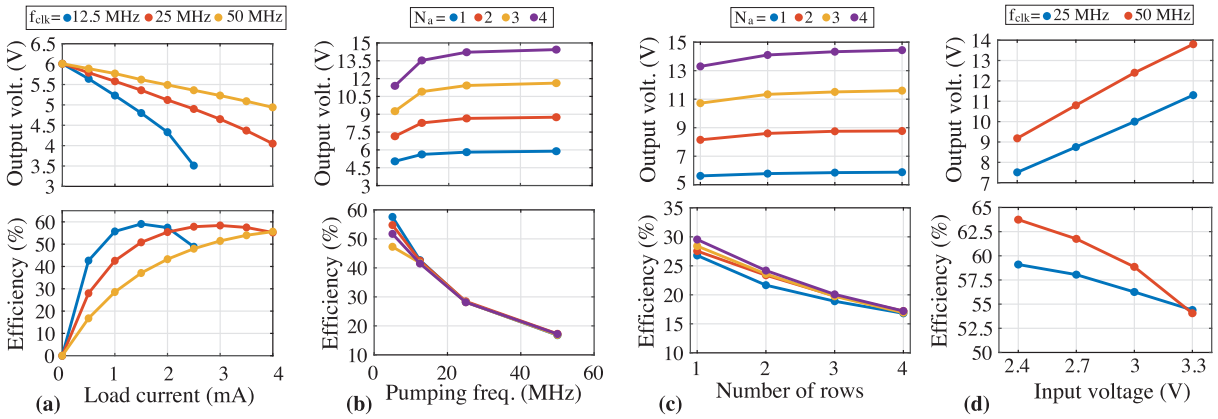


Fig. 14. Open loop measurements. Parameters: (a) $M_a = 4$, $N_a = 1$, $V_{in} = 3\,\text{V}$; (b) $M_a = 4$, $I_{load} = 0.5\,\text{mA}$, $V_{in} = 3\,\text{V}$; (c) $f_{clk} = 50\,\text{MHz}$, $I_{load} = 0.5\,\text{mA}$, $V_{in} = 3\,\text{V}$; and (d) $M_a = 4$, $N_a = 4$, $I_{load} = 3.5\,\text{mA}$.

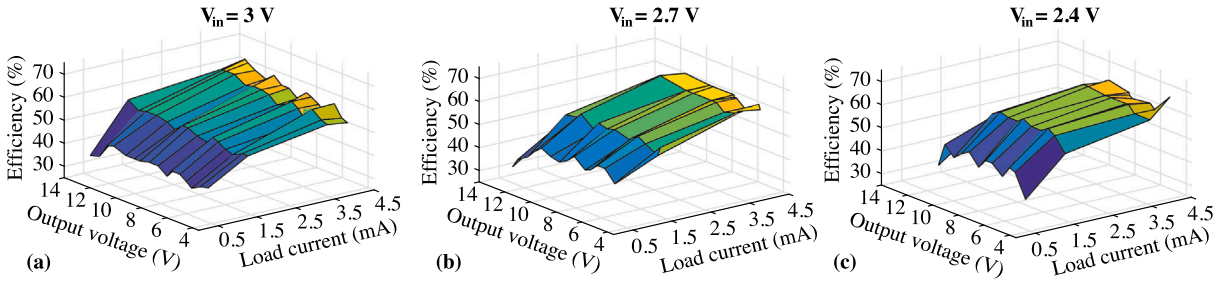


Fig. 15. Closed loop measurements. Power efficiency for (a) $V_{in} = 3.0\,\text{V}$, (b) $V_{in} = 2.7\,\text{V}$, and (c) $V_{in} = 2.4\,\text{V}$.

3.1. Open loop characterization

In this setup, the output of the regulation circuit is disconnected from the programming interface, the pumping clock clk is provided externally, and the average output voltage and efficiency of the DC–DC converter are measured under different conditions.

Fig. 14(a) shows the effect when the load current is swept from 0 to 4 mA for pumping frequencies of 12.5, 25, and 50 MHz. The number of activated rows and columns, M_a and N_a, are 4 and 1, respectively. As described in (6), the average output voltage decreases linearly with the load current, and the slope becomes steeper as the clock frequency decreases. Also, the load current for which the power efficiency is maximum increases with the clock frequency. Note that when the output voltage drops below roughly 4 V –i.e. the pumping voltage is below 1 V–, the charge is not fully transferred by the CP-cell and the output voltage exhibits a more pronounced decrease with the load current.

Fig. 14(b) illustrates the converter behavior when the pumping frequency f_{clk} is swept from 2.5 to 50 MHz for different numbers of activated columns N_a. In these plots, the number of activated rows is 4 and the load current I_L is 0.5 mA. Note that the output voltage tends asymptotically to V_0 as the pumping frequency increases, reaching 14.45 V for f_{clk}=50 MHz. Also, in agreement with (9), for a given load current, the power efficiency decreases with the pumping frequency from nearly 60% to 15%.

Fig. 14(c) shows the converter performance for different numbers of activated rows and columns, M_a and N_a. Load current and pumping frequency are 0.5 mA and 50 MHz, respectively. The output voltage increases with the number of activated rows as a result of the decrease in the equivalent output impedance of the DC–DC converter, as shown in (4). However, the power efficiency decreases due to the higher number of switching elements, as stated in (9).

Finally, Fig. 14(d) shows the output voltage and efficiency in terms of the input voltage. As shown in (6), the output voltage linearly increases with the input voltage; however, the measured efficiency decreases due to the increasing power losses, as stated in (9).

3.2. Closed loop characterization

In this setup, the pumping frequency of the CP array is internally controlled by the regulation loop; and the average output voltage, power efficiency, and output voltage ripple of the DC–DC converter are evaluated for all 16 possible values of V_{ref}. Measurements are repeated for every combination of load currents (assuming discrete values of 0.5, 1.5, 3.5, and 4 mA) and input voltages (assuming discrete values of 3.0, 2.7, and 2.4 V).

The surface plot of Fig. 15(a) illustrates the circuit behavior for a 3.0 V input voltage. Row/column configurations have been selected for improving power efficiency. The DC–DC converter can deliver output voltages from 4.2 V up to 13.2 V depending on the load current. For a 4 mA load, the output voltage is 12.1 V and the power efficiency is 65%. For loads larger than 1.5 mA, the efficiency is above 50%. At lower values, the efficiency decreases to 35%. Fig. 15(b) illustrates the case for $V_{in} = 2.7\,\text{V}$. The output voltage can be adjusted from 4.2 V up to 13 V and, hence, the VCR is comprised in the range 1.6–4.8 V/V. The peak power efficiency is 66%, obtained when the circuit delivers around 40 mW. Finally, Fig. 15(c) shows the operation for $V_{in} = 2.4\,\text{V}$. The DC–DC converter outputs voltages from 4.2 V up to 11.7 V, and the efficiency stays above 40% in most of the operation points, reaching a local maximum of 67%, when driving a 4 mA load current at 8.6 V.

Using the same setup, output voltage ripple, rather than power efficiency, is measured and the corresponding surface plots are shown in Fig. 16. In the case $V_{in} = 3.0\,\text{V}$, illustrated in Fig. 16(a), the peak voltage ripple is measured at 3.5 mA load current and 11.4 V output voltage, where a ratio $\Delta V_{out}/V_{out,avg}$ of 2.4% is obtained. In the case $V_{in} = 2.7\,\text{V}$, shown in Fig. 16(b), the peak ratio decreases to 1.4%, obtained at 4 mA load current and 10.4 V output voltage. Finally, when V_{in}=2.4 V (case shown in Fig. 16(c)), the peak $\Delta V_{out}/V_{out,avg}$ ratio

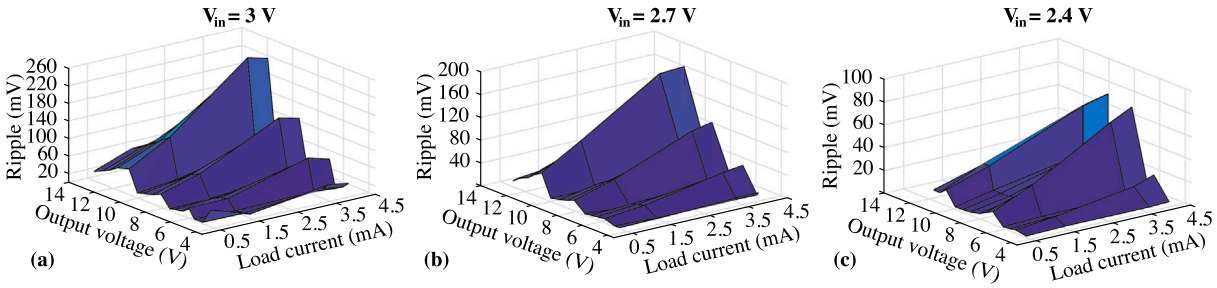


Fig. 16. Closed loop measurements. Output voltage ripple for (a) V_{in} = 3.0 V, (b) V_{in} = 2.7 V, and (c) V_{in} = 2.4 V.

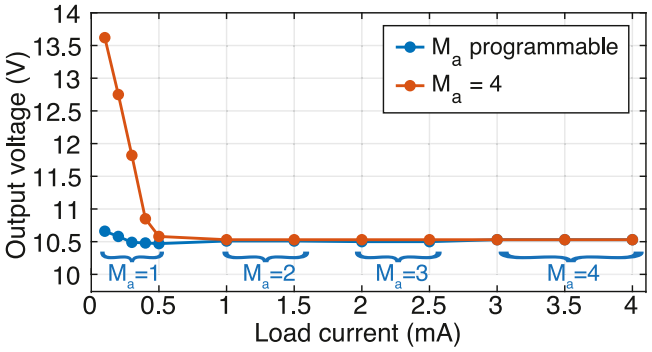


Fig. 17. Closed loop measurements. The orange line represents the output voltage for M_a=4. The blue line represents the output voltage when M_a is adapted to the load current. V_{in} = 3.0 V, V_{ref} = 1010, N_a = 4. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

further decreases to 0.9%, measured for V_{out}=8.6 V and I_L=4 mA. This decrease of the output voltage ripple with the input voltage can be explained through (2) and (7). Decreasing V_{in} increases the pumping clock frequency needed for reaching the target output voltage and, thus, ripples are smaller.

As discussed in Fig. 10, the programmability of the charge-pump array extends the low side of the load current operation range. This is experimentally confirmed in Fig. 17, which shows the output voltage, V_{out}, for different load currents ranging from 0.1 mA to 4 mA at V_{ref} ='1010'. The plot compares a case in which M_a = 4 to a case in which the number of activated rows is programmed according to the current load. Note that for currents below 0.5 mA the converter with M_a = 4 is not able to regulate the targeted output voltage and large deviations occur. Contrarily, when M_a is programmable, the circuit tolerates load currents as low as 0.1 mA with an average voltage deviation of 36 mV. This is in agreement with Fig. 10. Furthermore, as discussed in Section 2 and captured by (7), flying capacitors of disabled rows contribute to reducing the voltage ripple by increasing the equivalent capacitance, C_{eq}.

Fig. 18(a) illustrates the use of the DC–DC converter together with the on-chip neural stimulator. It shows the output voltage response to a load current I_L that switches from 0.2 mA to 2 mA at a rate of 1 kHz. During the transitions, the configuration of the CP array changes from M_a = 1, N_a = 4 (for the low current level), to M_a = 4, N_a = 3 (for the high current level). Note that despite the large load change and the structural reconfiguration of the array, V_{out} variations remain below 0.3 V. Additionally, it can be observed that the regulation loop successfully stabilized the output voltage after around 6 µs.

Finally, Fig. 18(b) shows the output voltage transient response to a change in the target output voltage, V_{ref} for a load current of 1.5 mA. Each 40 µs, the target voltage is changed from '0000' to '1111'. The output voltage can reach the target within 5 µs.

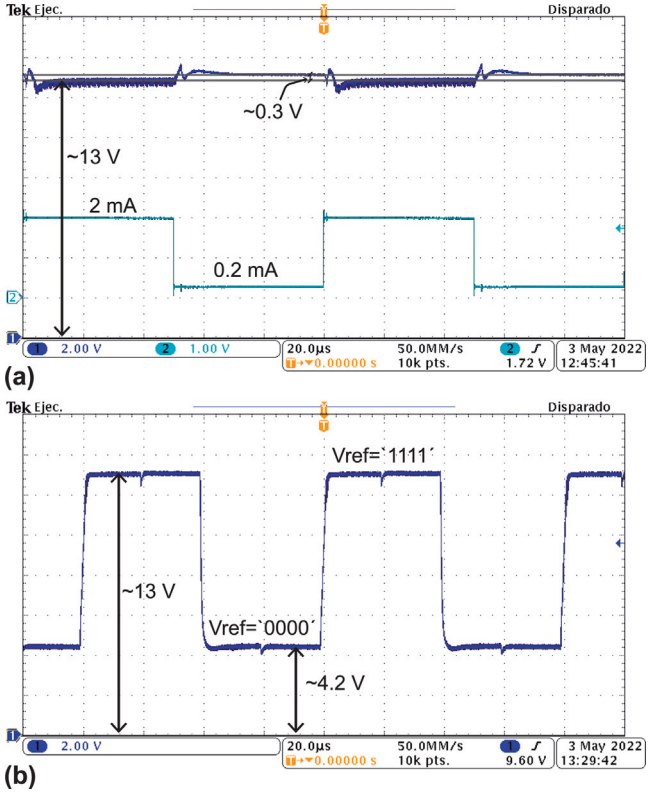


Fig. 18. (a) Response of V_{out} to a switching load current. (M_a, N_a) is set to (1, 4) under I_L=0.2 mA and to (4, 3) under I_L=2 mA. V_{in}=3 V, V_{ref}='1111'. (b) Response of V_{out} to a change in V_{ref}. (M_a, N_a) is set to (2, 1) for V_{ref}='0000' and to (2, 4) for V_{ref}='1111'. V_{in}=3 V, I_L=1.5 mA.

3.3. State-of-the-art comparison

Table 1 summarizes the performance of the proposed HV-regulated DC–DC converter, together with other solutions proposed in the literature. Only a few reported HV DC–DC converters implemented LV CMOS processes are fully implemented on-chip [9,15–17]. Compared to them, the proposed circuit obtains higher output power and the occupied area is smaller than the work achieving similar delivered power [16]. Our proposal works for input voltages $V_{in} \in [2.4, 3.0]$ V what makes it suitable to operate with WPT systems such as the one presented in [4]. Moreover, the efficiency when delivering maximum power is among the highest of the fully-on-chip solutions. Finally, the output voltage gets regulated under a wide range of load currents and the regulation loop is able to stabilize the output voltage within a few microseconds when the load current switches abruptly.

Table 1
Performance comparison with previously reported HV DC–DC boost converters in LV CMOS process.

	[14]	[15]	[17]	[16]	[18]	[9]	This work
CMOS Process	0.18 μm LV	0.35 μm LV	0.18 μm LV	0.18 μm LV	0.18 μm LV	65 nm LV	0.18 μm LV
V_{in}	1.8 V	2.5 V	3.3 V	3.3 V	2.8 V	0.5 V	**2.4-3 V**
V_{out}	1.7-11.4 V	7.5-16 V	5-19.6 V	3.3-12.6 V	12.8 V	11 V	**4.2-13.2 V** **4.2-13.0 V** **4.2-11.7 V**
Load current	0.1-1 mA	0.1-25 μA	Up to 150 μA	0.5-3.5 mA	0.01-2 mA	Up to mA	**0.1-4 mA**
Max. op. point	9.8 V@1 mA	11.5 V@25 μA	17 V@150 μA	10.8 V@3.5 mA	12.8 V@1 mA	11 V@2 mA	**12.1 V@4 mA** **10.2 V@4 mA** **8.6 V@4 mA**
Max. power (mW)	9.8	0.3	2.6	37.9	12.8	22	**48.4 (3.0 V)** **40.8 (2.7 V)** **34.4 (2.4 V)**
Efficiency at max. op. point	77%	32%	34%	60%	82%	31%	**65% (3.0 V)** **66% (2.7 V)** **67% (2.4 V)**
Area (mm^2)	–	0.07	0.06	2.87	–	0.04	**2.10**
Capacitors	1.2 μF	18 pF	26.4 pF	400 pF	9 μF	–	**400+125 pF**
Fully on-chip	No	Yes	Yes	Yes	No	Yes	Yes
Regulated	No	Yes	Yes	Yes	Yes	Yes	Yes

4. Conclusion

This paper reports a fully on-chip HV-regulated DC–DC converter for implanted neural stimulation applications, implemented in a standard 1.8V/3.3 V CMOS process. It can generate output voltages four times higher than the nominal process supply while keeping device terminal voltages below safe limits, thus ensuring long-term reliability. Furthermore, the converter can tolerate a wide range of output current loads, from 0.1 mA up to 4 mA, making it suitable for quite diverse stimulation scenarios, both in rodents and mammals.

The circuit features an array of individually configurable charge-pumps which maximize its power efficiency, up to approximately 65% with V_{in}=3 V, as the load current increases, thus allowing to relax the power demand of the neuromodulator when more current consumption is needed, i.e., during the stimulation cycles. This is particularly relevant if the implanted device is supplied with wireless powering techniques. Additionally, the on-chip regulation loop allows fast recovery of the converter output under abrupt changes in the load current.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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