Novel Pipeline Architectures based on Negative Differential Resistance Devices

Juan Núñez , María J. Avedillo and José M. Quintana

Instituto de Microelectrónica de Sevilla (IMSE-CNM-CSIC) & Universidad de Sevilla
Av. Américo Vespucio s/n, 41092, Sevilla (Spain)
{jnunez, avedillo, josem} @ imse-cnm.csic.es

Abstract. Devices exhibiting Negative Differential Resistance (NDR) in their *I-V* characteristic are attractive from the design point of view and circuits exploiting it have been reported showing advantages in terms of performance and/or cost. In particular, logic circuits based on the Monostable to Bistable (MOBILE) operating principle can be built from the operation of two series connected NDR devices with a clocked bias. MOBILE gates allow compact implementation of complex logic function like threshold gates and are very suitable for the implementation of latch-free fine grained pipelines. This pipelining relies on the self-latching feature of MOBILE operation. Conventionally MOBILE gates are operated in a gate level pipelined fashion using a four-phase overlapped clock scheme. However other simpler, and higher through-output interconnection schemes are possible. This paper describes latch-free MOBILE pipeline architectures with a single clock and with a two phase clock scheme which strongly rely on distinctive characteristics of the MOBILE operating principle. Both proposed architectures are analyzed and experimentally validated. The fabricated circuits use a well-known transistor NDR circuit (MOS-NDR) and an efficient MOBILE gate topology built on its basis. Both solutions are compared and their distinctive characteristics with respect to domino based solutions are pointed out.
Keywords: Negative differential Resistance (NDR), Fine-grain pipeline, Monostable to Bistable Logic Elements (MOBILE), MOS-NDR.

1 Introduction

Different emerging devices like Resonant Tunneling Diodes (RTDs), tunnel transistors or molecular RTD devices exhibit Negative Differential Resistance (NDR) in their *I-V* characteristic. Many circuits taking advantage of it have been reported covering different applications and with different goals, including high speed, low power or reduced device count [1], [2], [3], so that design techniques exploiting this feature at different levels (circuit, architecture, …) are currently an area of active research. Moreover, exploration of transistor circuits that emulate the NDR characteristic has recently received renewed attention in order to incorporate the benefits of NDR based circuits into transistor technologies [4]-[10].

From the point of view of design, the NDR characteristic is very attractive. On one hand, it can be exploited in non-linear circuits like oscillators or frequency dividers. On the other, it is useful in the implementation of memories due to the existence of

stable states associated to the inclusion of NDR elements. In particular, the Goto pair is well known [11]. The circuit consists of two NDR devices connected in series leading to three operating points, two stable and one unstable. The two stable points can be used to represent and store data. On the basis of the Goto pair, logic circuits which operation is based on a Monostable to a Bistable transition (MOBILE) have been developed. MOBILE gates are implemented operating two series connected NDR devices with a switching bias. There is a pair of interesting characteristics of MOBILEs in comparison to conventional logic gate implementations.

First, they increase the functionality implemented by a single gate in comparison to MOS and bipolar technologies and, thus, reducing circuit complexity. In particular, the operating principle of MOBILE is extremely well suited to implement the arithmetic operation on which Threshold Gates (TGs) are based [12]. Different topologies for MOBILE TGs and Multi-Threshold Threshold gates have been reported and experimentally validated [13], [14].

Second, the self-latching property of MOBILEs arising from their NDR characteristic allows the implementation of fine grain pipelines which can be achieved without resorting to memory elements [1], [15]. In this way, exploration of interconnection schemes for MOBILE gates is relevant for the design of functional units for high performance applications, which is currently an area of active research.

Originally, it was proposed to operate MOBILE gates in a gate level pipelined fashion using a four-phase overlapped clock scheme. Conventional counterpart of this super-pipelining is the operation of Domino logic in a pipelined fashion using an overlapping multi-phase clock scheme and without latches between consecutive clock phases [16]. Variations of this multi-phase domino solution (three to six phases) have been developed by different companies and applied into commercial circuits [17], [18]. However, MOBILE pipelines do not exhibit the functional limitation of domino solutions, and thus, both inverting and non-inverting blocks can be chained.

The overcoming of the functional limitation is not the only advantage of the MOBILE architectures, but their edge-triggered feature allows the implementation of other distinctive interconnection schemes. In particular, this characteristic can be exploited to reduce the number of clock-phases, which is attractive both from the point of view of increasing through-output, and for simplifying clock distribution.

This paper describes latch-free MOBILE pipeline architectures with a single clock and with a two phase clock scheme which strongly rely on distinctive characteristics of the MOBILE operating principle.

The paper is organized as follows: in Section 2, MOBILE logic style is described. Section 3 presents the MOS-NDR device and the implementation of MOBILE logic gates on its basis. In Section 4 and 5, we describe and analyze the single phase and the two-phase MOBILE pipelines respectively. Section 6 shows experimental results validating their operation and compares both approaches. Finally, some key conclusions are given in Section 7.

2 MOBILE operation principle

2.1 MOBILE logic gates

The MOBILE [12] in Fig. 1a is an edge-triggered current controlled gate which consists of two devices exhibiting NDR in their *I-V* characteristic (Fig. 1b), connected in series and driven by a switching bias voltage, V_{CK}. When V_{CK} is low, both NDRs are in the on-state and the circuit is monostable. Increasing V_{CK} to an appropriate maximum value ensures that only the device with the lowest peak current switches from the on-state to the off-state. Output is high if the driver NDR switches and it is low if the load does. Logic functionality can be achieved if the peak current (I_P in Fig. 1b) of one of the NDR devices is controlled by an input. In the configuration of the rising edge-triggered inverter MOBILE shown in Fig. 1c, the peak current of the driver NDR can be modulated using the external input signal V_{in}. Transistor behaves like a switch, so that for a low input, current flows only through NDR_D, but for a high input, the effective peak current of the driver is the sum of the peak currents of NDR_D and NDR_X. More complex logic functionality can be implemented in two different ways. Clearly, replacing the single transistor in Fig. 1c by an NMOS transistor network, other logic functions are implemented. NDR peak currents are selected such that the value of the output depends on whether the network transistor evaluates to "1" or to "0". Alternatively, topologies for implementing threshold functions[1] [19] have been proposed. The inverter shown in Fig. 1c can be also explained as a threshold gate, with a single input with associated weight $w_1 = -1$ and threshold $T = 0$. Adding input branches (NDR device plus transistor) in parallel to the driver (load) NDR inputs with negative (positive weights) are implemented. That is, the weighted sum and the comparison to a threshold value which defines the operation of a threshold gate is realized by means of the current controlled switching principle of the MOBILE.
Figure 1d depicts a falling edge triggered inverter. Note that branch implementing functionality is now in parallel to the load NDR and uses a p-type transistor.

It is well known that a sufficiently slow V_{CK} rising (or falling) is required for MOBILE operation [20]. That is, there is a critical rise time for the switching bias below which the gate does not operate correctly. Under that critical rise time, there is at least one input combination for which the gate does not produce the expected logic output. It is due to AC currents associated to internal parasitics and output capacitive loads (fan-out), which are more important for faster clock changes, that somewhat "alter" the ideal MOBILE operating principle based on peak currents comparison. This critical value depends on both circuit (NDR peak currents, fan-out …) and technological parameters. That is, design requires taking into account this AC currents in

[1] A threshold gate (TG) is defined as a logic gate with n binary input variables, x_i (i=1, . . . , n), one binary output y, and for which there is a set of (n +1) real numbers: threshold T and weights w_1, w_2, . . . , w_n, such that its input–output relationship is defined as y=1 iff $\sum_{i=1}^{n} w_i x_i \geq T$ and y=0 otherwise. Sum and product are the conventional, rather than the logical, operations.

order to guarantee the desired relationship between load and driver currents for each input combination when V_{CK} approaches $2V_p$, being V_p the peak voltage of the NDRs (see Fig. 1b).
Rising (falling) edge-triggered MOBILE logic gates evaluate the inputs with the rising (falling) edge of the bias voltage and hold the logic level of the output while the bias voltage is high (low), even though the inputs change (self-latching operation [21]). The output returns to zero (to one) with the falling (rising) edge of the clock until the next evaluation. The self-latching operation allows the implementation of gate-level pipelined architectures without extra memory elements [1] and without the functional limitation of dynamic based solutions like the widely used domino logic style.

2.2 Interconnecting MOBILE gates

As it was stated in previous section, and assuming rising-edge MOBILEs, there are four steps in the operation of each gate: evaluation (clock rises), hold (clock high), reset (clock falls) and wait (clock low). Gate-level pipelining is possible if each MOBILE gate evaluates while those driving it are in the hold state. In this way, it is guaranteed that inputs to each gate are stable during evaluation, and that the reset of the MOBILE gates do not affect those they drive, since they have already evaluated when it happens. Thus, memory elements are not required. Note that this is true both for inverting and non-inverting MOBILE stages, and even when adding and output stage (static inverter or buffer) to the output of the MOBILE blocks to ease management of fan-out and interconnections. That is, fulfilling above stated constraint allows ultra-fine-grain pipeline operation where both inverting and non-inverting stages are allowed. In domino solutions only non-inverting stages are possible which complicates logic design (inverters need to be pushed towards the inputs or some parts of the circuits are duplicated), unless a double rail implementation is used which almost duplicates device count.
Conventionally, and because of the four steps in MOBILE operation, cascaded rising edge-triggered MOBILE gates are operated in a pipelined fashion using a four-phase overlapping clock scheme shown in Fig. 2 [1]. $V_{CK,\,i}$ is delayed with respect to $V_{CK,\,i-1}$ by $T/4$, being T the clock period. Thus, the i^{th} stage evaluates (rising edge of $V_{CK,\,i}$) while the $(i\text{-}1)^{\text{th}}$ stage is in the hold phase ($V_{CK,\,i\text{-}1}$ high). Four clock signals are enough, since the first phase can be used for the fifth level and so on. In previous section, it was stated that there is a critical rise time below which the gate does not operate correctly. This explains the clock shape with equal rise, high, fall and low times. Thus, for this scheme four gates/stages serially evaluate in one clock period.
However other schemes are compatible with the constraint that one stage evaluates while preceding stages are in hold state. Moreover, the constraint can be somewhat relaxed making possible other simpler schemes. Sections 4 and 5 describe two novel architectures developed on the basis of previous statement.

3 MOS-NDR MOBILE Logic

NDR *I-V* characteristics derived from a Λ type NDR topology described in [22], can be emulated with CMOS transistors using the MOS-NDR device shown in Fig. 3a [6]. It consists of two NMOS and one PMOS transistors, which leads to an *I-V* curve with only one positive differential resistance region (PDR), as shown in Fig. 3b. Both the PDR and the NDR zones of the NDR *I-V* characteristic are obtained through the current of a NMOS transistor (N_1) whose gate-to-source voltage is modulated by the output voltage of the CMOS inverter biased by V_{DD}. For low values of V N_1 is working in lineal region (generates PDR region of the *I-V* curve), until the output of the inverter falls and, thus, N_1 cuts off.

The peak voltage (V_P) and current (I_P) can be modified by properly setting up the sizes of the transistor. In this way, I_P is increased with the width of N_1. Assuming that all transistors have the same gate length, the position of V_P is controlled by the ratio between the widths of the NMOS and the PMOS transistors of the inverter. In this way, higher values of V_P are obtained by decreasing such ratio.

Implementations of MOS-NDR MOBILE gates have been reported [10], [28], [6] leading to compact implementations of complex functions. Figure 3c depicts a MOBILE inverter designed using such CMOS emulator, in which each NDR device have been replaced by a MOS-NDR device. Driver NDR includes logic functionality, which has been implemented by adding two series-connected NMOS transistors: the one of the top represents the weight of the input branch and the other operates as a switch which is enabled by the input. Complex functions can be efficiently implemented by adding input branches in parallel (either with the driver or the load) [6].

Self-latching operation of MOBILE gates implemented with MOS-NDR devices is also observed. Figure 3d shows simulation waveforms corresponding to the MOBILE inverter in Fig. 3c, where it can be inferred that changes of the input when the clock is in hold state do not trigger variations of the output.

4 Single Phase MOBILE architectures

A network of MOBILE-based gates can be operated with a single clocked bias signal if rising edge-triggered gates and falling edge-triggered gates are alternated and latches are added at each stage to remove the return-to-reset behavior [23]. However, it has been demonstrated that it is not necessary to remove the return-to-reset behavior to ensure correct operation [24]. It is enough to keep the output of each MOBILE stage until it has been evaluated by the next one. Thus, each latch is replaced by a static inverter/buffer. However, in these architectures, negative edge-triggered MOBILE are used which requires p-type transistors. This translates in larger transistors, and so in larger parasitic capacitances which degrade gate speed. The proposed single phase architecture is built from rising-edge MOBILE gates driven by a single clock signal, and skewed static stages between MOBILE blocks. Figure 4a depicts a block diagram of the proposed architecture. Its correct operation requires satisfying a set of relationships among given timing parameters of its components.

That is, for the proposed interconnection scheme to work, different timing constraints must be satisfied. For the purpose of deriving them, lets us introduce the following parameters:

$t_{MOBILE\_Eval\_1}$: *MOBILE evaluation time of a logic 1*

$t_{MOBILE\_Eval\_0}$: *MOBILE evaluation time of a logic 0*

t_{MOBILE_Reset}: *Reset time of the MOBILE stage*

t_{Static_1}: *Propagation delay through the static logic of a low to high transition*

t_{Static_0}: *Propagation delay through the static logic of a high to low transition*

t_{Stet_up}: *Amount of time that MOBILE input must be stable before the clock rising edge*

t_{Hold}: *Amount of time that MOBILE input must be stable after the clock rising edge*

T: *Clock period*

T_H: *Clock pulse width*

Following three types of constraints must be fulfilled by each pair of consecutive stages.

1.- It must be guaranteed that signals do not propagate too slow. That is, in one clock period the MOBILE stage evaluates, and the static logic propagates its output in time for the next stage to correctly evaluate. Formally:

$$t_{MOBILE\_Eval\_0} + t_{Static\_1} + t_{Set\_up} < T \quad (1)$$

$$t_{MOBILE\_Eval\_1} + t_{Static\_0} + t_{Set\_up} < T \quad (2a)$$

Relation (2a) can be relaxed taking into account that $t_{MOBILE\_Eval\_1}$ is zero, since the output of the MOBILE was already zero due to the previous reset phase. Moreover, as it was already zero, it means static logic has more than T to propagate a 0, and so, it can be rewritten:

$$t_{Static\_0} + t_{Set\_up} < 2T - T_H - t_{MOBILE\_Reset} \quad (2b)$$

2.- It must be guaranteed that signals do not propagate too fast. That is, a pipeline stage (MOBILE block + static logic) does not propagate to its output the result of an evaluation associated to a given clock edge before the MOBILE blocks it drives have taken the decision corresponding to that clock edge. Formally:

$$t_{MOBILE\_Eval\_0} + t_{Static\_1} > t_{Hold} \quad (3)$$

$$t_{MOBILE\_Eval\_1} + t_{Static\_0} > t_{Hold} \quad (4a)$$

which as in previous case, taken into account the previous reset of the MOBILE stage can be rewritten:

$$t_{Static\_0} > T - T_H + t_{Hold} - t_{MOBILE\_Reset} \quad (4b)$$

3.- Due to the reset behaviour of MOBILE gates, it must be guaranteed also that the reset of the MOBILE, produced by the falling edge of the clock, does not

reaches the output of the static logic in time to be evaluated by following stage with next rising clock edge. Formally:

$$t_{MOBILE\_\mathrm{Re}set} + t_{Static\_0} > T - T_H + t_{Hold} \quad (5)$$

Note that constraint 5 is equal to constraint 4b. This is so because when deriving hold constraint, relation 4 was rewritten taken into account the reset behaviour of the MOBILE gates.

In addition, every MOBILE block must have enough time to reset. This limits the duration of the clock pulse width (T_H), since reset occurs with the falling edge and should be completed before rising edge, which means available time is $T - T_H$.

Note that t_{Hold} and t_{set_up} are small because MOBILE gates evaluate with the rising clock edge.

Static logic must be designed such that it propagates inputs slow enough not to reach next MOBILE too early (constraint 3 and constraint 4b), but not too slow to reach next MOBILE too late (constraint 1 and constraint 2b). According to derived timing relationships, the static logic is designed in order to slow down the low to high output transition with respect to the opposite one in order to full-fill with constraints 4b and 5, and also because upper limit of the low-to-high transition is more relaxed than for the later (constraint 2b versus constraint 1). Nevertheless, detailed electrical simulation is required and equations above must not be considered a design tool at the logic level, but a mean to introduce timing aspects of the proposed architecture.

Clearly this architecture works on the basic of the intrinsic self-latching characteristic of MOBILE blocks. A similar one based on domino stages is not possible because evaluation is carried out in this case when the clock is high, instead of being associated to the clock transition.

One of the main advantages of this architecture is that a single clock is distributed. However there are some other design challenges that require some explanation. First, these circuits exhibit a minimum operating frequency due to constraints 4b and a maximum operating frequency, that can be determined by any of the other constraints when considering very fine-grain pipeline which is our target. The limit situation of pipeline is a single inverter between consecutive stages, in the sense that more complex static logic (a gate with embedded functionality or several logic levels) could help in relaxing lower bounds on delays which complicates design.

For our current purpose of explaining the interconnection challenges, a given MOBILE inverter is considered and the impact of the static inverter on circuit operation is analyzed. From our experience, if the inverter is too much skewed, operation is going to be limited by hold failures (constraint 3) and maximum frequency is reduced from what it could be achieved according to constraints 1 and 2b, leading to a much reduced range of operating frequencies, that might be even unable to tolerate variations of process parameters.

Figure 4b shows simulations results of a chain of MOBILE inverters with skewed static inverters between them, corresponding to a W_P/L_P to W_N/L_N ratio of the static inverters equal to 35 at a frequency slightly over its maximum operating frequency (1.6GHz). It can be observed that the output of the first stage, $V_{\mathrm{OUT},1}$, is correct. Alternating 0`s and 1`s are obtained as expected for the applied input, V_{IN}. This means the MOBILE is able to operate at this speed and with this clock transition times. It can be observed also that low to high transitions of $V_{\mathrm{OUT},1x}$ are very slow and high to low

transitions are very fast. The second MOBILE stage does not work. It correctly evaluates the 0`s of the first stage's output, but it fails to produce a correct output for 1's. Note the intermediate voltage level at the output $V_{OUT,2}$ which translates in functional failure as it can be seen comparing input V_{IN} and output V_{OUT}. The problem arises from the very fast high to low transition of $V_{OUT1,X}$, simultaneous to the rising edge of node V_{CK} which acts as the clock for the MOBILE core of the cell, which produces a "hold violation". Correct operation is observed, for example, for a W_P/L_P to W_N/L_N ratio equal to 14 now at a higher frequency (2.1GHz). Process and operation parameter variations can modify the range of operating frequencies. Corner and Monte Carlo simulations of the second design have been also carried out showing correct behaviour.
Second concern for fine grained pipelines is related to clock skew tolerance due to the fact that all stages evaluate with the same clock edge.

5 Two-Phase MOBILE architectures

An alternative solution to avoid drawbacks found in single-phase interconnection schemes is to use an overlapping two-phase clock [25] scheme as shown in Fig. 5a and 5b. In this configuration each gate evaluates while preceding one is in the hold state and, only two stages serially evaluate in one clock period. Note that inter-gate elements (inverting or not inverting) can also be added if required by logical (to increase design flexibility), or electrical (for example, efficient handling of large loads) considerations. Unlike the single phase architecture, the overlapping of the two clocks allows to directly connect two MOBILE gates since the return to reset of one stage takes place after the evaluation of the next one.
A timing analysis, as in the case of the single phase, is also carried out. For each pair of consecutive stages:

1.- It must be guaranteed that signals do not propagate too slow. That is, in half clock period, the MOBILE stage evaluates, and the static logic, if it exists, propagates its output in time for the next stage to correctly evaluate. Formally:

$$t_{MOBILE\_Eval\_0} + t_{Static\_eval\_1} + t_{Set\_up} < T/2 \quad (6)$$

$$t_{MOBILE\_Eval\_1} + t_{Static\_eval\_0} + t_{Set\_up} < T/2 \quad (7a)$$

Again relation (7a) can be relaxed taking into account that $t_{MOBILE\_Eval\_1}$ is zero, since the output of the MOBILE was already zero due to the previous reset phase. Moreover, as it was already zero, it means static logic has more than T to propagate a 0, and so, it can be rewritten:

$$t_{Static\_eval\_0} + t_{Set\_up} < 3T/2 - T_H - t_{MOBILE\_Reset} \quad (7b)$$

2.- Note that there are not conventional hold constraints in this scheme since consecutive stages do not evaluate with same clock edge.
3.- Constraint related to the reset of the MOBILE stage not being "seen" by following stage is also quite relaxed because the two clock phases overlap. It must be only guaranteed that the reset of the MOBILE does not reaches the output of

the static logic before the hold time of following stage expires. Formally and calling $t_{overlap}$ the time amount by which the two phases overlap:

$$T_{MOBILE\_\text{Re}set} + t_{Static\_0} + t_{overlap} > t_{Hold} \quad (8a)$$

which can be written:

$$T_{MOBILE\_\text{Re}set} + t_{Static\_0} + T_H - T/2 > t_{Hold} \quad (8b)$$

Moreover, every MOBILE block must have enough time to reset. This limits the width of the clock pulse (T_H), as previously discussed and so this translates in an upper limit for the overlapping of the two clock phases.

A comparison to Domino-based counterparts is also interesting. As we mentioned in the introduction, multi-phase overlapped clock domino have been widely applied in high speed applications, but usually with more than two phases. When only two phases are used, evaluation could slip over consecutive stages if overlap is too long (race-through failure) complicating design and motivating that in many cases latches are introduced [26][27].

The operation of the two-phase chain of inverters of Fig. 5a, working at 2GHz, is shown in Fig. 5c. Design challenge in this interconnection scheme is a proper choice of the overlap time between both clock signals. Due to the edge-triggered nature of MOBILE evaluations, required minimum overlap is in general small, especially when static stages are used between MOBILE blocks. This is so because, as it was anticipated, the interconnection constraint can be relaxed. Correct operation is achieved if current stage takes a decision before it sees the reset of the previous stage. That is, before the output of the preceding MOBILE blocks reaches a low level output voltage and it propagates through the inter-MOBILEs elements. Indeed, Fig. 5c shows that each rising edge of $V_{CK,2}$ (dashed line) comes before $V_{out1,x}$ goes to reset. On the other hand, the maximum overlap is only limited by the maximum allowable duty cycle of the clock, which is determined by the minimum time required for the reset of the MOBILE gates.

6 Experimental results and discussion

The operation of the proposed single-phase and the two-phase clock schemes has been experimentally validated. Ten-stage chains of MOBILE inverters have been designed and fabricated in a 1.2V/90nm CMOS commercial process. In the single phase architecture, skewed static inverters are used between consecutive MOBILE blocks. That is, the logic diagram of the fabricated circuit corresponds to the one in Fig. 4a. In the two-phase architecture, MOBILEs are directly connected without static logic. The circuits also include clock circuitry to avoid power clocks. That is, the clocked bias (clock) required by the MOBILE gates is generated internally from de external clock which drives an input buffer. In addition, the two overlapped phases required for one of the architectures are also generated on chip from a single external clock.

The test has been carried out on the packaged circuit. Waveforms have been captured using the oscilloscope Agilent DSO6104A and pulse generator HP81134A for the clock and the input.
Several tests have been programmed in order to fully verify the fabricated chains. First, constant inputs (both '0' and '1') have been applied to the chains in order to rule out that the operation is not limited by the MOBILE gates. Correct operation is obtained for both architectures up to 1.5GHz. Over this frequency, the experimental set-up attenuates signals too much despite of using low capacitance probes which minimize the effect of the experimental set-up on them. The second experiment consists of using an input with a frequency equal to the half of the frequency of the clock (similar to the one shown in Fig. 3c), which corresponds to an alternating sequence of zeros and ones. This input is the most unfavorable case.
Figure 6 shows experimental results for the single-phase architecture. Figure 6a depicts waveforms when the sequence alternating 0's and 1's is applied to the ten-stage pipeline. V_{CK} and V_{IN} are 1.2V pulse trains at 1.1GHz and 550MHz, respectively. As expected, V_{OUT} is a periodical signal of the same frequency of the input. That is, the 0101…01 sequence is obtained at the output of the pipeline. Note the different shapes of V_{IN} and V_{OUT} which is due to the return to zero behavior of MOBILE. Results are shown at 1.1GHz and so signals are attenuated by the experimental set-up. Measured results for an input frequency of the eight part of the clock are also provided in Fig. 6b. Correct behavior is observed. As expected the sequence 1111000011110000… is obtained.
Figure 7 depicts results for the two-phase architecture. Same two experiments than for the single-phase counterpart are shown. Correct operation is also observed.
Finally, additional simulation experiments have been carried out to further analyze the proposed clock schemes. It was already mentioned the potential of the two-phase architecture for improving clock skew tolerance with respect to the single-phase one. This is due to the overlapping of the two phases. It can be chosen so that enough overlap exist even if skew reduces it. Simulations to measure this tolerance have been done. For that, a different clock source has been used for each MOBILE stage in the pipeline and a variable controlling the position of its edges have been associated to each of them. Monte Carlo simulations applying Gaussian distributions to the clock variables have been carried out. The sigma parameter has been increased until the circuits fail. The single-phase chain of inverters with the skewed static inverters has been evaluated. For the comparison to be fair, a two-phase chain of inverters but with static logic between consecutive MOBILEs has been chosen for the experiment. The sigma tolerated by the two-phase circuit is three times larger than the tolerated by the single-phase one.

7 Conclusions

Single-phase and two-phase fine grain pipelined architectures based on MOBILE operating principle have been proposed, analyzed and experimentally validated. Both of them work on the basis of the edge-triggered evaluation feature and self-latching behavior of MOBILE gates and are so distinctive from what can be implemented with CMOS domino. There is not a similar single-phase domino counterpart and the

MOBILE two-phase solution eliminates the race-through failure inherent in the domino structure. In addition, the proposed interconnection schemes do not present the functional limitations of the later. For ultra-fine-grain pipelines which are the target of this paper, the two-phase architecture exhibits advantages over the single-phase solution. Mainly, the elimination of the lower bound on operating frequency associated to the timing interconnection constraints and a higher clock skew tolerance are pointed out.

Working circuits in a commercial technology have been presented and different experiments have been carried out showing correct operation in agreement with simulation predicted behavior. The fabricated circuits use a three-transistor circuit as NDR device and an efficient MOBILE gate topology.

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