Efficient Realization of MOS-NDR Threshold Logic Gates

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Introduction: Negative differential resistance (NDR) devices have been frequently used in the design of logic circuits [1] due to their unique NDR current-voltage (I-V) characteristic. This property can be exploited to significantly increase the functionality implemented by a single gate in comparison to CMOS and bipolar technologies [2].

Resonant tunneling diodes (RTD) have been widely used to demonstrate the operation of logic circuits which take advantage of the properties of NDR devices. In particular, a number of threshold gates (TGs) based on RTDs monolithically integrated with three-terminal devices which implement complex logic functions have been fabricated and have demonstrate high speed and robust operation [3]. However, most of the reported working circuits have been fabricated in III-V materials while *Si*-based tunneling diodes compatible to standard CMOS fabs are currently an area of active research [4].

To overcome this difficulty, we have resorted to MOS-NDR devices [5], which consist of MOS transistors and thus, can be fabricated by standard CMOS process. Moreover, circuit ideas coming from RTD-based designs can be extended to an “all CMOS” environment.

In this paper, we propose a new programmable MOS-NDR device which can be used to obtain efficient realization of Threshold Logic gates. To prove this, we have selected a key circuit whose performance, in terms of area and power consumption, can be improved with regard to other MOS-NDR or CMOS realizations.

The MOS-NDR programmable device: Figure 1a shows the schematic of the programmable MOS-NDR device which we have designed and fabricated (by a standard 0.13μm CMOS process) a programmable MOS-NDR device. Figure 1b shows the I-V characteristic of our programmable device (measured by HP-4145A parameters analyzer). The positive differential resistance (PDR) and the negative differential resistance (NDR) region are obtained through the current of $NMOS_2$ transistor, which gate-to-source voltage is modulated by the output voltage of the CMOS inverter made up by $NMOS_1$ and $PMOS_1$ and biased by V_{INV}. The peak voltage (V_p) and current (I_p) of the I-V characteristic in Fig. 1b can be modified by properly setting up the sizes of the transistor $NMOS_2$. In this way, I_p is increased with the width of $NMOS_2$. Assuming that all transistors have the same gate length, the position of V_p is controlled by the ratio between the widths of $NMOS_1$ and $PMOS_1$. Higher values of V_P are obtained by decreasing the ratio between the widths of the transistors $NMOS_1$ and $PMOS_1$, W_{NMOS1}/W_{PMOS1}.

The peak current can be also modified by the new branch consisting of two series-connected NMOS transistors, $NMOS_S$ and $NMOS_3$. $NMOS_S$ operates as a switch controlled by the voltage supplied to terminal *PROG*, V_S., so that when it is large enough to enable $NMOS_3$ the original peak current of the device is increased.

Design of MOS-NDR inverted majority gates: The operation principle of the programmable MOS-NDR device can be extended to implement logic circuits based on the MOnostable-BIstable Logic Element (MOBILE). The MOBILE is a rising edge triggered current controlled gate which consists of two MOS-NDR devices connected in series (the driver and the load) and driven by a switching bias voltage (V_{CK}). When V_{CK} is low both devices are in the on-state (or low resistance state) and the circuit is monostable. Increasing V_{CK} to an appropriate value ensures that only the device with the lowest peak current switches from the on-state to the off-state (the high resistance state). Logic functionality is achieved by modifying the peak current of one of the MOS-NDR structures, as described previously.

A threshold gate (TG) is defined as a logic gate with n binary input variables, x_i (i=1, …,n) one binary output y, and for which there is a set of (n+1) real numbers: threshold T and weights w_i, such that its input–output relationship is defined as:

$$F(x_1,\ldots,x_n)\begin{cases}1 \;\; iff \;\; \sum_{i=1}^{n} w_i x_i \geq T \\ 0 \;\; iff \;\; \sum_{i=1}^{n} w_i x_i < T\end{cases} \qquad (1)$$

The MOBILE operation principle can be easily extended to implement Threshold Logic gates with programmable MOS-NDR devices. Figure 3 depicts the implementation of a generic TG defined as y=1 iff x_1+ x_2-x_3- x_4≥T and 0 otherwise. Positive and negative weights are associated to the area of the MOS-NDR devices connected in parallel to the load and driver NDR, respectively. The effective relationship between the peak currents of the driver and the load will determine the final value of the output voltage.

The inverted majority gate of M inputs, $NMAJ_M$, is a key example of Threshold Logic gates. It can be written in terms of Eq. 1 as follows:

$$NMAJ_M(x_1,\ldots,x_n)\begin{cases}1 \;\; iff \;\; \sum_{i=1}^{n} x_i < M/2 \\ 0 \;\; iff \;\; \sum_{i=1}^{n} x_i \geq \lceil M \rceil/2\end{cases} \quad (2)$$

Figure 3a shows the circuit diagram of a MOS-NRD $NMAJ_3$ gate. Since all weights are equal to -1, the input branches are placed in parallel with the driver MOS-NDR. The operation of this gate is shown in Figure 3b, where it can be observed that when two inputs are equal to ‘1’ (‘0’) the output voltage goes to the low (high) level.

Simulation results: We have compared our $NMAJ_3$ gate realization with the design proposed by Mira, et al. in [6] (in Fig. 3c), so that we can check the efficiency in terms of area and power consumption. Unlike our structure, this design uses one CMOS inverter for each MOS-NDR device. Inverted majority gates of 3, 5 and 7 inputs have been analyzed. In order to make fair comparisons, we have selected the same sizes for the transistors, as well as the same values for the bias and the input voltages. We have performed a set

of simulations for different values of the frequency of the clock signal and we have measured the average power consumption for each circuit.

The proposed implementation of $NMAJ_M$ gives better results in terms of power consumption. Moreover, this performance is improved when the number of inputs and the operation frequency increases, as shown in Fig. 4a to 4c.

Since our structure only uses two CMOS inverters (one for the load and another for the driver NDR), the difference between areas becomes apparent when the number of inputs increases. We have defined the “normalized area” as the sum of the widths of all the transistors (we have considered that all the transistors have the same length). Fig. 4d shows the results of calculating the normalized area for both implementations of the $NMAJ_M$ gates.

Conclusions: A new realization of threshold logic gates based on a programmable MOS-NDR device is presented. It has been demonstrated to reduce the area and power consumption over a well known structure when the number of inputs and the operation frequency increases.

References

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