AI-Assisted Sigma-Delta Converters – Application to Cognitive Radio

José M. de la Rosa, *Fellow, IEEE*

***Abstract*—This brief discusses the use of Artificial Intelligence (AI) to manage the operation and improve the performance of Analog-to-Digital Converters (ADCs) based on Sigma-Delta Modulators ($\Sigma\Delta$Ms). The reconfigurable nature of $\Sigma\Delta$Ms can be enhanced by AI algorithms in order to adapt the specifications of ADCs to diverse input signal requirements, environment interferences, noise levels, battery status, etc. A high degree of programmability is required, which demands for scaling-friendly, mostly-digital analog circuit techniques as well as suitable topologies of Artificial Neural Networks (ANNs) to implement the AI engine. Moreover, the practical implementation of AI-assisted $\Sigma\Delta$Ms requires to adopt diverse design strategies – from the $\Sigma\Delta$M architecture itself to AI modules and circuit building blocks – which are overviewed in this brief. As an application and case study, an ANN-assisted ADC for Software-Defined Radio (SDR) and Cognitive Radio (CR) is considered. The system is based on the use of a widely-tunable Band-Pass (BP)-$\Sigma\Delta$M, and an ANN is used to predict the occupancy of frequency bands and modify the notch frequency of the BP-$\Sigma\Delta$M accordingly.**

***Index Terms*—Analog-to-digital conversion, sigma-delta modulation, artificial intelligence, neural networks, cognitive radio.**

I. Introduction

ARTIFICIAL Intelligence (AI) is one of the key technology players of the so-called *digital transformation*, which is shaping many different aspects of our daily lives [1], [2]. The use of AI algorithms is becoming more and more intensive in countless application scenarios which include, among others, multimedia pattern classification and recognition, biometric identification, robotics, computation, communications, etc. [3]–[7]. In most cases, AI modules are implemented in the form of Artificial Neural Networks (ANNs). Essentially, an ANN is a computing system formed by the interconnection of layers of *artificial neurons*, which are inspired by the way biological neurons set connections among them by means of *synapses* [8]. ANN-based AI systems, such as Machine Learning (ML) and Deep Learning (DL), are fuelled by an increasingly computing power provided by both cloud and edge computing, as well as the giant volumes of data collected and provided by Internet-of-Things (IoT) devices [9], [10]. This way, the combination of big data and AI is used nowadays to solve a number of automatization and optimization problems [7], [11].

Manuscript received January 24, 2022.

This work was supported in part by Grant PID2019-103876RB-I00, funded by MCIN/AEI/10.13039/501100011033, by the European Union "ESF Investing in your future", and by "Junta de Andalucía" under grants US-1260118 and P20-00599.

José M. de la Rosa is with the Institute of Microelectronics of Seville, IMSE-CNM (CSIC/University of Seville), C/ Américo Vespuccio 28, 41092 Sevilla, SPAIN, e-mail: jrosa@imse-cnm.csic.es.

Moreover, technology downscaling is allowing the integration of more and more systems into a single chip, with the subsequent benefits in terms of increased performance of information storage and management, together with communication and computation facilities, located in end-devices such as mobile phones and IoT nodes [12], [13]. Embedding AI modules in Systems-on-Chip (SoC) is becoming a commonplace in mobile terminals, where ML/DL engines are used for some specific tasks such as face or fingerprint recognition [7]. Moreover, ANN-based algorithms are also being applied to improve the performance metrics of analog circuits by means of linearization or calibration techniques [14]–[20].

These AI-empowered systems benefit from digital signal processing in terms of programmability, scalability and robustness against technology process and environment variations. Thus, the increasingly number of digital-driven applications and systems is moving the analog/digital interfaces closer and closer to the point where the information is either collected or transmitted, so that most part of the hardware is digital, and hence, easier to program via software. The need of earlier digitization makes the Analog-to-Digital Converter (ADC) one of the key components in many SoCs. The use of ML/DL algorithms can be applied to improve the performance metrics of ADCs [21], so that their main specifications such as the effective resolution and the sampling rate, can be dynamically adapted and optimized to diverse signal requirements, environment conditions, power/battery status, etc. AI algorithms can be also applied as optimization engines to automate the synthesis and design procedure of ADCs [22].

The state of the art on ADCs is mostly dominated by three architectures: Pipeline, Successive Approximation Register (SAR) and Sigma-Delta Modulators ($\Sigma\Delta$Ms) [23]–[27]. These techniques – or a combination of them – cover a vast range of applications: from biomedical devices, sensors, instrumentation to wideband communications. In terms of energy, SAR ADCs are more efficient in applications with resolutions below medium resolution ($11-12$ bit), while $\Sigma\Delta$M ADCs consume less energy if higher resolutions are needed. However, the efficient implementation of AI-managed ADCs demands for new generations of A/D interfaces which will be able to include strategies at both system and circuit level, and increase the degree of programmability and robustness to make them suited to be controlled by AI modules. Examples of these ADCs include hybrid SAR/$\Sigma\Delta$M/Pipeline [28], [29] or Noise-Shaping (band-pass) SAR ADCs [30], among others. At circuit level, some scaling-friendly/mostly-digital techniques such as time/frequency-based quantization [31], [32] or digital-assisted analog circuits [33], [34], are among the most promising candidates to implement programmable AI-managed ADCs,

since they are more suitable to embed ANN-based algorithms to enhance their performance.

The main goal of this tutorial brief is to present a survey of some circuits and systems techniques and design methods intended for AI-managed ΣΔM ADCs – going from system-level models, architectures and algorithms to circuit-level implementation. As a case study, the use of AI-managed ADCs for Cognitive-Radio (CR) digitizers is considered as one of the key technology enablers to implement efficient hand-held terminals and IoT nodes. The rest of this article is organized as follows. Section II explains the concept behind AI-empowered ΣΔMs, revisiting their main fundamentals. Section III discusses the use of ANNs as optimization engine for the automated synthesis of ΣΔMs. Section IV highlights some programmable and mostly-digital circuits suited for AI-assisted ΣΔMs. Finally, Section V shows a case study, and conclusions are drawn in Section VI.

II. AI-EMPOWERED ΣΔMS: THE CONCEPT

Fig. 1(a) shows a conceptual block diagram of an AI-managed ΣΔ ADC, where the operation of the ΣΔM is assisted by an ANN. In order for this system to work properly, the ANN should be previously trained to optimize the performance of the ΣΔM in terms of its main specifications, i.e. Signal-to-Noise Ratio (SNR), Dynamic Range (DR), Total Harmonic Distortion (THD), etc. These ΣΔM performance metrics are used as input variables for the ANN and its outputs are the design parameters that determine the maximum performance of ΣΔM in practice, i.e. the building-block electrical requirements such as: amplifier finite DC gain, Gain Bandwidth (GB), Slew-Rate (SR), Output Swing (OS), etc. The nonideal errors associated to ΣΔM building-block metrics are grouped into an error vector, denoted as $\bar{\epsilon}$, which degrades in practice the ΣΔM loop-filter transfer function, $H(f,\bar{\epsilon})$, and consequently the noise-shaping of the modulator.

Assuming a linear additive white noise model with gain k_q for the B-bit quantizer in Fig. 1(a), the Z-transform of the ΣΔM output, y, can be expressed as:

$$Y(z,\bar{\epsilon}) = \text{STF}(z,\bar{\epsilon})X(z) + \text{NTF}(z,\bar{\epsilon})E(z) \tag{1}$$

where $X(z)$ is the Z-transform of the input signal, $E(z)$ is the Z-transform of the quantization error, and STF and NTF stand for the signal- and noise-transfer functions, given by:

$$\text{STF}(z,\bar{\epsilon}) = \frac{k_q H(z,\bar{\epsilon})}{1+k_q H(z,\bar{\epsilon})}, \text{NTF}(z,\bar{\epsilon}) = \frac{1}{1+k_q H(z,\bar{\epsilon})} \tag{2}$$

Considering an Lth-order loop filter, it can be shown that the DR of a ΣΔM can be approximately given by [26]:

$$\begin{aligned}\text{DR} \approx & 6.02\cdot B + 1.76\text{dB} \\ & + 10\log_{10}[(2L+1)\cdot \text{OSR}^{(2L+1)}/\pi^{2L}] \\ & - \Delta_{\text{DR}}(\text{OSR}, L, B, \bar{\epsilon})|_{\text{dB}}\end{aligned} \tag{3}$$

where $\text{OSR} \equiv f_s/(2\cdot B_w)$, stands for the *oversampling ratio*, f_s is the sampling frequency and B_w is the signal bandwidth. The first term of Eq. (3) defines the Effective Number Of Bits (ENOB) of a Nyquist-rate B-bit ADC. As known, ΣΔMs increase ENOB with OSR by approximately $3\cdot(2L+1)$ dB/octave – second term in (3) – although this enhancement is degraded by the effect of circuit errors – conceptually formulated as Δ_{DR} in (3). The three *key parameters*, namely OSR, L and B, define the system-level performance of ΣΔMs, and can be combined in many ways, giving rise to a diverse topologies of ΣΔMs – single-loop or cascade; Low-Pass (LP) or Band-Pass (BP); single-bit or multi-bit; Continuous-Time (CT) or Switched-Capacitor (SC) — in order to achieve the maximum DR [35], [36].

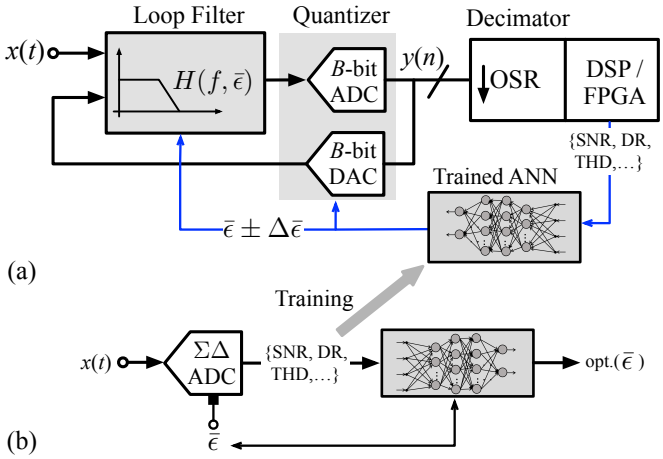

Fig. 1. AI-assisted ΣΔMs: (a) Conceptual diagram, (b) ANN training.

The idea behind an AI-empowered ΣΔM consists of using an ANN to minimize the DR degradation, Δ_{DR}, caused by circuit nonidealities, $\bar{\epsilon}$. To this end, an ANN can be trained to achieve the maximum performance for a given ΣΔM architecture. The training process is conceptually depicted in Fig. 1(b). During the design phase of the ΣΔM, training data is generated from simulated ΣΔM output metrics, i.e. SNR, THD, NTF, STF, etc. within the multi-dimensional design space formed by a number of design points defined by the combinations of design parameters inset $\bar{\epsilon}$. This way, the ΣΔM performance metrics (SNR, THD, etc), play the role of input variables of the ANN while $\bar{\epsilon}$ are the ANN outputs. This way, the learning process consists of *mapping* such input data, i.e. the ΣΔM specifications, onto the output data, i.e. the design parameters, $\bar{\epsilon}$, that optimize the performance of the ΣΔM.

Once the ANN is trained, it can be used to control the operation of the ΣΔM by modifying its building-block design parameters as depicted in Fig. 1(a). Thus, measured SNR, DR, THD, etc. are provided to the trained ANN, which generates a new set of design parameters, denoted as $\Delta\bar{\epsilon}$, that minimizes Δ_{DR}. This approach – successfully implemented as calibration scheme to linearize CT-ΣΔMs [6] – can be extended to control and optimize the performance of ΣΔMs.

III. ANN-ASSISTED SYNTHESIS OF ΣΔMS

In addition to be embedded in ΣΔM circuits to enhance their performance after being designed, ANNs can be used during the design phase of ΣΔMs. In this case, the ANN plays the role of the optimization engine which is combined with a simulator to automate the synthesis of ΣΔMs. Indeed, ANNs

have been already applied as part of the design methodology for the sizing of analog and mixed-signal circuits [14]–[17], [22], [37], and they can be used for the optimization of ΣΔMs.

Optimization-based synthesis methodology is widely used for the automatic sizing of circuits and systems, in order to find the best set of design parameters that meet the required specifications of a given circuit. To this end, the well-known *top-down/bottom-up* design procedure divides a given system – a ΣΔM in this case – into several hierarchy levels, so that at each abstraction level, the design process consists of transmitting *or mapping* the specifications in a hierarchical way: from the top level to the bottom level. Thus, at system level, ΣΔM specifications, B_w and ENOB, are mapped onto bulding-block specifications, i.e. the electrical requirements of amplifiers, transconductors, comparators, switches, etc. At this design stage, the design variables of the sizing problem are the finite DC gain, GB, SR, etc. Once these design variables are found, the sizing process is moved to the lower abstraction level, i.e. the electrical level, in which, after an appropriate topology has been selected for every ΣΔM subcircuit, transistor sizes and bias currents are obtained [38].

Fig. 2(a) shows the conventional flow diagram of the optimization-based high-level synthesis of ΣΔMs based on the combination of behavioral simulation (SIMSIDES in this example [39]) as performance evaluator, and an optimizer to explore the design space and find the optimum set of building-block electrical parameters to get the optimum modulator performance. The starting point is the modulator architecture. Here, the design parameters are the building-block specifications; that is, the nonideal parameters used to model the main error mechanisms that affect the performance of ΣΔMs and define the electrical specifications of its subcircuits: integrators, comparators, DAC elements, and so on, which are generically denoted in this paper as $\bar{\epsilon}$. Considering arbitrary initial conditions in Fig. 2(a), a set of perturbations of the design parameters is generated by the optimizer. With the new design parameters, a new set of simulations is carried out to evaluate the modulator performance and the process is repeated in an iterative way until a cost function is optimized. The type and value of such perturbations, as well as the iteration acceptance or rejection criteria, depend on the type of optimization method, i.e. evolutionary algorithms, genetic, simulated annealing, etc [26], [40].

Some authors propose using ANNs in an optimization-based synthesis methodology. In some works, the ANN has been trained to replace the simulator, while other approaches consider ANNs as the optimization engine [14]. In the latter case, the ANN is trained to size a given system for a set of specifications. Thus, the ANN should be trained with sized solutions known from prior optimized designs. Once the ANN is trained, it is able to automate the sizing process and generate optimum sizing solutions for additional sets of specifications which were not considered in the training dataset. This methodology, proposed in [14] for arbitrary analog circuits, is illustrated in Fig. 2(b) for the optimization of ΣΔMs.

As conceptually depicted in Fig. 2(b), the data used to train the ANN is comprised of a set of data pairs denoted as $\{\bar{\epsilon}, \bar{\Gamma}\}$,

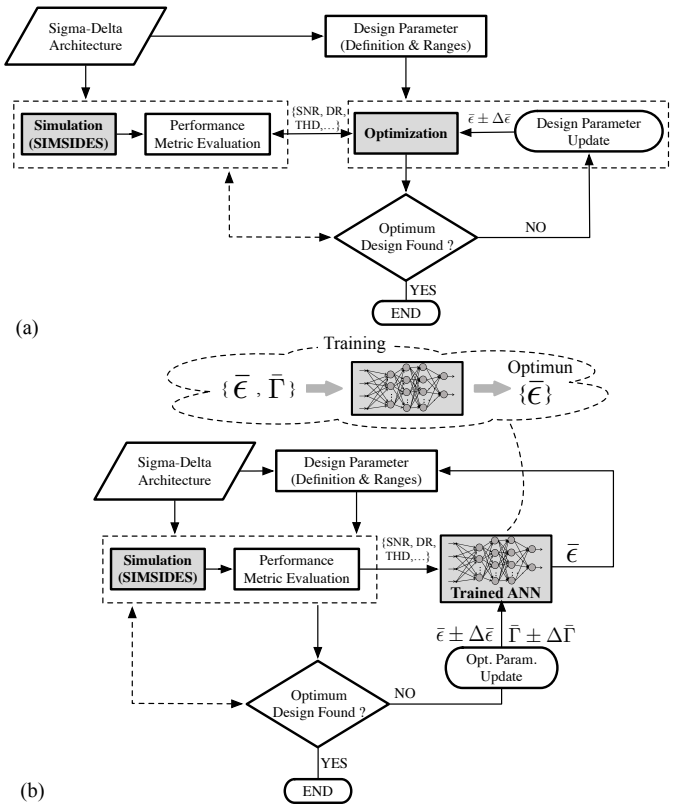

Fig. 2. Using ANNs to optimize the high-level design of ΣΔMs: (a) Conventional synthesis methodology, (b) ANN-based synthesis methodology.

where $\bar{\Gamma}$ stands for a vector of performance metrics, i.e. SNR, B_w, THD, etc. In order to train the ANN, an input dataset $\{\bar{\epsilon}, \bar{\Gamma}\}$ is generated from a database of previous simulations of ΣΔMs which led to useful designs[1]. This dataset can be augmented to increase the number of input data to train the ANNs, so that they can learn to find optimum designs outside the train set distributions. Once the ANN is trained, it can be used to generate optimum designs, i.e. to provide an optimum case of $\bar{\epsilon}$ that satisfies a given set of specifications. To that end, the ANN-based optimizer is combined with a behavioral simulator (SIMSIDES) to explore the design space and to find the best design as illustrated in Fig. 2(b).

ANNs can be implemented in many different ways, regardless it is used as an optimization algorithm to design ΣΔMs (Fig. 2(b)) or as part of the circuit itself (Fig. 1(a)). In the latter case, it can be either synthesized in hardware, as an Field-Programmable Gate Array (FPGA) or as an on-chip dedicated module, or software embedded in a Digital Signal Processor (DSP). There are also diverse ways to connect artificial neurons, either in a feedforward or Recurrent NNs (RNNs), or including hidden layers of neurons – referred to as Deep NNs or DNNs. Depending on the degree of connectivity of their neurons, ANNs can be divided into fully-connected ANNs – where each neuron in a given layer is connected to

[1]Typically, thousands of simulations are needed to generate the training dataset. This may take several hours depending on the computing resources. However, once this dataset is generated, it can be applied to a number of different synthesis problems, where the training and optimization process may take a few minutes, depending on the ΣΔM architecture and specifications.

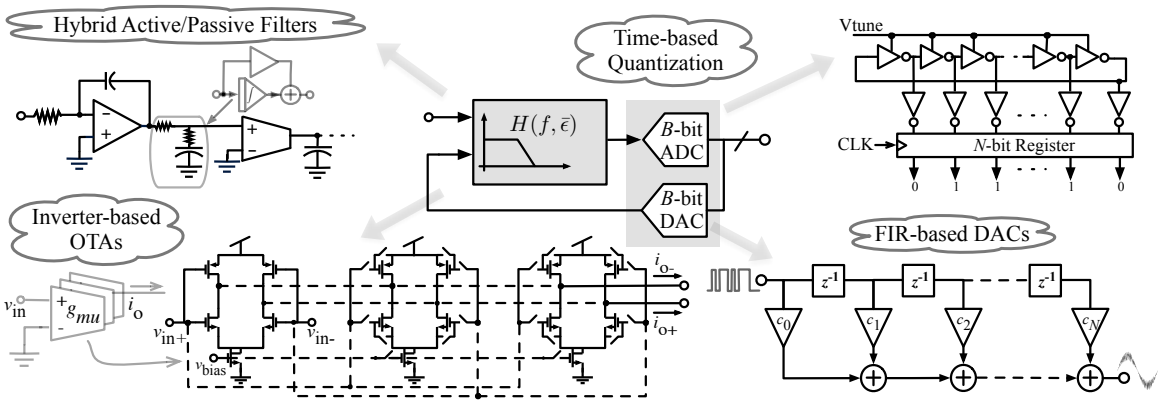

Fig. 3. Scaling-friendly analog circuit techniques for mostly-digital ΣΔMs.

all neurons of the remaining layers – or Convolutional Neural Networks (CNNs), where each neuron is connected to a given subgroup of neighboring layers[2].

IV. Digital-Friendly Programmable Analog Circuits for AI-managed ΣΔMs

Highly-reconfigurable analog circuits are needed to increase the programmability of ΣΔM building blocks, so that their operation can be managed by an ANN module. Digital-assisted, scaling-friendly analog circuits – some of them highlighted in Fig. 3 – are suited for AI-enhanced ΣΔMs [41].

Inverter-based and VCO-based Operational Transconductance Amplifiers (OTAs): A good candidate is the use of CMOS inverters for the realization of OTAs, as originally proposed by Nauta [42]. Since the first inverter-based OTAs, there has been an increasing interest to apply this technique for the implementation of filters and ADCs, due to their better efficiency for the required gain performance and bandwidth [36]. More and more digital circuits are being embedded to improve the performance of analog circuits, by means of calibration, tuning, etc, that try to alleviate the limitations of nanometer CMOS analog circuits [43]. In spite of their potential benefits, inverter-based OTAs offer lower performance metrics such as robustness over PVT variations, impact of circuit parasitics, limited DC gain, etc. Some authors have proposed improved versions of inverted-based OTAs [43]–[48] and their use is becoming more and more popular in ΣΔMs [33], [34], [49]. Other authors suggest the use of Voltage-Controlled Oscillators (VCOs) to implement OTAs, as an alternative to increase the gain of inverter-based OTAs for lower supply voltages, and to implement highly-programmable ΣΔMs [50].

Hybrid Active/Passive ΣΔMs: Another approach to reduce the number of power-hungry circuits consists of replacing some active building blocks with passive circuit elements. This has a number of drawbacks such as the loop-filter gain loss, increased thermal noise and a higher sensitivity to technology process variations and parasitics. In spite of these limitations, passive RC networks are becoming a popular circuit solution for the implementation of ΣΔMs in diverse applications [51]–[56]. Indeed, hybrid active/passive circuits are suited for reconfigurable loop filters such as Time-Interleaved (TI) or N-path filters [57] made up of switchable RC networks [58].

Time-based Quantization: Another *scaling-friendly* approach is based on translating the quantized information from the amplitude domain to the time domain by means of a voltage-to-frequency conversion. The principle of operation behind this approach, proposed in [59], relies on the use of a ring oscillator to count the number of edges within a given time period as conceptually depicted in Fig. 3. The result is directly related to the input signal, thus obtaining a digital representation of the amplitude. In addition to their higher speed and lower supply voltages, VCO-based quantizers provide an implicit first-order noise-shaping filter [15], [31], [32], [59]–[71]. However, it is limited in practice by the nonlinearity of the voltage-to-frequency conversion, requiring the use of either calibration or linearization techniques [65]–[67], [72], [73]. An alternative to VCO-based quantizers consists of using pulse-width modulation (PWM) [74], [75] and a Time-to-Digital Converter (TDC) that generates a time-quantized representation of the signal [76]–[80]. The so-called Gated Ring Oscillators (GROs) have been successfully applied attenuate the nonlinearity of VCOs and be combined with active-RC integrators, thus benefiting from both amplitude- and time-based circuit techniques [81].

Finite Impulse Response (FIR) Feedback DACs: Regardless the ΣΔM quantizer is realized either in amplitude or time domain, by increasing the number of bits yield to an increase of the circuit complexity and nonlinearity of the feedback DAC. These problems can be palliated by using a DAC with a FIR filter [51], [82]–[84]. The idea – originally proposed in [85] and conceptually illustrated in Fig. 3 – is to feedback a filtered version of the single-bit quantization output, such that due to the high-frequency attenuation of the FIR filter, the DAC output, is a multi-level waveform. This allows to achieve the low-jitter sensitivity and high linearity of a multi-bit ΣΔM, while keeping the simplicity and robustness of single-bit ΣΔMs [84], [86]. The combination of TI topologies and FIR DACs is an alternative to implement GHz-range ΣΔMs [87], [88]. Moreover, FIR DACs make it easier to digitally control ΣΔM specifications by mean of an ANN, as required in AI-assisted ΣΔMs.

[2]A detailed explanation of ANNs is beyond the scope of this brief and the interested reader can find a large number of references in literature [7].

V. Case Study: AI-Managed ΣΔMs for CR ADCs

As a case study, let us consider the CT BP-ΣΔM shown in Fig. 4(a) intended for RF ADCs in CR systems. This is a communication paradigm that allows to make a more efficient use of the frequency spectrum, by dynamically modifying receiver specifications according to the information sensed from the electromagnetic environment. In this example, an AI module – made up of Long Short-Term Memory (LSTM) networks – is used to predict and to identify the least occupied frequency band [89], [90], so that the noise-shaping of the BP-ΣΔM is modified accordingly, in order to operate over the selected band. This feature can be realized by BP-ΣΔM ADCs with a widely tunable *notch* frequency, f_n, while keeping the required resolution over the digitized band [41], [91].

The BP-ΣΔM of Fig. 4(a) is designed in 65-nm CMOS, and consists of a 4th-order loop filter made up of inverted-based Gm-LC resonators and a 4-bit quantization [92]. The loop-filter resonators are based on programmable inverter-based transconductors like those shown in Fig. 3, which are in turn made up of unitary circuit elements that can be connected or disconnected depending on the operation mode required for the digitizer. This way, the tuning of specifications can be managed by the AI module. Both system-level and circuit-level reconfiguration techniques are considered to allow the modulator to digitize signals placed at several carrier frequencies, ranging from 450MHz to 950MHz, with a programmable 1.2/2GHz clock rate [92], [93].

As stated in Section IV, inverted-based unitary transconductors are simple and modular, thus increasing the flexibility and programmability of the RF ADC according to the information provided by the ANN engine. In order to adjust the values of the requested loop-filter coefficients with a higher accuracy, different values of the unitary transconductance are used, namely: g_{mu}, $1/2g_{mu}$. These values can be easily changed by properly scaling the value of the tail current, I_{bias}, of the unitary transconductors as well as the sizing. Another reconfigurable circuit strategy consists of programming the resonant frequency by using banks of switchable unitary capacitors, which are in turn digitally controlled in order to program the value of f_n required for the BP CT-ΣΔM to work in each operation mode [26], [92].

The performance of the CT BP-ΣΔM can be adapted to the different operation modes with optimized power consumption, by adjusting the biasing of all building blocks by means of a programmable master current generator. One of the characteristics of highly programmable ADCs is the huge number of digital control signals required to control and program their operation. For instance, in a reconfigurable BP CT-ΣΔM like that shown in Fig. 4, almost 200 digital control signals are needed. Such a large number of digital signals are provided in practice by a serial-to-parallel register that collects a serial input data and transforms this data into a set of parallel control bits which program the operation of the ADC [26].

This way, the CT BP-ΣΔM can be digitally programmed in an easy way, by loading the required control configuration for each operation mode. In the case of AI-managed digitizers for CR end-devices, the serial input data contains the information sensed from the electromagnetic environment, which is provided by the ANN engine, as conceptually illustrated in Fig. 4(a). Fig. 4(b) shows the evolution of the occupancy signals of several channels. Every time the ANN engine selects a certain channel, control parameters of different building blocks in the CT BP-ΣΔM can be modified accordingly. This is illustrated in Fig. 4(c), that shows how the notch frequency of the BP CT-ΣΔM can be tuned according to the feedback provided by the LTSM-based ANN module. In order for the overall CR system to operate correctly, the granularity of the programmability of the ΣΔM-based ADC must be as fine as possible in order to give the AI engine more degrees of freedom to properly choose the best parameters to optimize the communication in the selected channel.

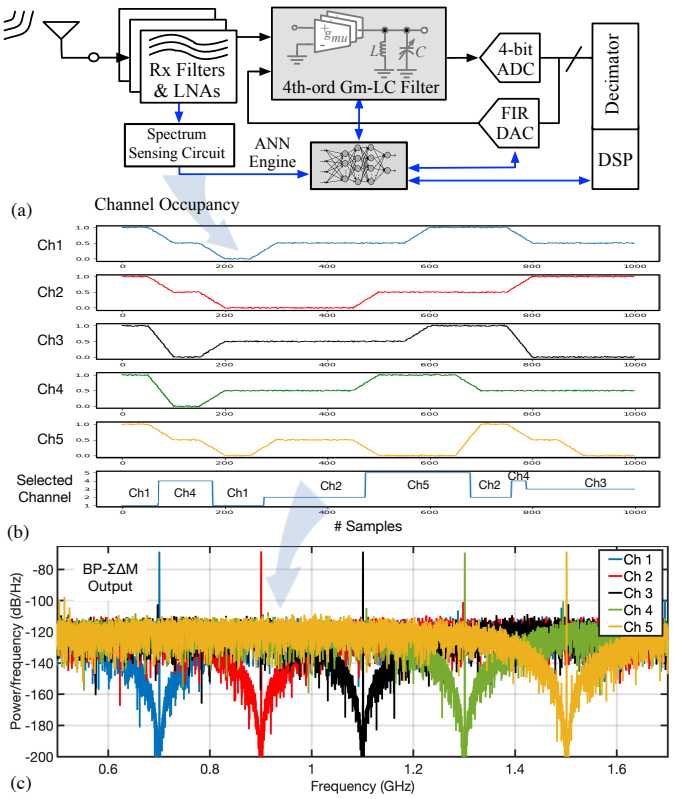

Fig. 4. AI-assisted BP-ΣΔMs for CR systems: (a) Receiver (Rx) diagram, (b) Channel occupancy over time, (c) BP-ΣΔM Noise shaping tuning.

VI. Conclusions

The performance of ΣΔM ADCs can be improved by the action of AI algorithms implemented as ANNs. These engines can be used as an enhancement building block to manage and control the operation of ΣΔMs. They can also assist the synthesis methodology of ΣΔMs by playing the role of an optimizer to find out the best sizing solution in a top-down design process. The practical implementation of these AI-assisted techniques would impose a number of design trade-offs which involves reconfiguration techniques at both circuit and system level, as well as new design methods and CAD tools. Some of them have been overviewed in this tutorial brief, while many others are still open to research.

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