AI-Managed Cognitive Radio Digitizers

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Abstract—Embedding Artificial Intelligence (AI) in integrated circuits is one of the technology pillars of the so-called *digital transformation*. Nowadays, the vast majority of electronic devices benefits from digital signal processing to implement more and more functionalities, which can be further enhanced by the action of AI algorithms and artefacts. Moreover, as the analog/digital interfaces are moving closer and closer to the point where the information is either acquired or transmitted, the so-called AI-managed data converters are becoming key building blocks in an increasingly number of interconnected *cyberphysical* systems – made up of both software and hardware components. Software Defined Radio (SDR) and Cognitive Radio (CR) systems intended for 5G/6G communications are good examples which can benefit from an early digitization managed by AI engines.

In this context, this paper presents an overview of circuits and systems techniques for AI-managed analog/digital interfaces with application in SDR/CR mobile telecom systems. Some design trends and challenges are discussed, going from new communications and computing paradigms for AIoT devices and networks, to digital-based/scaling-friendly analog circuit techniques for an efficient digitization. The state of the art on Analog-to-Digital Converters (ADCs) is surveyed, putting emphasis on highly-programmable Sigma-Delta Modulators ($\Sigma\Delta$Ms) as one of the best ADC candidates for SDR/CR transceivers. Some chip examples are shown to illustrate their potential application in AI-enhanced CR end-devices.

Index Terms—Cognitive Radio, software defined radio, artificial intelligence, analog-to-digital conversion, sigma-delta modulation.

I. INTRODUCTION

THERE is no doubt that we are living one of the greatest technological revolutions in the history of humankind. Some *disruptive technologies* such as Artificial Intelligence (AI), big data, robotics and cloud computing, are becoming more and more present in our daily lives, and they have accelerated their pace of penetration, prompted by the needs arisen from the global crisis generated by the COVID-19 pandemic, transforming many of our social and economic activities towards a virtual format. This *digital transformation* [1] is fuelled by the continuous evolution of the micro/nanoelectronics industry, that has exponentially grown over the last six decades as predicted by Moore's law. Nowadays it is possible to design chips which contain billions of transistors with dimensions close to a few atoms of silicon [2].

Among other benefits, the downscaling of microelectronics allows the pervasive integration of information, communication and computation technologies in everyday objects, giving rise to the so-called Internet of Things (IoT) as one of the key technology players in the virtualization process. IoT implies the interconnection of billions of *cyberphysical* entities, which can either be physical or virtual, with a hybrid software/hardware structure, capable of communicating with each other, sometimes without the need of human intervention thanks to Machine-to-Machine (M2M) communication protocols. Moreover, IoT is expected to have a potential impact on the global economy of 11.1 trillion dollars in 2025, what means above 10% of the gross domestic product globally, about 30 billion connected devices in year 2023 and 350 billion by 2030 [3], [4].

IoT devices need to be equipped with a certain level of *intelligence*, so that they can make decisions in real time, and locally, i.e. without being connected to remote servers. It is therefore necessary to address a number of design challenges in order to build a solid bridge between the physical environment and its corresponding virtualized version. Efficient IoT nodes will require also the development of hybrid software/hardware platforms, new computation paradigms and communication protocols, as well as highly adaptive and programmable circuitry, and very specially in the analog side of the system and the analog/digital interface [2], [3], [5], [6].

One of the main bottlenecks associated to the increasingly number of IoT devices which will have an impact of the design of end-devices is the increasingly shared use of the electromagnetic spectrum. Although new bands – such as millimeter wavelengths (mm-Wave or mm-W) – are being incorporated in the latest generations of mobile networks (5G and the incoming 6G), they will also keep increasing the traffic of data [7]–[13]. The so-called Cognitive Radio (CR) [14] allows communication systems to make a more efficient use of the frequency spectrum, by dynamically modifying the transceiver specifications according to the information sensed from the electromagnetic environment [15]. An efficient implementation of CR-based terminals may benefit from embedding AI engines in their main building blocks, which in turn will need new Circuits and Systems (CAS) strategies with a high degree of programmability and reconfigurability in order to dynamically select the optimum set of performance metrics and transmission bands [3], [9], [13], [16]–[19].

Fig. 1 shows the conceptual diagram of a CR-based transceiver, where the operation of its main building blocks is controlled by an AI engine. CR-based mobile terminals would require also that the analog/digital (A/D) interfaces should be placed as close as possible to the antenna, so that most of the hardware can be essentially digital, thus being easier to program its functionality by software. Another key technology
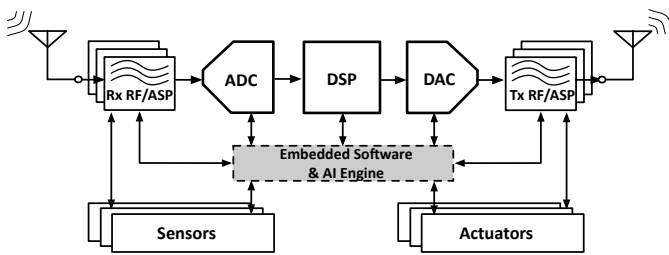
Fig. 1. Conceptual diagram of a CR-based AI-managed transceiver.

Fig. 2. Evolution of mobile telecom systems.

enabler is related to the use of AI-managed Analog Signal Processing (ASP) and Radio-Frequency (RF) front-ends, so that they can set their best specifications in an autonomous way, according to the environment conditions (communication coverage, band occupancy, noise and interferences, etc.), battery status and energy consumption. However, the practical realization of CR-based IoT devices requires highly programmable *digital-friendly* analog/RF front-ends [20].

In this context, this paper overviews some emerging strategies – including telecom systems and computing architectures, AI algorithms based on neural networks, as well mostly-digital/digital-assisted analog circuit techniques – intended for energy-efficient CR-based end-devices. A survey of the most important technology enablers is given to set the application scenario and define the main objetives that should be addressed by AI-managed CAS for CR-based IoT nodes, by focusing on the Analog-to-Digital Converter (ADC) as one of their key building blocks. The state of the art is briefly surveyed and main architectures and circuit strategies to implement programmable, digital-friendly digitizers are overviewed, putting emphasis on Sigma-Delta Modulation ($\Sigma\Delta$M) as one of the best candidates to implement AI-managed digitizers.

The rest of the paper is organized as follows. Section II gives an overview of mobile telecom systems, which have evolved from voice-transmission devices to AI-empowered multimedia handheld computers. Section III presents some background and fundamentals of CR systems. The other important pillar of CR/AIoT networks is the AI engine and neural computation, which is discussed in Section IV. Section V goes down to circuit level and focuses on the main objective of this article: analog/digital interfaces based on mostly-digital highly programmable $\Sigma\Delta$Ms. Section VI shows some chip examples and case studies and conclusions are drawn in Section VII.

II. FROM VOICE-TRANSMISSION TO CONNECTED-INTELLIGENCE

Wireless communications are key elements for the optimal implementation of CR/AIoT end-devices and networks. They must be adapted and programmed to communicate with very diverse types of devices – from computers and mobile phones to household appliances, industrial robots, etc – and interact with both virtual and physical media, through sensors, actuators and transceivers, having a high capacity of reconfigurability and adaptability to the very diverse conditions in which wireless communications take place [21]. The vast majority of IoT nodes are equipped with diverse types of
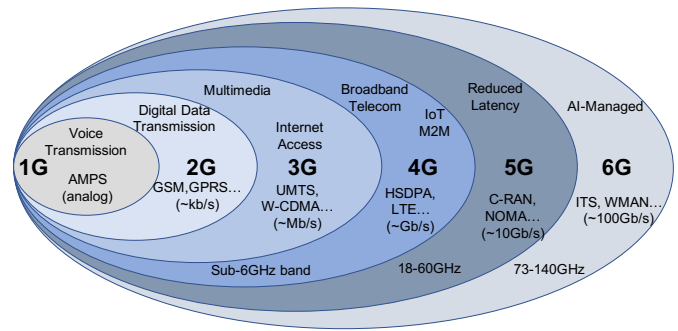
wireless communication systems, thus benefiting from the rapid evolution of *i-devices* such as tablets, cell phones, smart watches as well as many other wearable gadgets. This has led to a second wave of the digital transformation, fuelled by the complement action of three main technology vectors: digitization, computation and communications [1].

A. Evolution of Mobile "Phones"

To get an idea of the pace of evolution of mobile communications it is illustrative to look at some of the most representative operation modes, standards and main services offered by the different generations of wireless systems, illustrated in Fig. 2. At the beginning of the wireless telecom era, about three decades ago, mobile terminals were simple electronic devices whose only functionality was the voice transmission – called first generation (1G). Later, the so-called second generation (2G), incorporated a Short Message Service (SMS), whose data transmission speeds were in the order of a few kilobits per second (kb/s). With the development of the third generation (3G) in the first years of this century, mobile phones began to transform into *handheld computers*, by offering a number multimedia services as well as wideband connection to the Internet, with data transfer rates of several Megabits per second (Mb/s). This was followed by the fourth-generation (4G), which included previous communication standards – such as GSM, GPRS, EDGE, UMTS, Bluetooth, Wireless LAN, etc. – with new ones – such as HSDPA and LTE. The fourth generation of cellular networks is widely extended, by making it possible to notably increase the data rates, ranging from hundreds of Mb/s to Gigabits per second (Gb/s) – depending on the network conditions [22], [23].

This trend is set to continue and the fifth generation (5G) mobile telecom is being progressively implemented, reaching up to tens of Gb/s data rates, thanks to new communication standards operating in different frequency bands – ranging from the sub-6GHz band to the mm-W band. Moreover, 5G networks are extending the possibilities of IoT services and applications, with an estimated volume of wireless data traffic 1000 times higher than that achieved a decade ago. Among others, 5G allows the realization of new multiple access techniques such as Non-Orthogonal Multiple Access (NOMA), as well as the so-called Cloud Radio Access Network (C-RAN) protocols. In addition to its higher operation frequencies, 5G will bring a notably reduction in latency. This feature
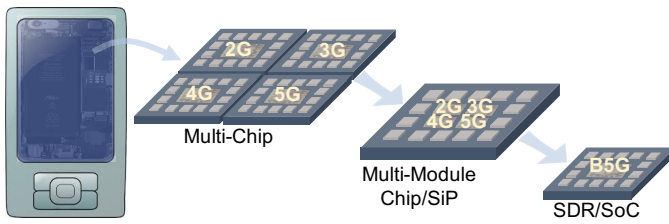
Fig. 3. Multi-standard chipsets embedded in mobile telecom: from hardware-based multi-chip and SiP modules to reconfigurable SDR-based SoCs.
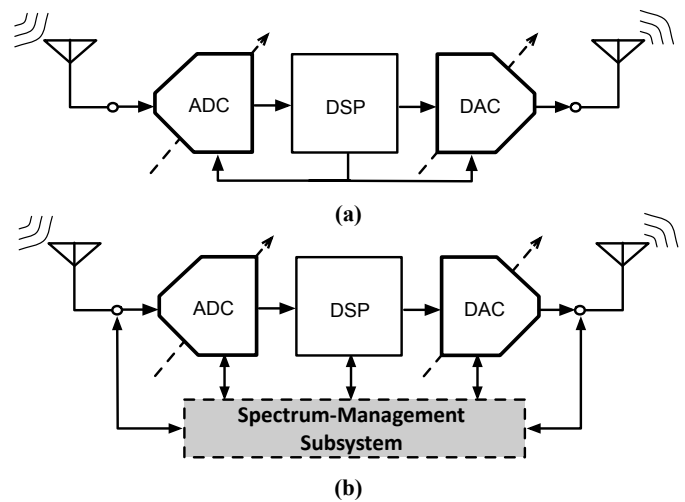

Fig. 4. Conceptual diagram of SDR and CR transceivers: (a) SDR transceiver, where signals are ideally transformed from RF to digital domain – unfeasible in practice due to the power-hungry A/D interfaces (ADC in the receiver path and DAC in the transmitter path). (b) Ideal CR transceiver made up of two main building blocks: the SDR and a spectrum-management subsystem.

provides real-time interactivity for services where peer-to-peer communication must be almost instantaneous. This is specially critical in applications like telemedicine, very demanded to remotely monitor some situations like epidemics or severe deseases where it is difficult to access in person to the patients [8], [10], [11], [23], [24].

B. Towards Software Defined Radio

Although most smart phones already present a great number of the mentioned standards and applications, the current addition mechanism of new operating modes and services are difficult to sustain since they do not scale. Every time a new communication protocol is developed, it usually requires a dedicated RF and baseband chipset to implement it on the device – conceptually illustrated in Fig 3. There are a number of different System-in-Package (SiP) technologies, in which the required components are assembled by using *ultra-dense* packaging, so that the physical volume of the electronic parts of every new mobile generation either remains constant or even shrinks. Moreover, it could be said that many of today's cellphones are marvels of miniaturization although fundamentally, they are still just *plain* radios. Even though this trend turns into a significant increase in component count and Bill of Materials (BoM), the final product price can be kept or even reduced, partially thanks to the huge number of terminals sold. Indeed, the celerity at which new functionalities are incorporated in handheld devices is starting to exceed the rate of package reduction and the trend towards Systems on Chip (SoC) provided by technology downscaling. Addressing this challenge implies redefining the concept of mobile terminals, going from pure hardware-based to hybrid hardware/software-based devices [6], [22], [25]–[28].

As envisaged by Mitola in 1995 [29], a Software-Defined-Radio (SDR) is defined as a universal radio platform which can be programmed to steer any frequency band, and process arbitrary communication protocols, while ensuring the required quality of service as well as guaranteeing privacy and security [6]. An ideal SDR transceiver – conceptually depicted in Fig. 4(a) – would process all information in the digital domain, so that it would be composed by three main building blocks: the antenna, the A/D interfaces and the DSP. As will be discussed later, this implementation is not realistic due to the huge amount of power consumed by the A/D interfaces, what requires at least some analog signal conditioning circuitry (see Fig. 1), to really implement an efficient interface between RF signals and the digital data.

SDRs are the base platform to implement CR technology in order to make a more efficient use of the electromagnetic spectrum [14], by dynamically modifying its transmission and reception parameters according to the information sensed from the environment – a technique also referred to as *spectrum sensing*. Essentially, CR-based technology enables wireless networks and handheld terminals to use the RF spectrum in a dynamic manner. As a result, a more efficient use of licensed/unlicensed spectrum can be done, with reduced interferences and/or at a lower power consumption. This way, SDR/CR-based mobile terminals would be capable of dynamically *sensing* their spectral environment and to exploit the captured information to change their transmission/reception parameters in order to improve the communication link and to reduce the energy consumed on the fly.

Therefore, SDR/CR devices must be smart enough to incorporate cognitive (also referred to as *spectrum-sensing*) capabilities, and *flexible* enough to be dynamically programmed according to the information obtained from their interaction with the environment. As conceptually illustrated in Fig. 4(b), SDR/CR systems can be divided into two main building blocks: the SDR transceiver itself and a spectrum-management subsystem. The latter will do the cognitive tasks required to implement CR functionalities. Note that this approach is completely different from the fixed spectrum assignment policy followed by today's mobile telecom systems, in which a large portion (around $80 - 90\%$) of the assigned radio spectrum is used sporadically while the remaining bands are truly busy at any given time. Indeed, it is expected that the combined use of SDR and CR approaches can be advantageous to optimally selecting the most suitable parameters for the communication systems, depending on the environment conditions, interferences, battery level, etc. as well as optimizing power consumption. It will also add flexibility in a number of applications such as autonomous vehicles, thanks to the
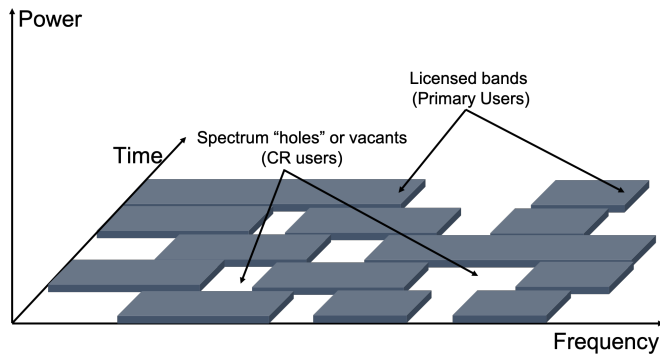
Fig. 5. Illustration of the concept of CR: frequency allocation and occupancy over time by primary users (PU) versus secondary users (SU).

incorporation of new protocols such as the so-called Vehicle-to-Everything (V2X) [16], [30].

As will be discussed later, one of the direct consequences of the physical implementation of SDR/CR-based terminals is that the RF signal conditioning, the ASP and the digitizer, i.e the circuits responsible for transforming the signals from the analog/RF to the digital domain, should be moved as close as possible to the antenna, so that most of the hardware is digital and hence, it is easier to program via software. This is however one of the main design challenges and bottlenecks – specially from the circuit designer perspective. But, before going down to the circuit level, it is illustrative to get some insight about CR systems.

III. BACKGROUND ON COGNITIVE RADIO

The idea of CR was first proposed by Mitola more than 20 years ago [14]. As illustrated in Fig. 5, the core concept behind CR systems consists of using free, vacant bands or *frequency holes*, by CR users, also known as Secondary Users (SUs), when those bands are not occupied by the Primary Users (PUs). This way, those users (PUs) who occupy frequency bands assigned or licensed to commercial communication standards and protocols in a given location, can allow CR users (SUs) to use their bands when they are vacant. For that reason, sometimes CR is also referred to as an *opportunistic* radio approach, since their users, i.e. SUs, make use of licensed frequency bands only when they are not occupied by their owners, i.e. PUs. The CR concept is really clever and pretends to make a more efficient use of the electromagnetic spectrum. However, the real implementation of CR presents a large number of practical limitations, which go from aspects related to legal regulations dealing with the bands licensed to mobile companies and internet providers for its commercial use, to the so many technical challenges – such as for instance the interferences caused by SU/CR users to PU/licensed users as well as the spectrum-management tasks (access, sensing, band allocation, handoff, etc.) [15], [16], [31].

A. CR Regulation, Standards and Modalities

Several regulatory institutions around the world – including the International Telecommunication Union (ITU), the European Telecommunications Standards Institute (ETSI) and the Federal Communications Commission (FCC) – are working to set the corresponding legal and technical regulations for CR to be implemented in the most efficient way, in order to make use of the spectrum which can be dynamically changed over the time and places, without interfering with the licensed users at different locations and regions. There have been several approaches to this problem, which go from occupying some unused and/or unlicensed, portions of the spectrum, like digital broadcasting TV *white spaces* or the Industrial, Scientific and Medical (ISM) bands. The first CR Wireless Regional Area Network (WRAN) standard, IEEE 802.22, was developed by IEEE 802 LAN/MAN standard committee and published in 2011. This standard – which can be considered as the *official* communication protocol for CR systems – is based on geolocation and spectrum-sensing techniques in order to identify unused portions (bands, channels) of the frequency spectrum in a given time period and/or in a specific location or geographical area [15]–[18], [32].

Attending to the degree of reconfigurability of transmission and reception parameters, CR systems can be divided into two main categories: *Full CR* – also known as Mitola radio – in which the CR system must sense all transmission parameters required to reconfigure the entire operation of CR transceivers and *Spectrum-Sensing (SS)* CR, where just the sensing of the RF spectrum is taken into account by CR transceivers. There are other classification criteria of CR systems depending on whether they use or not some portions of licensed bands such as ISM, Bluetooth or IEEE 802.11; the spectrum mobility over band transitions, etc. Most existing research and practical implementations of CRs focus on SS-based CRs, since they are the best candidates to put the concept of CR transceivers in practice [16]–[18].

B. Spectrum Management in CR

As stated above, CR systems must be able to develop several spectrum-management functions, which include at least the following ones [16], [31], [33], [34]:

- *(1) Spectrum sensing*: determine and identify the available frequency holes,
- *(2) Spectrum decision*: select the best portion of the spectrum among detected holes,
- *(3) Spectrum sharing*: manage the spectrum so that it can be shared by CR users (SUs) without interfering PUs,
- *(4) Spectrum allocation*: vacate the occupied channels/bands when PUs require their use.

In order to implement these functions, CR transceivers must be capable to interact with the electromagnetic environment to sense the information needed i.e. CR circuits and systems need to be doted with some kind of *cognitive capability*. On the other hand, CR transceivers must be able to *reconfigure* their specifications – in terms of sensitivity, selectivity, Quality of Service (QoS), frequency band, power consumption, modulation scheme, etc. – in order to adapt the performance of the transceiver building blocks to the information sensed from the surrounding environment. This way, any CR transceiver must have at least two main building blocks as illustrated in Fig. 4(b): the transceiver itself and a spectrum-management
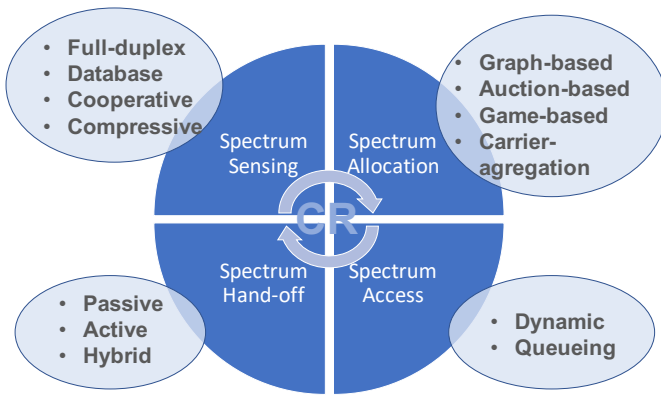
Fig. 6. Overview of CR spectrum-management techniques.

subsystem. The former will process the information as in any other wireless transceiver, while the latter will be responsible for doing the spectrum-management functions listed above. Embedded software or hardware (or a mix of both) are needed to implement the required signal processing algorithms together with the main part of the system, i.e. the transceiver, which will essentially process the information signals.

As stated above, Spectrum Sensing (SS) is one of the most important tasks to extract the required information from the electromagnetic environment, so that CR systems can detect the best band to be used by SUs without interfering the operation of PUs. There have been many diverse SS techniques reported so far, including among others: energy detection, cyclostationary-feature detection, matched filter detection, etc. The former, energy detection, is one of the most used ones, since it is relatively simple to implement, based on detecting the presence or absence of a signal by sensing/measuring the power received in a given band. However, in spite of its simplicity, it is not easy for the energy detector system to distinguish what is really an information signal from simply noise variance information flowing through the communication channel. To this end, more sophisticated and precise strategies – such as matched filter or cyclostationary-feature detectors – are used. Cyclostationary-feature detection method is based on the idea that deterministic information signals being propagated through the electromagnetic spectrum, i.e. those signals which carry information, are not simply channel noisy signals. Therefore, these signals follow a well-known communication protocol based on a modulation technique, such as BPSK, QPSK, OFDM, etc, and feature a cyclostationary behavior – not shown by Additive White Gaussian Noise (AWGN) present in the communication channel. There has been a number of approaches to implement spectrum-management techniques – summarised in Fig. 6. The detailed explanation of all of them can be read in detail in the open literature[1] [16], [33], [34].

Apart from the above mentioned techniques – which can be generically grouped as narrowband techniques – there are other SS-based CR approaches based on a wideband analysis and inspection of the spectrum. Although these methods can

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[1]The interested reader can find more details about these techniques in some surveys included in the references such as the work by Hu *et al.* at [16].

provide more detailed, precise and exhaustive information about the bands occupied by PUs and SUs, interferences, etc. the price to pay is that a large spectral bandwidth, typically in the order of tens to hundreds of MHz, or even GHz, need to be handled by CR digitizers! This is not feasible due to the power consumption demanded by the spectrum-management block of the CR system. Some other alternatives involve the use of the so-called *compressive spectrum sensing* or any kind of sub-Nyquist sampling in order to relax the requirements of the ASP/RF and very specially the speed requirements of the A/D interface. Most of CR spectrum-management functions can be optimized if they are carried out by an AI engine – as conceptually shown in Fig. 1. Another limitation deals with their legal coexistence with the vast amount of commercial/licensed wireless communication standards available in 5G and incoming 6G mobile networks [8]–[11], [18]. Regardless the way in which such AI engine is implemented, i.e. either by embedded software, hardware or an hybrid way, an efficient computing strategy must be used to make CR-based mobile terminals feasible in terms of energy, cost and practical implementation.

IV. EFFICIENT COMPUTING FOR CR/AIoT DEVICES

In addition to the communication subsystems, CR/AIoT devices and networks will need also to increase their computing capabilities for the huge volumes of information being handled. In many cases, these devices will require to process the sensed information in the shortest possible time and in a ubiquitous way, i.e. without being able to communicate with a remote server, and the minimum energy consumption [12]. Conventional processors based on von Neuman computer architectures are inefficient to perform the tasks required by CR/AIoT nodes. This has prompted the exploration of alternative computing paradigms to implement the AI engine embedded in CR transceivers. First approaches are based on the so-called Machine Learning (ML) and Deep Learning (DL), which are in turn based on the use of algorithmic models – mostly implemented in software and inspired in Artificial Neural Networks (ANNs) – successfully used nowadays for image and voice recognition [35]. The approach here is to extend the use of ML/DL and ANNs to automatize the SS functions required by CR devices [18], [36]–[40]. Let us revisit some basic concepts about ANNs first.

A. Artificial Neural Networks: Basics and Main Topologies

Essentially, an ANN is a computing system formed by the interconnection of layers of units or nodes called *artificial neurons*, which are inspired by the neurons in a biological brain. Similarly to biological neural systems, artificial neurons establish connections among them by means of synapses, so that they can transmit (electrical) signals to other neurons. These connections or synapses are represented by real numbers or *weights*, so that the output of each neuron in an ANN is computed as a (nonlinear) function of the sum of its inputs, i.e. those neurons connected to that neuron. The behavioral model of ANNs adjusts the values of the connections by increasing
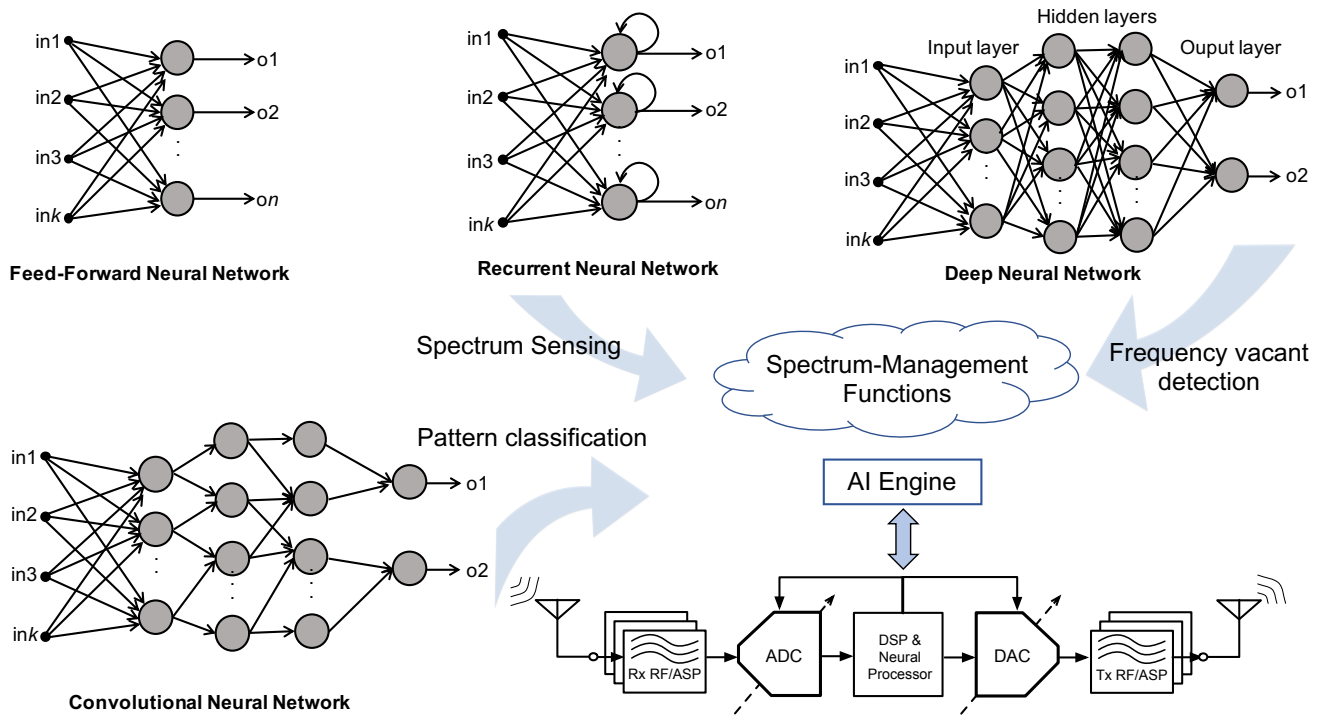
Fig. 7. Main ANN topologies and their application to implement spectrum-management functions in CR systems.

or decreasing the weights, depending on the strength of the synapse, i.e. the signals at a given connection [41], [42].

The generic concept of an ANN can be implemented in many different ways, either in software or hardware or as an hybrid form. Fig. 7 illustrates some of the most common ANN topologies and their potential application to CR systems. Those called generic ANNs – where synaptic weights are trained by using examples – can either be feedforward or recurrent, and are usually associated to applications like artificial vision or voice recognition, where logic programming presents some limitations. The so-called Deep Neural Network (DNN) has at least more than one hidden layer of neurons and it operates in a feedforward way. These ANNs use costly offline training methods which require huge amount of datasets. They also present very good performance for some tasks like face recognition, movement detection, etc. Another topology of ANNs – shown in Fig. 8 – is the so-called Spiking Neural Network (SNN) [43]. In this type of ANNs, neurons update their state only when they receive an input spike – in a similar way as it happens in biology – and there is a temporal correlation between spikes, which becomes crucial for the correct modeling of these kinds of ANNs [41], [42].

There are many other classification criteria of ANNs. One of then is the degree of connectivity of their neurons, so that ANNs can be divided in fully-connected ANNs – where each neuron in a given layer is connected to all neurons of the remaining layers in a feed-forward way – or Convolutional Neural Networks (CNNs), where each neuron is connected to a given subgroup of neighboring layers in a projective/receptive field (see Fig. 7). Another classification criterion deals with the way ANNs are trained, thus dividing ANNs into supervised-

learning, unsupervised-learning or self-learning, depending on the data provided to the ANN to get them trained. Finally, another criterion deals with the implementation itself, which can be either in software – by using many diverse language programs such as Python, C, MATLAB, etc. – or in hardware, either in FPGAs or embedded in a chip.

B. Neuromorphic Computing

One of the ANN approaches that is gaining more and more relevance in the last years is the so-called *neuromorphic computing*, which is inspired by the information processing of the human brain [44], and allows DL algorithms to be implemented in hardware instead of software [45]. This is the case of the TrueNorth processor, designed by IBM in 28nm process [46] – with a high energy efficiency of 26 pJ per synapse – making it viable for a broad spectrum of commercial applications. Another milestone is the Loihi chip, developed by Intel in a 14nm technology, with the capacity to emulate 130,000 artificial neurons [47]. Neural computing is also beginning to be implemented in modules embedded in conventional processors to perform very diverse ML functions. For example, the A1X Bionic series processors – developed by Apple for their mobile devices and more recently in their M1X series processors included in recent generations of their computers and iPads – incorporate a neural computing module, which can perform several billion operations per second in a more efficient way than their von Neumann counterparts. Some other best-known neuromorphic chips are Neurogrid [48] and BrainScaleS [49], to cite a few. A comparison of these chips based on specifications like technology, feature size, number
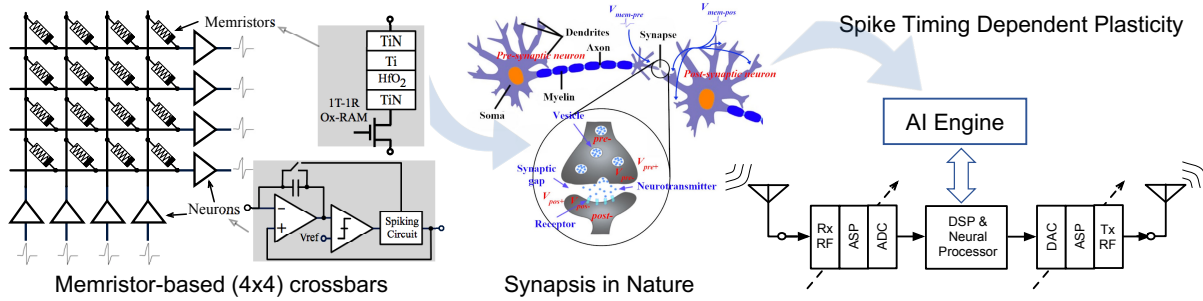
Fig. 8. Illustration of spiking neural networks based on memristive-based crossbars and their application to neuromorphic processors for AI-managed CR.

of transistors, number of neurons, number of synapses, energy, etc. can be found in literature – see for instance [50].

Another promising technology – still in its infancy – consists of emulating synapses by memristors. As well known, Prof. Leon Chua postulated the existence of a *fourth circuit element*, which he coined as 'memristor' in the early 70s [51], although it was not until 2008 when HP labs demonstrated the physical existance of this element [52]. Among its multiple applications, it has been demonstrated that memristive devices can emulate synapses in ANNs and they can be combined with CMOS neurons in a 3D chip implementation. However, one of the limitations to realize general-purpose neuromorphic processors is their scalability, so that they are capable of emulating SNNs – conceptually shown in Fig. 8 – with the required computational capacity and feasible power consumption, although recent research studies demonstrate that using some circuits and systems techniques – like offset calibration – are promising approaches to increase the scalability of memristor-based neuromorphic processors [53].

C. Application of ANNs to AI-managed CR Systems

In spite of the mentioned limitations, some recent studies suggest the possibility to use ANNs and AI/ML technologies to manage the signal processing and performance metrics of the communication systems embedded in IoT nodes in order to implement the CR concept in 5G mobile systems and beyond. As mentioned above, although general-purpose neuromorphic processors are still far from reality, the need of more efficient ubicuos computation requirements opens the doors to look for alternative computing paradigms. Indeed, in the last years, there has been an increased interest in applying learning-based techniques, such as DL/ML, to optimize the management of the electromagnetic spectrum – a core function in CR systems as described in previous sections. A detailed analysis of the multiple reported approaches is well beyond the scope of this article, but the interested reader can find excellent surveys and overviews published in literature [17], [54], [55]. Instead, let us consider here some applications of ANNs to SS-based CR transceivers to illustrate the big picture and envision the potential applications of AI/ML to automatically manage the performance metrics of CR transceivers, and to identify the optimum way to manage the information in terms of frequency spectrum occupancy, noise, interferences, battery status, or any other performance metric [8], [17], [36], [38], [39], [54]–[58].

Although AI-managed engines embedded in a SoC solution for CR transceivers are still far from an actual implementation, there are some interesting approaches which show the way on how the use of learning-based spectrum-driven strategies can be successfully applied to analyze and manage the spectrum in CR nodes and networks. Some authors in [56] show how DL algorithms implemented in CNNs can be applied at the physical layer to address problems such as modulation recognition. The same approach is followed to radio fingerprinting [17] and Medium Access Control (MAC) [59]. In the majority of cases, a collection of signal stimuli is extracted from spectrum data, stored in the cloud and used as training models for the AI engine [17]. This approach may work well for some functions needed in SS-based CRs such as power management, dynamic spectrum access and any other task requiring the identification and classification of some spectrum features. However, it is not clear how this procedure can be applied in practice to effectively address real-time problems. A very promising approach is based on translating the identification problem of frequency holes to a time series prediction problem. To solve these kinds of problems, the so-called Recurrent Neural Networks (RNN) have been used for decades and more recently, a specific type of RNN called Long Short-Term Memory (LSTM) networks has been proposed to be specially suited to predict temporal evolution of data [60].

LSTM networks are one of the best ANN architectures to predict the future occupation of arbitrary frequency bands in a CR-based system, so that using the predictions provided by the LSTM network, the CR-based device can take a decision to use the less occupied band and tune dynamically CR transceiver design parameters to transmit/receive the information through that frequency band [60], [61]. Another open question is the real implementation of the AI engine, either as embedded software or as a specific hardware block, implemented either in an FPGA or in the same chip together with the rest of the CR transceiver. This is still a matter of research, and there are many opportunities of designs innovations in this field. The efficient implementation of CR nodes will also demand an increase of circuit-level programmability in order to adapt the transceiver specifications to the performance metrics set by the AI engine according to the information sensed from the electromagnetic environment. This is specially critical for the ASP/RF subsystem and digitizers, as discussed in next sections.
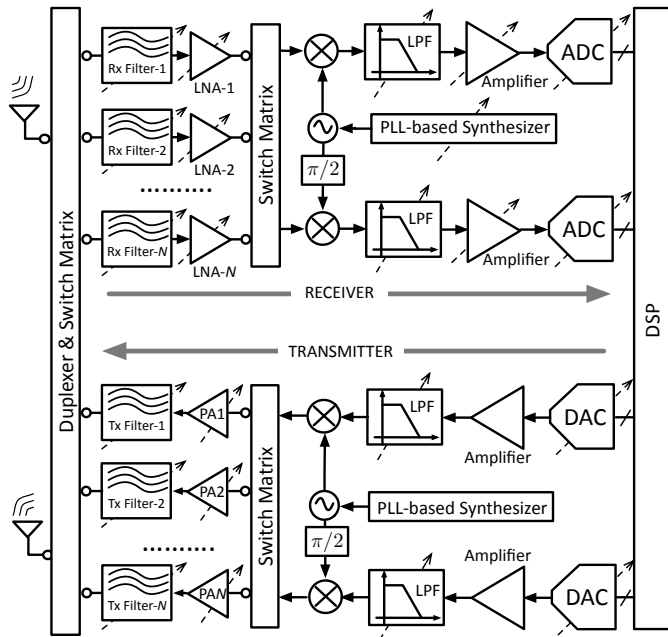
Fig. 9. Multi-standard transceivers based on switchable RF front-ends.

Fig. 10. Fully programmable multi-standard (direct-conversion) transceivers.

V. PROGRAMMABLE AND MOSTLY-DIGITAL DIGITIZERS – KEY TECHNOLOGY ENABLERS FOR CR TRANSCEIVERS

The system-level trends and challenges discussed in previous sections are transferred to the circuit and physical level, by demanding innovative solutions to implement efficient Integrated Circuits (ICs) to put SDR/CR concept in practice. As stated in Section II, multi-standard transceivers embedded in last-generation cellular phones tend to reduce the analog/RF content, although it is still a common approach to implement such multi-mode transceivers by using single down/up conversion scheme as conceptually depicted in Fig. 9. This architecture eliminates the need for both Intermediate-Frequency (IF) and Image Reject (IR) filtering and requires only a single oscillator and mixer, which increases hardware sharing. Moreover, the most common situation in practice is that, separate (switchable) RF front-end paths are used for different standards, whereas a single, digitally-programmed baseband section is shared by all of them.

One of the major design challenges is to make as many RF building blocks reconfigurable as possible, so that the ideal scheme should be as that conceptually shown in Fig. 10. However, even this fully-programmable transceiver scheme would be feasible, there are several issues that should be also taken into account. On the one hand, multi-standard transceivers must be able to support different standards concurrently. For example, several standards operate in a concurrently way at a given time. Thus, it is common to use simultaneously cellular standards (GSM, UMTS, LTE, etc.) with other wireless communications such as WLAN, Bluetooth, GPS, etc. The challenge therefore lies in designing a reconfigurable cellular transceiver that can meet many diverse requirements without replicating the hardware and increasing the cost/size. The trend nowadays is towards implementing the DSP, the programmable A/D/A interface and most of the reconfigurable ASP/RF signal
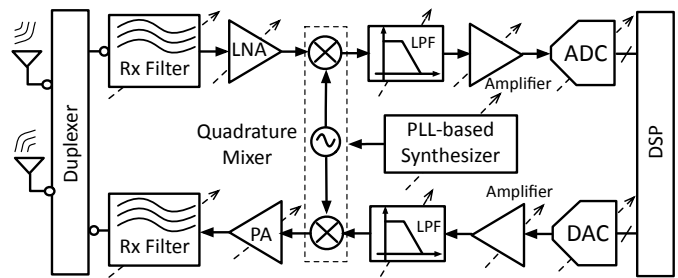
processing in an advanced CMOS technology process, while the rest of components, basically the antenna interface and RF front-end components, can be implemented in *RF-friendly* III-V semiconductor technologies, such as GaAs or SiGe [62].

One of the key technology enablers to make SDR and CR a reality is to translate most of the signal processing from the analog to the digital side. This strategy makes the A/D interfaces one of the most critical building blocks and design bottlenecks of incoming generations of wireless (SDR/CR) transceivers. As stated earlier, the boundary between the analog and digital domains has increasingly shifted to the antenna, with the subsequent benefits from technology downscaling and programability – a very important feature required by SDR/CR systems. Indeed, in an ideal SDR/CR transceiver, there would theoretically be no need for any ASP other than that necessary for the corresponding ADC in the receiver and the Digital-to-Analog Converter (DAC) in the transmitter.

In an ideal SDR/CR system, most of the signal processing could be implemented via software in the DSP. However, such a SDR/CR end-device is unfeasible in practice, since it would imply the need for ADCs and DACs with specifications which are well beyond the state of the art. Roughly speaking, the A/D interface would need to digitize signals placed at carrier frequencies within the GHz range with signal bandwidths of tens or even hundreds of MHz and effective resolutions of 10-12 bit, or even more, depending on the communication standard. These demanding requirements should be fulfilled with the minimum amount of energy to maximize the battery life, what in many cases would involve consuming only a few μWs. These specifications can be relaxed by means of an ASP/RF and signal conditioning interface between the antenna and the digitizer (see Fig. 10). The rest of the paper focuses on the receiver path of CR transceivers, and puts emphasis on the ADC as one of its key components and technology players enabling CR systems. State-of-the-art ADC architectures as well as some key reconfigurable, mostly-digital/digital-based analog circuit techniques are revisited, looking at the features demanded by AI-managed systems.

A. An overview of the State of the Art on ADCs

Fig. 11 represents the performance of state-of-the-art ADCs in terms of their main specifications, i.e. the digitized signal bandwidth, B_w, as a function of the resolution, quantified by the Effective Number Of Bits (ENOB). The conversion region covered by $\Sigma\Delta$Ms is comparable to the rest of (Nyquist-
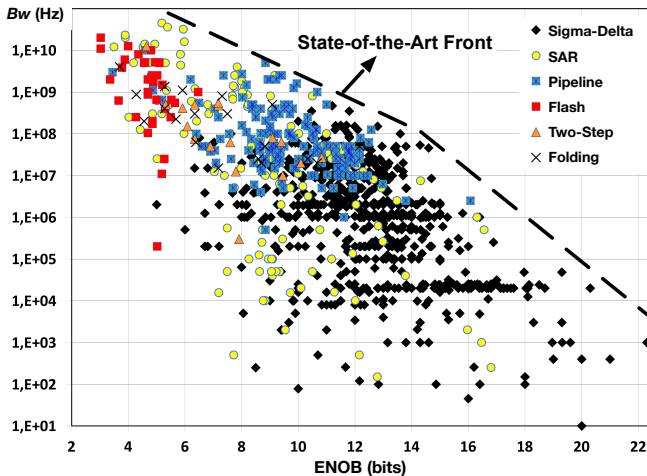
Fig. 11. Conversion region (*aperture plot*) of CMOS ADCs [64].

Fig. 12. Evolution of energy plot of CMOS ADCs over the last three decades.

rate) ADCs, which is in turn mostly dominated by Successive Approximation Register (SAR) and Pipeline ADCs. These three techniques – or a combination of them – cover a vast range of applications [63], [64].

Two different state-of-the-art *fronts* can be identified in Fig. 11. One front – mainly dominated by $\Sigma\Delta$ ADCs – goes from low-frequency (tens/hundreds of Hz) and high-resolution ($<$ 21 bit), to medium-high frequency (tens/hundreds of MHz) and medium-high resolution ($<$ 14bit). The other front is dominated by SAR and Pipeline ADCs, and goes from hundreds of MHz and medium-resolution (in the order of 10 bit), to dozens of GHz and low-resolution (up to 5-6 bit). The fastest ADCs are the Flash architectures – based on a parallel A/D conversion using a bank of 2^N comparators, with N being the effective resolution. This resolution is limited by the power consumed by the exponential number of comparators. In contrast, other types of ADCs such as semi-Flash (two-step), Pipeline (multi-step), SAR and $\Sigma\Delta$M ADCs relax the energy-vs-resolution trade-off by relying their performance on a *divide and conquer* strategy. Essentially these ADCs trade the precision of their (analog) building blocks by (digital) signal processing. As a result, a more efficient digitization is achieved in terms of the *conversion energy*, and the price to pay is a reduction in the comparison speed as compared to fully-parallel Flash ADCs [63]–[67].

The energy consumed per conversion in an ADC, can be quantified as $E \equiv P/f_{\text{snyq}}$, where P is the power dissipated and $f_{\text{snyq}} \equiv 2 \cdot B_w$, stands for the ADC Nyquist rate or output rate. The conversion energy has been reduced over the years, by pushing state-of-the-art ADCs foward. This is illustrated in Fig. 12, which shows the evolution of the energy per conversion of state-of-the-art ADCs within the last three decades. This picture – commonly known as an *energy plot* – represents graphically the aforementioned trade-off between resolution and conversion energy [68]–[70]. It is clear from Fig. 12 that ADCs have benefited from technology downscaling to make more and more efficient digitization.

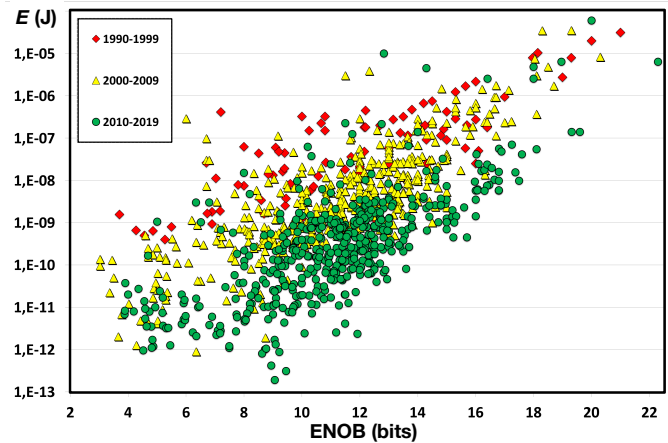AI-managed CR-based transceivers would require energy-efficient ADCs with a high degree of programmability to digitize very diverse signal types, while handling the environmental interferences and noisy signals, battery status, spectrum band occupancy, etc. ADCs based on $\Sigma\Delta$Ms, noise-shaping SARs, and hybrid SAR/$\Sigma\Delta$M/Pipeline architectures are – a priori – good candidates to implement highly programmable A/D interfaces. Moreover, prompted by its inherent robustness provided by the action of noise-shaping and feedback, $\Sigma\Delta$M-based digitizers are among the best ADC topologies to merge with RF/ASP front-end circuits as well as with the ANN engine that control the operation of CR/SDR transceivers [71].

The use of $\Sigma\Delta$Ms in some spectrum-management functions such as energy detection [72], RF digitizers [73]–[79], as well as their suitability to embed RF signal processing as Image-Reject (IR) filtering [80], are just some examples of the versatility and suitability of $\Sigma\Delta$M circuits and systems techniques to design incoming AI-managed CR digitizers. There are also some hybrid ADC architectures such as $\Sigma\Delta$M-SAR [81], Noise-Shaping SAR [82]–[84], SAR-Pipeline [85], [86], or GHz-rate Continuous-Time (CT) Pipeline ADCs [87] – just to cite a few – suited to implement some spectrum-management functions in CR systems [88]. The remaining sections mainly focus on some $\Sigma\Delta$M-based architectures and circuit strategies to implement highly programmable, *digital friendly* digitizers for AI-managed CR-based receivers.

B. $\Sigma\Delta$M-based Receivers for SDR/CR

Over the years, more and more CT-$\Sigma\Delta$Ms are demonstrating to be a competitive solution for the implementation of power-efficient ADCs operating in the GHz range [74]–[76], [89]–[99]. The use of CT loop filters make more feasible the development of *digital-intensive* RF transceivers [100] and SDR, often referred to as $\Sigma\Delta$ *receivers* [101]. One of the most common topologies in mobile handsets consists of using a Direct Conversion Receiver (DCR) like the one conceptually depicted in Fig. 13(a). This receiver is made up of an ASP – made up of a LNA, a mixer, and a baseband filter – followed by a Low-Pass (LP) CT-$\Sigma\Delta$M. The latter benefits from their CT circuit nature to merge some RF functions like out-of-band blocker/interfering-rejection filtering, frequency-mixing process, channel-selection and antialiasing filtering [80], [98],
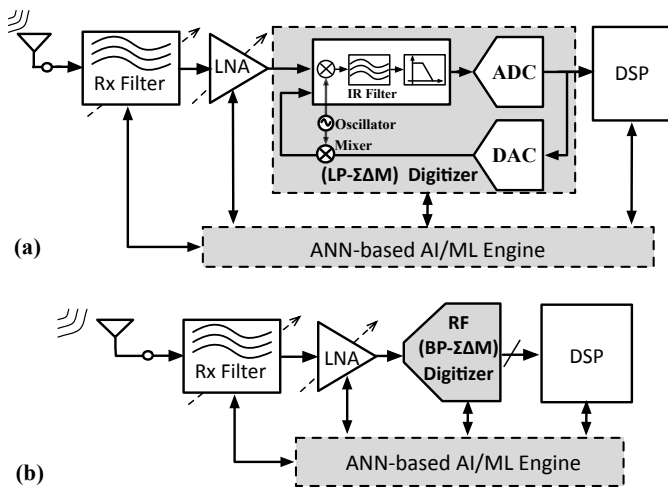
Fig. 13. AI-managed ($\Sigma\Delta$M-based) receivers for CR systems: (a) Low-Pass (LP) $\Sigma\Delta$M with embedded IR filter and mixer. (b) RF (BP-$\Sigma\Delta$M) digitizer.

[102]–[113]. These functionalities can be embedded within the $\Sigma\Delta$M feedback loop, thus yielding to more compact RF receivers [64]. However, the analog content is still too complex to be controlled by an AI engine, where a mostly-digital approach is more suited to merge it with ANNs.

An alternative trend towards SDR receivers is based on placing GHz-range BP CT-$\Sigma\Delta$Ms as close as possible to the antenna, as illustrated in Fig. 13(b), yielding to the so-called *RF-to-baseband converters* or *RF-to-digital converters* [92], [94], [101], [114]–[121]. Although this topology is close to the ideal implementation of SDR [29], its practical application is mostly limited by the unfeasible *power-hungry* requirements demanded by the GHz-clocked ADC. These specifications can be patially mitigated by using some techniques such as embedded out-of-band filtering [101], [120], frequency-translating [116], [120] and *undersampling* or *subsampling* [94], [114], [115], [122], [123].

For BP-$\Sigma\Delta$ ADCs intended for RF conversion, tuning range is also a concern. The majority of RF-to-digital BP CT-$\Sigma\Delta$Ms use a fixed center or *notch frequency* and a programmable frequency synthesizer. This issue has motivated the interest for reconfigurable/programmable BP-$\Sigma\Delta$Ms with wide tunable notch frequency [76], [92], [124]–[126]. Another limiting challenge is associated with the design of loop filters in the GHz range, which need to achieve a high-quality and accurate resonance. LC tanks are great from a power and linearity perspective but typically support only an octave of range, whereas active-RC resonators can be widely tunable but require amplifiers with high gain at the ADC's center frequency [71]. These limitations have motivated exploring alternative signal processing techniques, such as translational circuits, polyphase or N-path filters [127]. Although the idea of using N-path filters in BP $\Sigma\Delta$Ms is not new [128], there has been a *resurgence* of these signal processing techniques to implement BP-ADCs, by combining NS-SAR and $\Sigma\Delta$M techniques [129]. Indeed, these techniques can be combined with either active or passive downconversion structures embedded into the modulator loop filter as conceptually shown

in Fig. 13(a), in order to achieve the required received linearity and sensitivity [32], [101], [130], in some cases without needing integrated inductors [130].

The $\Sigma\Delta$M-Rx architectures depicted in Fig. 13 are – a priori – among the best candidates for SDR/CR. The main advantage of using a BP-$\Sigma\Delta$M is its high degree of programmability, since virtually all signal processing is done digitally. The biggest drawback lies in the accuracy required for analog blocks, specifically the LNA and the RF-to-digital converter [64]. However, the use of suitable synthesis methodologies [125], combined with circuit-level optimization and RF/ASP circuit tuning strategies can reduce the power consumption to the order of a few mW [126] or even μW [131]. However, even though the tuning range can be increased, the specifications required for the ADC are still well beyond the state of the art. The required Dynamic Range (DR) can be however achieved by the ASP/RF subsystem. This imposes also significant trade-offs in terms of the signal saturation and sensitivity of the receiver, which must be handled while keeping the requested programmability to implement CR functions.

Although the performance of some $\Sigma\Delta$M RF digitizers like that shown in Fig. 13(a) is still well short of what is needed for being included in SDR/CR end-devices, the state of the art on ADCs look at different circuits and systems techniques to further reduce the RF/ASP content and make CR-based transceivers more and more programmable via software to easy their control an AI engine [64]. Another alternative – based on a DCR in which out-of-band blockers are embedded in the $\Sigma\Delta$M loop filter– takes the advantage of the feedback nature of the $\Sigma\Delta$M to reduce the sensitivity of the analog circuitry to non-ideal effects [80]. Moreover, the use of some techniques like either multi-channel BP-$\Sigma\Delta$M [79] can further enhance the operation of $\Sigma\Delta$M-Rx for SDR/CR applications.

Regardless the topology of the CR-based receiver, the overall system must work under the control of the AI/ML engine. This subsystem – which implements the spectrum-management functions required by the CR terminal – can be implemented in diverse ways. It can be synthesized either in hardware as an off-chip (FPGA-based) part, or as an on-chip dedicated module – which would need its own ASP and A/D interfacing – or as a software embedded in the DSP. If dedicated hardware is used by the AI engine, this would require low/medium bandwidth ADCs in the receiver. Alternative, in case of AI algorithms embedded in a DSP, a wideband digitizer would be needed. Both approaches – still a matter of research – have their pros and cons in terms of hardware complexity, power consumption, programmability, etc. and they have a significant impact on the performance metrics of the whole CR end terminal [72], [132], [133].

C. Digital-Friendly Analog Circuits for AI-managed $\Sigma\Delta$Ms

Fuelled by the mentioned need of an earlier digitization, there is a trend in recent years to either complement or replace more and more ASP building blocks by the so-called digital-assisted, digital-friendly analog solutions – some of them highlighted in the conceptual diagram shown in Fig. 14. A clear example is the use of CMOS inverters for the realiza-
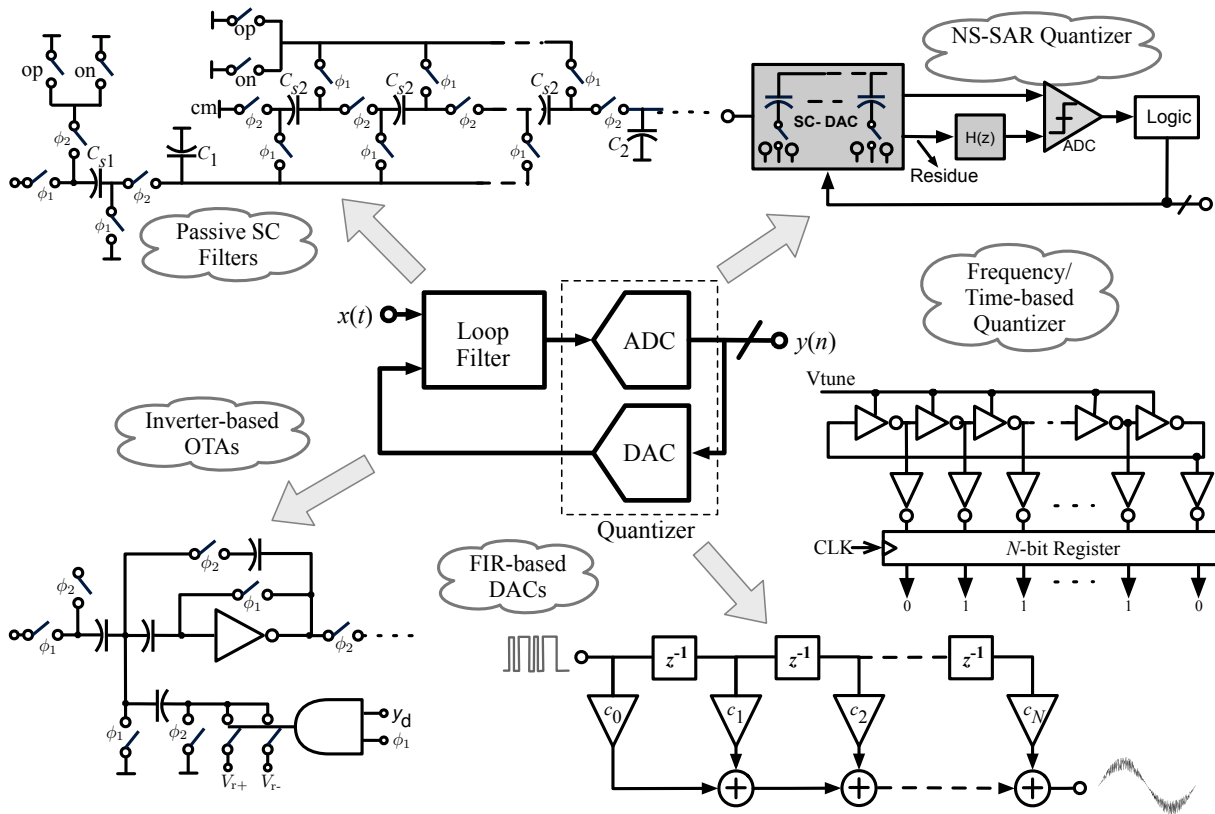
Fig. 14. Scaling-friendly analog circuit techniques for mostly-digital $\Sigma\Delta$M and hybrid $\Sigma\Delta$M/Nyquist-Rate ADCs.

tion of Operational Transconductance Amplifiers (OTAs), as originally proposed by Prof. Bram Nauta in the late 1980s. Since then, there has been an increasing interest to apply this technique to the implementation of GHz-range filters, as well as ASP/ADCs, which may obtain greater energy efficiency for the required gain performance and bandwidth [71]. At the same time, more and more digital circuitry is being embedded to improve the performance of ASP circuits, by means of calibration, tuning, etc, that try to alleviate the limitations of nanometer CMOS analog circuits [134]. These features can be enhanced by the action of an embedded AI engine to manage the operation of the analog/digital interface [20].

In spite of their potential benefits, inverter-based OTAs offer lower performance metrics such as robustness over PVT variations, impact of circuit parasitics, limited dc gain, etc. These limitations have motivated some authors to proposed improved versions of inverted-based integrators to implement both Switched-Capacitor (SC) and CT $\Sigma\Delta$Ms [134]–[139]. The use of digital-based ASP is a very promising strategy for the implementation of highly programmable digitizers, and it is expected that the use of these circuit techniques might benefit from technology downscaling in the next few years [140], [141].

Hybrid Active/Passive & Amplifier-Less $\Sigma\Delta$Ms: Another alternative to reduce the number of OTAs consists of replacing some active building blocks with passive-RC networks. The drawbacks of this approach are the loss in loop-filter gain, increased thermal noise as well as a higher sensitivity to

parasitics. Although the idea is not new, passive RC networks are becoming a popular circuit solution for the implementation of both CT- and SC-$\Delta\Sigma$Ms [93], [121], [142]–[148]. Hybrid active/passive analog filters can be applied to BP-$\Sigma\Delta$Ms for RF digitizers. However, due to their higher operating frequencies – in the GHz range – RF digitizers present larger sensitivity to mismatch, technology process variations, as well as the degradation caused by parasitics – specially critical to achieve a high quality factors of integrated inductors in loop-filter resonators. Indeed, hybrid active/passive circuits could be properly combined with other kinds of hybrid circuit techniques – such as CT/SC $\Sigma\Delta$Ms– to take advantage of the different circuits involved, i.e. faster operation of CT circuits and lower sensitivity of SC circuits to errors [147]–[155].

Hybrid $\Sigma\Delta$M/Nyquist-rate ADCs: The performance of $\Sigma\Delta$Ms can be enhanced by using high-resolution quantizers implemented by energy-efficiency SAR or Pipeline ADCs. This idea – originally proposed in [156] to implement hybrid Pipeline-$\Sigma\Delta$ ADCs – can also increase the reconfigurability and programmability of the resulted ADC. Indeed, there has been a number of hybrid $\Sigma\Delta$M-Nyquist ADCs featuring a competitive performance in very diverse application scenarios [82], [157]–[166]. In the majority of cases, the basic strategy followed by hybrid $\Sigma\Delta$M/Nyquist ADCs consists of replacing (power and area)-hungry Flash quantizers, by another type of Nyquist-rate ADCs, such as pipeline [156], [157], [161], [164], two-step flash [161], SAR [82], [159], [163], [165], [166], cyclic [158], [160] and integrating ADC [162].

Incremental $\Sigma\Delta$ ADCs (I-$\Sigma\Delta$ ADCs) can also be considered as hybrid $\Sigma\Delta$M/Nyquist ADCs. These kinds of ADCs use oversampling and noise-shaping, but reset the loop-filter integrators and digital filters after each conversion [167]. These features allow these ADCs to be especially efficient in low-frequency high-resolution applications like sensor interfaces using SC circuits [168] and other applications requiring to process multiplexed low-frequency signals with high-resolution [169]. Some other I-$\Sigma\Delta$ ADCs are based on *multi-step* architectures or the so-called *extended counting* [36], which in turn can benefit from the hardware/stage-sharing techniques. These ADCs consist of a front-end I-$\Sigma\Delta$ ADC and a back-end stage made up of a Nyquist-rate–which can either be a SAR or a Cyclic ADC– to digitize the residue voltage of the front-end I-$\Sigma\Delta$ stage [170]. Although I-$\Sigma\Delta$ ADCs have been used in low/medium frequency applications, the use of CT circuit techniques and the combination with either SAR or Pipeline ADCs is allowing their application to wideband digitizers and can also be suited to implement reconfigurable ADCs [171]–[173], which can be handled by ANNs in CR/SDR.

Time-based Quantization: Another *scaling-friendly* approach – suitable for medium-low resolution (< 10bit) and GHz-range speed required in RF digitizers – is that based on time coding by using Voltage Controlled Oscillators (VCOs), rather than using amplitude quantization. The idea consists of translating the quantized information in the amplitude domain to the time domain by means of a voltage-to-frequency conversion. This can be performed by a VCO circuit as conceptually depicted in Fig. 14, that shows one of the first implementations of this concept [174]. The principle of operation behind this approach relies on the use of a ring oscillator to count the number of edges within a given time period. The result is directly related to the input signal, thus obtaining a digital representation of the amplitude. In addition to their higher speed, they can operate at supply voltages below 0.5V, while reducing the analog content, which makes them highly scalable. Moreover, VCO-based quantizers provide an implicit first-order noise-shaping filter due to their inherent differentiator operation required to implement the frequency-to-voltage conversion in the digital domain [100], [174]–[190].

The main limitation of VCO-based quantization is the inherent nonlinearity of the voltage-to-frequency conversion, requiring the use of either calibration or linearization techniques [180]–[182], [191], [192]. Another strategy consists of embedding VCO-based quantizers in the back-end stage of a cascade[2] $\Sigma\Delta$M, such that their nonlinearities can be attenuated by the noise shaping of precedent stages in the cascade [193]. Indeed, this idea has been used in other types of two-step hybrid $\Sigma\Delta$/Nyquist-rate ADCs [82], [194]. An alternative to VCO-based quantizers consists of using pulse-width modulation (PWM) [195], [196] and a Time-to-Digital Converter (TDC) that generates a time-quantized representation of the signal. Indeed, embedded TDCs have been succesfully implemented by a number of recent $\Sigma\Delta$Ms [197]–[203]. Another approach is based on the so-called Gated Ring Oscillators (GROs), which can attenuate the nonlinearity of VCOs and

be combined with active-RC integrators, thus benefiting from both amplitude- and time-based circuit techniques [204].

Finite Impulse Response (FIR) Feedback DACs: Regardless the ADC quantization is realized in either amplitude or time domain, it presents a number of inconveniences in terms of analog circuit complexity and the nonlinearity caused by mismatches in the feedback DAC. To address this problem, some authors propose the use of alternative implementations of the modulator feedback DAC waveforms–such as a DAC with a Finite Impulsive Response (FIR) [91], [93], [205], [206]. The idea –originally proposed in [207] and conceptually illustrated in Fig. 14 – is to feedback a filtered version of the single-bit quantization output, such that due to the high-frequency attenuation of the FIR filter, the DAC output is a multi-level waveform. This way, using a single-bit ADC and a FIR DAC allows to obtain the low-jitter sensitivity and high linearity of a multi-bit $\Sigma\Delta$M, while keeping the simplicity and robustness of single-bit $\Sigma\Delta$Ms as well as a reduced analog circuit content [206], [208]. Moreover, the combination of Time-Interleaved (TI) topologies [209] and FIR DACs is a promising approach to implement $\Sigma\Delta$M-based GHz-range and RF-to-digital converters [210]. Thus, FIR DACs reduce the analog content of the ADC and make it easier to digitally control its specifications by using an ANN algorithm as pretended in AI-managed digitizers.

Fully Depleted Silicon-on-Insulator (FDSOI) Technologies: The aforementioned *digital-assisted* analog techniques can benefit from the use of nanoscale technologies such as FDSOI. This process is postulated as one of the key technologies for mobile telecom applications, thanks to its better performance than bulk CMOS in terms of transit frequency (f_T), transconductance efficiency (gm/I_d), reduced impact of passive parasitic elements, as well as improved noise isolation. Another great potential of FDSOI is its enhanced body effect by a wider tuning of the threshold voltage, V_{th}, which makes it possible to reduce the voltage ranges to supply voltages in the order of a few hundreds of mV [211], thus increasing the performance metrics of ASP in communications, including the enhanced linearity of frequency/time-based circuits [212].

VI. CIRCUIT EXAMPLES: PROGRAMMABLE $\Sigma\Delta$MS FOR AI-MANAGED CR DIGITIZERS

As an application of the circuits and systems techniques discussed above, let us consider two $\Sigma\Delta$M examples and case studies which can be applied to implement mostly-digital, highly programmable digitizers for SDR/CR transceivers. Two circuit examples are shown to illustrate their application in the CR-based receivers shown in Fig. 13, i.e. a DCR receiver with a programmable LP-$\Sigma\Delta$M ADC and a widely tunable BP-$\Sigma\Delta$M for RF-to-digital conversion. In the latter case, an example of how LSTM-based AI engines can be used to manage the electromagnetic spectrum and reconfigure their operation in CR-based receivers will be shown.

A. Reconfigurable SC-$\Sigma\Delta$M for DCR-based SDR/CR systems

Let us consider first the use of $\Sigma\Delta$Ms for the design of reconfigurable baseband ADCs in DCR-based receivers.

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[2]Cascade are also known as multistage noise shaping (MASH) $\Sigma\Delta$Ms.
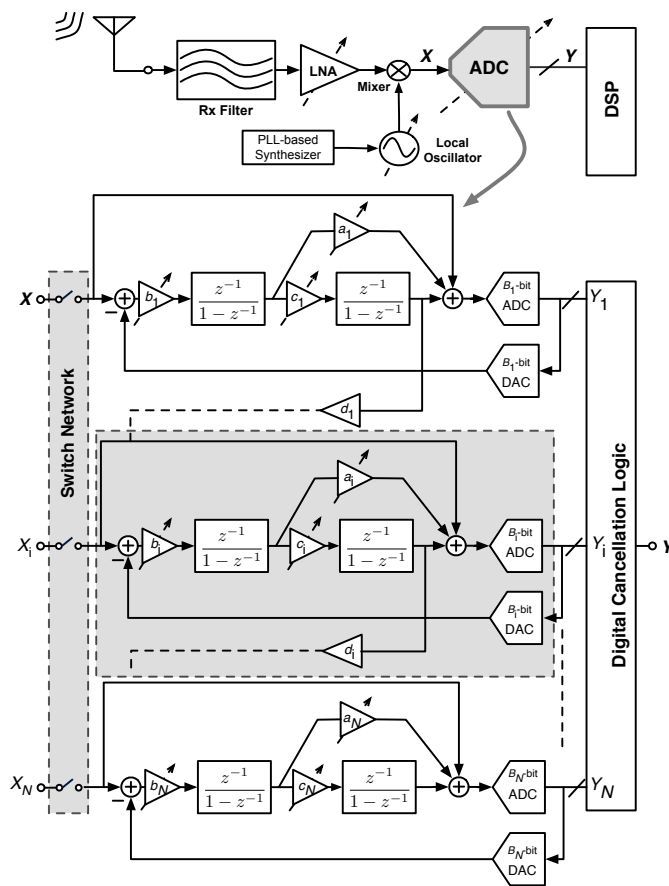
Fig. 15. Programmable MASH SC-$\Sigma\Delta$M for ADCs in CR-based DCRs.

Fig. 16. Programmability at circuit level: switchable SC-$\Sigma\Delta$M stages.

Fig. 13(a) shows the block diagram of such a receiver for SDR/CR, where after being filtered and preamplified, incoming RF signals are downconverted to baseband, where they are digitized by a reconfigurable LP-$\Sigma\Delta$M ADC. In this example, the receiver aims to cover the requirements of diverse wireless standards including in 4G such as GSM, Bluetooth, GPS, UMTS, DVB-H, WLAN, LTE, among others. These standards involve digitizing signals with B_w ranging from hundreds of kHz to hundreds of MHz with an ENOB within 12 to 8 bit, respectively. A Switched-Capacitor (SC) $\Sigma\Delta$M will be considered to highlight its high programability feature – one of the main characteristics required to implement AI-managed CR devices. The required programmable requirements can be addressed by properly reconfiguring a SC $\Sigma\Delta$M with a loop-filter order of $L = 2, 4, 6$, an embedded quantization of $B = 1$-to-3 bit, and an OverSampling Ratio, OSR $\in (10, 200)$ [64], [213]–[215].

Modulator Architecture: The conceptual $\Sigma\Delta$M considered in this example – shown in Fig. 15 – consists of a N-stage MASH topology, where all stages can be made independently switchable according to the desired quantization noise shaping, and the Digital Cancellation Logic (DCL) can be programmed according to the value of L [214]. If a stage is turned off, its building blocks can be powered down to save power. The number of bits of the internal quantizers, i.e., B_i, and/or the OSR can be also reconfigured to increase the flexibility of the ADC. In addition to its reconfigurable characteristics
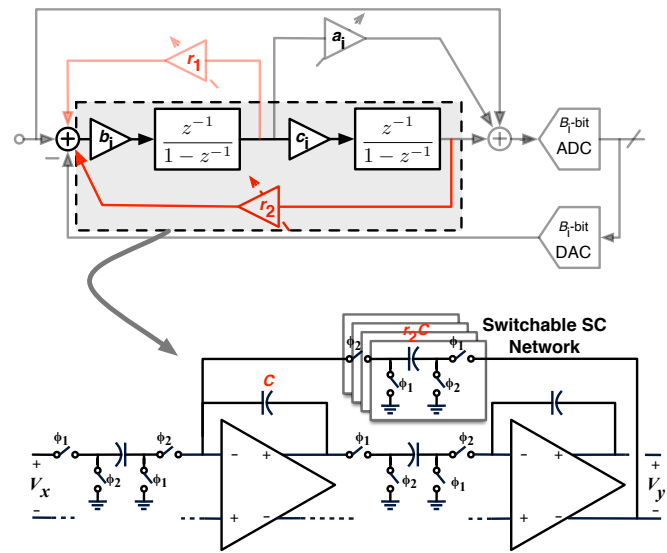
(OSR, L and B), a multimode $\Sigma\Delta$ ADC should be able to digitize signals corresponding to different standards–for instance, GSM and Bluetooth signals and WLAN signal–in a simultaneuous or *concurrent* way. Indeed, concurrency can be also implemented in a MASH $\Sigma\Delta$M, as shown in Fig. 15, where a switchable SC network is used to allow the ADC to be configured as several sub-ADCs, working in parallel–each one processing a different input signal [214].

Programmability at Circuit Level: Several alternative $\Sigma\Delta$M topologies can be considered for the ADC in Fig. 15, by properly combining 2nd-order stages and 1st-order stages in order to guarantee the stability of each sub-modulator [213], [216]. Fig. 15 shows an example based on 2nd-order stages with local *resonators* in the loop filter. This technique allows to place the zeroes of the Noise Transfer Function (NTF) in optimal frequencies to maximize the ENOB. As an illustration, the SC schematic of an intermediate stage with resonation is shown in Fig. 16, where switchable capacitor arrays are used to implement the programmable loop-filter coefficients. This SC-$\Sigma\Delta$M ADC requires additional digital logic blocks – not shown in the figure for the sake of simplicity – in order to implement the main reconfiguration functionalities by means of a set of control signals which are also used to power up/down the different building blocks according to the configuration needed by the ADC for each operation mode. This is an important requirement for the ADC in CR applications where the specifications must be dynamically modified according to the information sensed from the environment.

Scalable Power Circuit Techniques: Reconfigurable ADCs need to be capable to adapt their performance to the specifications of diverse standards with the minimum power consumption. This becomes particularly critical in portable devices such as CR handheld terminals. One of the most common ways to implement this power adaptability is to adjust the biasing of the $\Sigma\Delta$ ADC by means of a programmable master bias current generator [213], [217]–[219], as illustrated in Fig. 17. In this example, reconfiguration is performed by using binary-
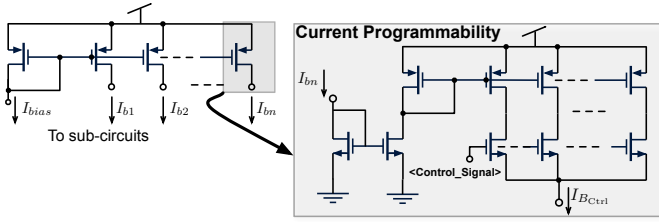
Fig. 17. Programmable master bias current generator.

weighted pMOS current mirrors, and all mirrored currents are selected by control signals, which are in turn applied to the gates of nMOS-based control switches. This way, the electrical characteristics of analog circuits such as loop-filter amplifier metrics – DC Gain, Gain-Bandwidth (GB), Slew-Rate (SR), etc. — can be modified according to the bias current demanded by each building block [215].

Measured Programmable Noise Shaping: As an illustration of the aforementioned programmability circuit techniques, let us consider two $\Sigma\Delta M$ chips designed in 90-nm CMOS intended for SDR [215]. One of them is a 4th-order two-stage (2-2) MASH with 3-level quantization and the other one is a 6th-order three-stage (2-2-2) which includes concurrency, programable local resonation and reconfigurable 3-to-5-level quantization. In both cases, the OSR can be programmed by varying the sampling frequency, f_s, from 40MHz to 240MHz. The noise-shaping of the ADC can be programmed according to required specifications by varying OSR, L or B.

Fig. 18(a) illustrates the capability to digitize different signals simultaneously, i.e. in a concurrent way. This example shows the experimental output spectra of the first and the second stages of the 6th-order $\Sigma\Delta M$ by processing two input sinewaves placed at 20 and 200 kHz, respectively. Fig. 18(b) shows the measured output spectra of the 4th-order MASH SC-$\Sigma\Delta M$ considering different configuration and operation modes, for an input sinewave with an amplitude of -12.2dB below Full-Scale (dBFS). This chip featured a peak SNDR of 72.3-to-48.7dB within 100kHz-to-10MHz, with an adaptive power consumption of 4.6-to-11mW, being at the cutting-edge of the state of the art in reconfigurable ADCs [213]. The programmability features of this $\Sigma\Delta M$, at both architectural and circuital level, make it suitable to be managed by ANN-based AI engines in applications such as CR receivers.

B. Widely-Tunnable CT BP-$\Sigma\Delta Ms$ for RF Digitizers

As stated above, CR-based ADCs require not only digitize GHz signals but also to seamlessly hop from one frequency band to another, according to the information sensed from the electromagnetic spectrum. This feature can be realized by BP-$\Sigma\Delta M$ ADCs with a widely tunable *notch* frequency, f_n, while keeping the required resolution over the digitized band [20], [76]. To illustrate this approach, let us consider a second $\Sigma\Delta M$ chip example, designed in 65-nm CMOS, which consists of a 4th-order loop filter made up of inverted-based Gm-LC resonators and a 4-bit quantizer, conceptually depicted in Fig. 19(a). The loop-filter resonators are based on programmable inverter-based transconductors shown in
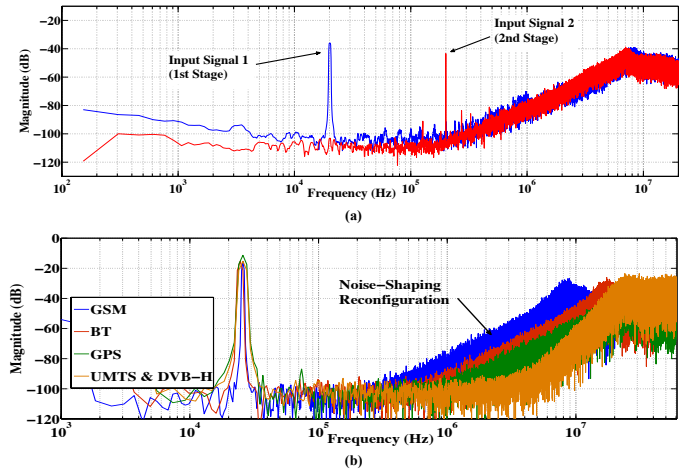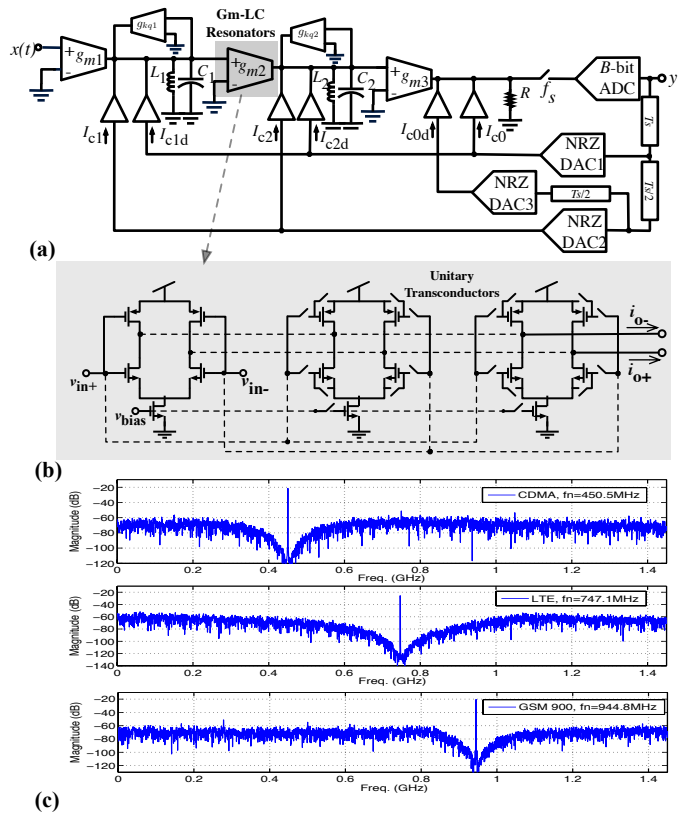

Fig. 18. Programmable noise shaping in SC-$\Sigma\Delta Ms$. (a) Measured output spectra for two concurrent input signals. (b) Measured noise-shaping reconfiguration for different communication standards [213], [215].

Fig. 19. Tunable Gm-LC BP-$\Sigma\Delta M$ RF digitizer. (a) Conceptual schematic. (b) Programmable transconductors. (c) Output spectra for several standards.

Fig. 19(b), which are in turn made up of unitary circuit elements that can be connected or disconnected depending on the operation mode required for the digitizer. This way, the notch frequency can be tuned as illustrated in the output spectra shown in Fig. 19(c). Moreover, the tuning of specifications can be managed by an LSTM network [61] as shown later.

Both system-level and circuit-level reconfiguration techniques are considered to allow the modulator to digitize signals placed at several carrier frequencies, ranging from 450MHz to

950MHz, with a programmable 1.2/2GHz clock rate. Inverter-based switchable transconductors are used to make the loop filter reconfigurable and optimize the ADC performance in terms of robustness to circuit errors, stability and power scalability. Usually, the design bottleneck is not so critical at the circuit level but at the system level, where a proper synthesis and sizing of the $\Sigma\Delta M$ can lead to a more efficient and robust design, while relaxing the required design margins of most performance metrics at transistor level [125], [126].

Increasing the Tunning Range of BP-$\Sigma\Delta M$ RF Digitizers: In order to increase the programmability of the BP-$\Sigma\Delta M$ ADC, loop-filter Gm-LC resonators are realized as switchable multiples of a unitary transconductance element as depicted in Fig. 19(b). The quality factor, Q, of the Gm-LC resonators is enhanced by adding two extra transconductances, $g_{kq1,2}$, which can be calibrated in order to maximize the performance of the modulator. The quantizer is made up of a 4-bit flash ADC in the forward path and a current-steering FIR-DAC in the feedback loop. The modulator was synthesized by applying a CT-to-DT transformation to a BP DT-$\Sigma\Delta M$ with a NTF, considering input signals with $B_w = 40$MHz placed at a programable notch frequency, from $f_n = 450$MHz to $f_n = 950$MHz. As discussed in more detail in [64], [125], the Schreier's toolbox can be used to synthesize the NTF for a given value of f_n. Once the ideal NTF and STF have been determined, the best values of the loop-filter coefficients are selected in order to optimize the performance of the BP CT-$\Sigma\Delta M$ in terms of robustness and stability, while maximizing DR and the SNDR with the minimum power consumption[3].

Circuit-level Reconfiguration Techniques for RF Digitizers: In order to put in practice the system-level programmability required in CR systems, proper reconfigurable circuits are needed. To this end, mostly-digital circuit implementations are very suitable, as for instance the use of switchable inverter-based transconductors to make Gm-LC resonators (Fig. 19(b)). Inverted-based unitary transconductors are simple and modular, thus increasing the flexibility and programmability of the RF digitizer, while minimizing its power dissipation. In order to adjust the values[4] of the requested loop-filter coefficients with a higher accuracy, different values of the unitary transconductance, $g_{mu} = 100\mu$A/V, are used, namely: g_{mu}, $1/2g_{mu}$. The same strategy is followed for g_{qu}, where $1/2g_{qu}$ $1/4g_{mu}$ are also used. These values can be easily changed by properly scaling the value of the tail current, $I_{bias} = 12.5\mu$A, of the unitary transconductors as well as the sizing. Another reconfigurable circuit strategy consists of programming the resonant frequency by using switchable unitary capacitors connected by switches, which are in turn digitally controlled in order to program the value of f_n required for the BP CT-$\Sigma\Delta M$ to work in each operation mode. Different values of unitary capacitances are used to increase the granularity of the overall capacitance value. Additionally, a pMOS-based varactor is also used to fine-tune the resonance frequencies required by each operation mode [64], [126].

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[3]The whole design methodology is described in [64], [126].
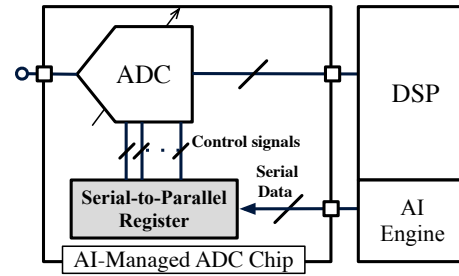[4]Details on the transconductances in this circuit can be found in [126].

Fig. 20. SPR combined with an AI engine to program an ADC.

Biasing and Digital Control Programmability: Similarly to the examples shown in previous section, the performance of CT BP-$\Sigma\Delta M$s can be adapted to the different operation modes with optimized power consumption, by adjusting the biasing of all building blocks by means of a programmable master current generator. One of the characteristics of highly programmable ADCs is the huge number of digital control signals required to control and program their operation. For instance, in the widely tunable BP CT-$\Sigma\Delta M$ of Fig. 19, more than 180 digital control signals are needed. Such a large number of digital signals requires a Serial-to-Parallel Register (SPR) to collect a serial input data and transform this data into the parallel control bits and hence program the operation of the ADC as illustrated in Fig. 20. This way, the BP CT-$\Sigma\Delta M$ can be digitally programmed in an easy way, by loading the required control configuration for each operation mode. In the case of AI-managed digitizers for CR end-devices, the serial input data contains the information sensed from the electromagnetic environment, which is provided by the AI engine, as conceptually illustrated in Fig. 20.

C. Application of LSTM-based ANNs for CR Digitizers

In a CR receiver like that shown in Fig. 13(b), the operation of all building blocks can be assisted by an AI engine in order to find the best frequency holes and optimize the quality of service of the communication. To this end, a LSTM-based ANN will be considered as AI engine in this case study. This ANN needs to interact with the ASP/RF front-end, the ADC and the DSP in order to sense the information from the electromagnetic environment and predict the level of occupancy in a given band and/or channel.

Fig.21(a) illustrates a portion of the frequency spectrum with n channels centered at frequencies f_1, f_2, ... f_n. For each channel i, let us assume that the band occupancy can be measured in real time, obtaining the signals represented in Fig.21(b) for channels 1, 2, ... n. These occupancy signals, Oc_i, constitute the inputs for the AI engine, as shown in Fig. 22. In this case, n LSTM networks work in parallel, each one predicting the future evolution of an occupancy signal Oc_i^{pre}, so that a decision block takes the decision about which channel will be less occupied next. The decision block provides the information required to modify the receiver specifications according to the selected band [61].

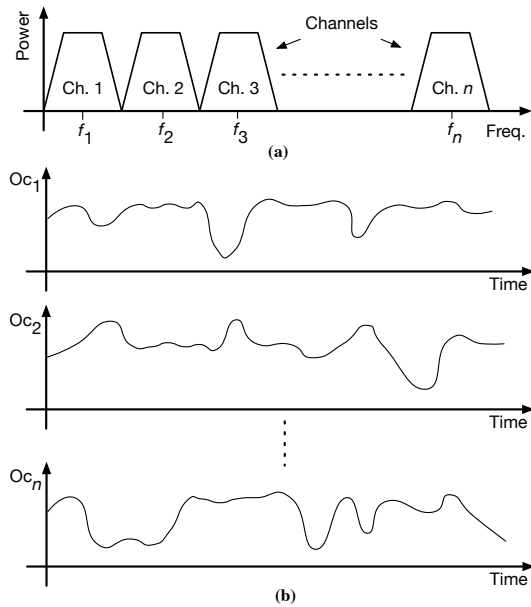*LSTM ANN for CR-based Receiver:* The LSTM networks used in Fig. 22 are *uni-variable*, i.e. they have one *neuron*,

Fig. 21. Frequency band with n channels. (a) Distribution of channels. (b) Channel power (occupancy) over time.

Fig. 22. CR transceiver controlled by a LSTM-based AI engine.

for input and output layers, while having one hidden layer with M LSTM cells followed by a fully connected layer and a single-neuron output layer. In this example, $M = 256$ is considered without loss of generality and a multi-step LSTM network was implemented to forecast more than one future time step, as defined for regression predictive modelling problems [220]. The aim of each LSTM network is to predict a certain number of future samples N_p of its input signal Oc_i. For that, the network has to be trained with a set of data representing real band occupancy signals, allowing the network to learn their characteristics and dynamics. After training phase, each network can start predicting occupation in real time. Every time the new LSTM network receives a time sample, it calculates a programmable number of future samples N_p that can be processed by the decision block. The number of predicted samples N_p is a trade-off: a very small value will give a more precise prediction but it will limit the capability of the system to anticipate the future evolution of the frequency spectrum, while a very large value will improve the anticipation but the error of the predicted signal will increase.

AI Engine Decision and Receiver Response: A decision subsystem receives all predicted occupancy signals for each channel and determines which one should be selected with a certain anticipation related to the value of N_p. The center frequency of the RF filter, the LNA and the BP CT-$\Sigma\Delta$M can be properly selected according to the data provided by the LSTM network engine, so that the desired signals can be moved to the most convenient band allocation in terms of interferences, noise floor and QoS. This can be implemented as follows: at a given time instance, t_0, the decision block has to compare the future evolution of each occupancy signal $Oc_i^{pre}(t_0, ..., t_0 + N_p)$. From the comparison of these n segments, the decision block predicts which channel will reach the lowest occupancy value within this time interval.
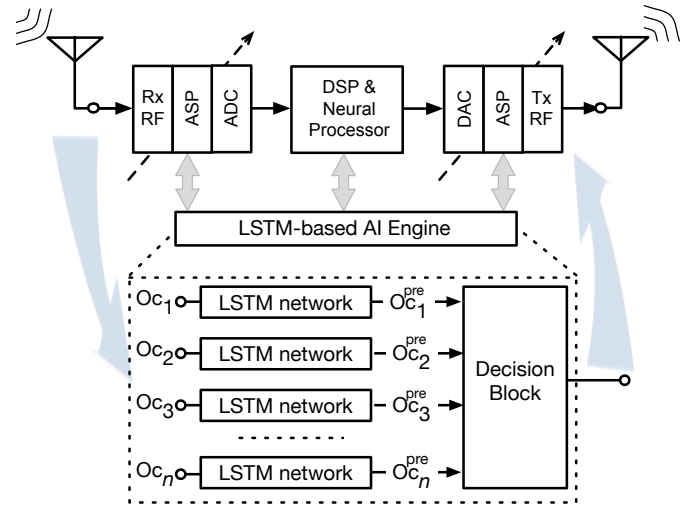
If the lowest value corresponds to a channel different from the currently selected one, the decision block has to choose a different set of control parameters to adjust the operating frequency of the different building blocks in the receiver chain. In this example, a look-up table approach is used to map the information provided by the LSTM network to electrical parameters of the RF filter, the LNA and the BP CT-$\Sigma\Delta$M.

Let us consider an example of four frequency channels as an example extracted from [61]. This is a particular case of the one proposed in Fig. 22 by considering four LSTM networks. As inputs, some synthetic patterns are defined by alternating between full and empty occupancy for each channel. First, a segment with $10,000$ samples was generated to train the LSTM networks, and afterwards 4 segments with $2,500$ samples were used to test the system. A fragment with $1,000$ samples of the 4 input test signals is shown in Fig. 23(a), while the last signal shown in this picture corresponds to the band selection signal generated by the decision block. Each step of this signal indicates which channel must be selected by the receiver. It can be shown how at instant t_1 the system predicts that the occupancy of channel 4 will decrease, selecting its corresponding frequency band. At t_2, the predictions say that the occupancy of the selected channel 4 will increase, while it will decrease for channel 3. Therefore, channel 3 is selected until t_3, when the system predicts that two different channels will become less occupied (1 and 2), so the first one is chosen following a priority list where lower bands are preferred. At t_4, the selected channel is expected to get busy again, so the decision block compares all predictions, selecting channel 2.

Note that every time the decision block selects a certain band, it modifies the control parameters of the different building blocks of the receiver, i.e. the BP filter, the LNA and the BP-$\Sigma\Delta$M, to make them to operate over the selected frequency. As an illustration, Fig. 23(b) represents the four transfer functions for an example bandwidth given by the RF filter, where each one is chosen to select a different frequency channel. The center frequency is automatically selected in each case according to the information provided by the LSTM AI
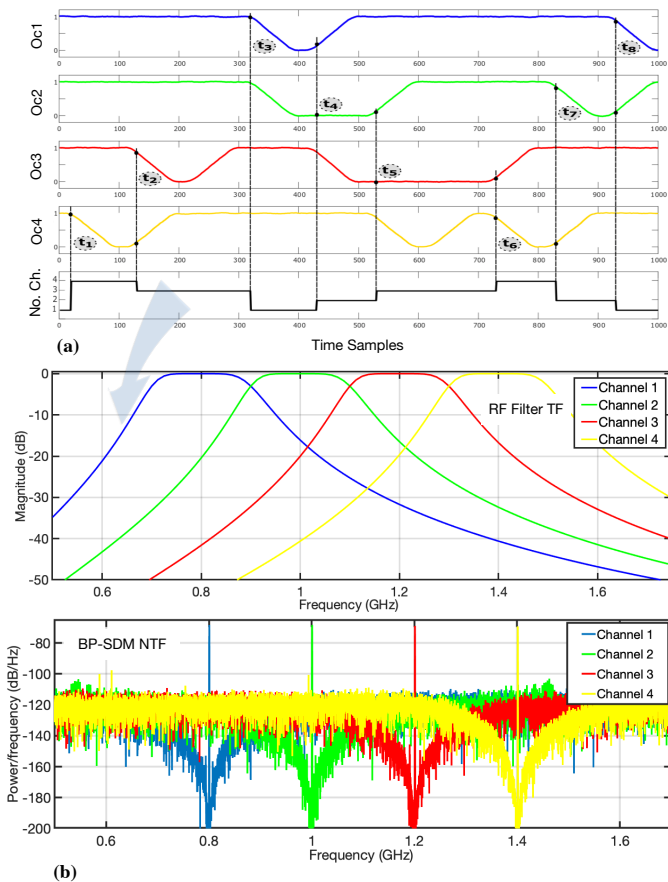
Fig. 23. Illustration of the operation of the LSTM-based AI engine in CR receivers. (a) Evolution of channel occupancy and band selection provided by the decision block [61]. (b) Effect on tuning of the RF filter Transfer Function (TF) and noise-shaping of the BP CT-$\Sigma\Delta$M.

the communication with the best quality of service possible. AI engines can be applied to this purpose and there are an increasing interest in using different types of ANNs to perform the spectrum sensing and management functions required for CR systems. However, although much work is being done, there is still a long way to make CR-based transceivers a reality and to put such transceivers in commercial mobile terminals. A number of design challenges must be faced – from system concept to circuit implementation, becoming more and more demanding for the RF front-end, analog signal processor and analog/digital interfaces of CR-based transceivers.

An survey of some of the circuits and systems techniques required to put CR end-devices in practice have been overviewed in this paper, highlighting the benefits and trends of using ANNs to do spectrum-management tasks and control the operation of CR transceivers. In the most ideal case, translating the signal processing from the analog to the digital domain would make it easier the implementation of the CR paradigm. However, there is a number of trade offs involving the use of a mostly-digital approach and the price paid by an early RF digitization. From the circuit design perspective, the RF/digital interface is one of the bottlenecks and special emphasis has been put in this article on the use of ADCs as one of the key building blocks and technology players to make CR transceivers a reality.

The state of the art on ADCs has been roughly reviewed, by putting special attention on those ADC architectures based on reconfigurable $\Sigma\Delta$Ms, as well as mostly-digital, digital-assisted analog circuit techniques as technology drivers to embed the required programmability in AI-managed RF-to-digital interfaces. Some examples discussed in the paper are emerging digitizers based on the hybrid combination of $\Sigma\Delta$Ms and Nyquist-rate ADCs – such as SAR and Pipeline – are also good cadidate architectures. Two chip case studies based on reconfigurable LP SC-$\Sigma\Delta$Ms and widely-tunable BP CT-$\Sigma\Delta$Ms, as well as the use of LSTM-based ANNs, have been shown as an illustration of using highly programmable $\Sigma\Delta$Ms for AI-managed ADCs in CR receivers. Some of the circuits and systems discussed in this survey are still in their early stages of deployment, while others are based on more mature circuit techniques. In all cases, merging AI engines to control the operation and specifications of ADCs is still a matter of research. Addressing some of the challenges discussed in this paper in the incoming deep-nanometer technology nodes will lead to new research opportunities and ways to implement AI-managed digitizers in an increasingly digital-driven world.

engine. Based on the information provided by the LSTM-based AI engine, the rest of receiver blocks change their parameters. This is also illustrated in Fig. 23(b) by showing how the NTF and the notch frequency of the BP CT-$\Sigma\Delta$M is modified according to the feedback provided by the decision block. It is important to remark that, in order for the overall CR system to operate correctly, the *granularity* of the programmability of the $\Sigma\Delta$M-based digitizer must be as fine as possible in order to give the AI engine more degrees of freedom to properly choose the best parameters to optimize the communication in the selected sub-band or channel. This would impose a number of design trade-offs which involves reconfiguration techniques at both circuit and system level which are still open to research.

VII. CONCLUSIONS

Cognitive radio postulates as one of the technology enablers to efficiently connect the increasingly number of wireless devices through new generations of mobile telecom systems such as 5G/6G and beyond. The basic concept behind CR – proposed by Mitola more than 20 years ago – is a smart way to manage the crowded electromagnetic spectrum by sensing the information from the environment, identifying the less occupied frequency band, and consequently adapting the transmission parameters of wireless transceivers in order to do

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