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Ultra-High-Resistance Pseudo-Resistors with Small Variations in a Wide Symmetrical Input Voltage Swing

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***Abstract*—This paper presents a new strategy and circuit configuration composed of serially-connected PMOS devices operating in the subthreshold region for implementing ultra-high-value resistors required in very low-frequency active-RC filters and *bio-amplifiers*. Depending on the application, signal bandwidth for instance in *bio-amplifiers* may vary from a few mHz up to a maximum of 10 kHz. Three different resistor structures are proposed to achieve ultra-high resistance. While ranging in the order of several TΩ, the proposed ultra-high-resistance pseudo-resistors occupy a small on-chip silicon area, which is one of the main issues in the design of analog front-end circuits in ultra-low power implantable biomedical microsystems. In addition, these ultra-high-value resistors lead to the use of a small capacitance to create a very small cut-off frequency. Therefore, the large area to implement capacitances is also considerably reduced. The proposed resistor structures have very small variations about 7% and 12% in a wide input voltage range (-0.5 V~+0.5 V), thus significantly improving the total harmonic distortion of *bio-amplifiers* and the analog front-end of the system. Simulation results of different circuits designed in a 180nm CMOS technology, are shown to demonstrate the advantages of the proposed ultra-high-resistance pseudo-resistors.**

***Index Terms*—MOST-based resistors, low-voltage, low-power biomedical systems.**

I. INTRODUCTION

A MOS transistor operating in the triode region is often implemented to make very low resistance values for realizing close-to-ideal switches [1]-[4]. Conversely, some systems, such as those used in biomedical signal recording applications, require ultra-high resistance values to create very low cut-off frequency for the filtering of undesired input signals, noise, and DC components caused by the effect of electrodes [5]-[13]. Depending on the application, the bandwidth of the input signal may range from a few mHz to a few kHz [13]. For example, signal bandwidth for ElectroEncephaloGraphy (EEG), and ElectroCardioGraphy (ECG) applications are in the range of 0.5–40 Hz, and 0.05–100 Hz, respectively [14]. Therefore, versatile amplification and filtering front-end circuits with very low operating frequencies are very desirable [15]-[17]. Fig. 1 shows a typical bio-amplifier that uses capacitive feedback [5], [18]. In many cases, the occupied on-chip area by the required capacitances is even larger than the area of the main amplifier itself [14]. Given the size limitation of on-chip capacitors, resistors in the range of hundreds of GΩ and even TΩ are normally needed to achieve the required very low cut-off frequencies [5], [18]-[20]. As can be seen, high-value resistors are very desirable for implementing very low-frequency filters. To address this demand, Harrison et al. [5] demonstrated that diode-connected pseudo-resistors can be used to implement ultra-high-value resistors. They also showed the application of the proposed ultra-high value resistor to design a low-noise low-power operational transconductance amplifier (OTA) with capacitive feedback for neural recording applications with very small low-cut-off frequency. Although the presented method was

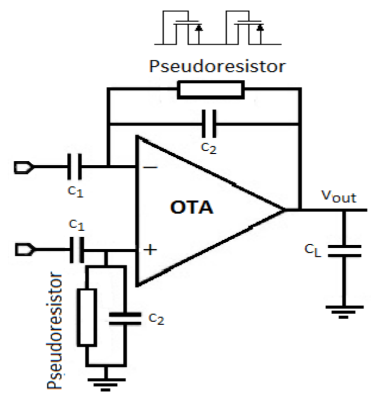

Fig. 1. Schematic of a bio-amplifier with diode-connected transistors to implement feedback resistors [5].

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successful in achieving high resistance values, the resistance highly depends on the common-mode voltage shifting and output signal level, that causes the resistance to drop severely. This issue results in strong variations in the cut-off frequency and consequently, it leads to harmonic distortion that can degrade the performance of the bio-amplifier and the amplified output signal. When the voltage across the pseudo-resistance (the difference between input signal and the output signal seen in Fig. 1) is changed and decreased, its resistance value drops to very low values, hence the cut-off frequency will be increased and in-band signal will be attenuated and distorted. In [21] a CMOS pseudo-resistors operating at the subthreshold region with an auto-tuning circuit was proposed to achieve high equivalent resistance. The auto-tuning circuit, was composed of an operational amplifier, some capacitors, and active resistors. However, the proposed structure was relatively complex due to its auto-tuning circuit, and a relatively large silicon area was used for the realization of the required capacitors. Furthermore, the maximum achievable resistance was restricted to 100 GΩ and the achieved resistance is relatively sensitive to the voltage across it such that ±0.5 V of voltage swing. This resulted in about 30% change in the resistance with the subsequent degradation due to harmonic distortion.

To address these issues, this paper proposes ultra-high-resistance pseudo-resistors (UHRPR), which benefit from steady resistance values of about 1.3 TΩ, 900 GΩ, and 2 TΩ over an extended voltage swing range of ±0.5 V. The proposed structures also benefit from small on-chip area while having relatively constant resistances over ±0.5 V voltage swing.

The brief is organized as follows. Following this introduction, Section II explains the proposed method and analyzes the technique. Section III proposes and describes three circuit configurations of UHRPR and depicts their simulation results to demonstrate the performance of the technique. Brief results and comparison with previous works are presented in section IV. Finally, the conclusion is given in section V.

II. Method and Analysis

Fig. 1 shows a band-pass bio-amplifier with diode-connected transistors used to implement the feedback resistors [5]. The middle band voltage gain of the band-pass amplifier, A_M, ω_L its low cut-off frequency, and ω_H, its high cut-off frequency are calculated by (1) to (3). A_M, is set by the ratio of the C_1 to the feedback capacitor (C_2). R_{PR}, the resistance of each Pseudo-resistor structure, which is produced by two MOS-Pseudo resistors is about tera-ohm requiring a very small C_2 for creating the small f_L.

$$A_M \approx \frac{C_1}{C_2} \tag{1}$$

$$\omega_L = \frac{1}{2R_{PMOS}.C_2} = \frac{1}{R_{PR}.C_2} \tag{2}$$

$$\omega_H = \frac{1}{R_{out-amp}.C_L} \tag{3}$$

As stated in the Introduction, CMOS pseudo-resistors operating in the subthreshold region can be used to achieve high equivalent resistance. To analyze these circuits, the EKV model of MOS transistors [22] will be considered. In this case, the source-drain current of a PMOS device working in the subthreshold region can be expressed as follows:

$$I_{SD} = I_s.e^{\frac{(V_{BG}-V_{T0})}{nU_T}}.\left(e^{\frac{-V_{BS}}{U_T}} - e^{\frac{-V_{BD}}{U_T}}\right) \tag{4}$$

where $I_s = 2n\mu C_{ox}(W/L_{eff})U_T{}^2$, and $U_T = KT/q$, in which, n is the subthreshold slope factor, μ is the mobility, C_{ox} is the gate oxide capacitance per unit area, W is the width of the transistor, L_{eff} is the effective length of the transistor, U_T is the thermal voltage, and V_{T0} is the threshold voltage of the transistor. As seen in (1), the current and, consequently, the resistance of a MOS transistor, R_{SD}, depends on V_{BG}, V_{BS} and V_{BD}. Therefore, by minimizing the variation of these voltages or by forcing them to be fixed, the variation of the MOS resistivity can be minimized.

Considering V_{BG} and V_{BS} equal to zero and according to (4), the source-drain current and the resistance of each PMOS transistor would be calculated as follows

$$I_{SD}|_{V_{BG}=V_{BS}=0} = I_s.e^{\frac{-V_{T0}}{nU_T}}.(1 - e^{\frac{-V_{BD}}{U_T}}) \tag{5}$$

$$R_{SD} = \left(\frac{\partial I_{SD}}{\partial V_{SD}}\right)^{-1} \tag{6}$$

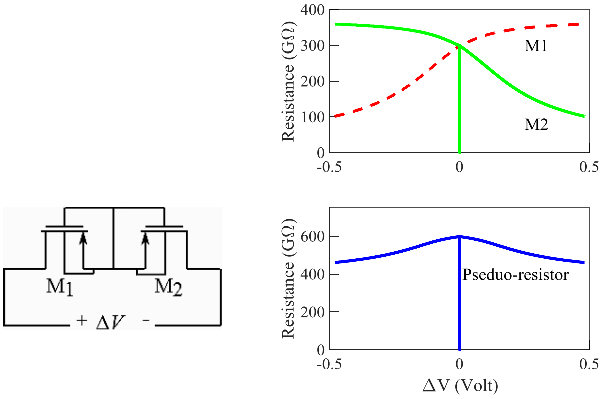
Since $V_S = V_B$,

$$R_{SD} = \left(I_s.\frac{1}{U_T}.e^{\frac{-V_{T0}}{nU_T}}.(e^{\frac{-V_{BD}}{U_T}})\right)^{-1} \tag{7}$$

III. Circuit Design and Simulation Results

Fig. 2(a) shows the basic structure of the proposed pseudo-resistor that consists of two series-connected MOS transistors operating in subthreshold region, in which their bulk, source and gate are connected together and hence, V_{BG} and V_{BS} are forced to be zero. In this configuration, as discussed in section II, the variation of R_{DS} of each transistor is minimized insofar as the voltage across the terminals, brings M_1, M_2 out of subthreshold region.

Fig. 2(b) depicts the resistance curves of transistors M_1 and M_2 versus voltage ΔV and also illustrates the mechanism of how a relatively linear pseudo-resistor is made. The resistance of each transistor varies from100 GΩ to 370 GΩ for ±0.5 V of voltage swing, but with the opposite slope. The resistance curve of the pseudo-resistor is equal to the summation of the resistance of each series transistors M_1 and M_2 and has the amount of 470 GΩ up to 600 GΩ for ±0.5 V of voltage swing. The graphs show that the resistance of M_1 and M_2 act complementary such that the total resistance of the series transistors M_1 and M_2 (for all values of ΔV) has a relatively high value with more linearity. In order to achieve an UHRPR with higher linearity, as shown in Fig. 3, two of these pseudo-resistor elements are connected in series. Note that in this configuration, the voltage across the UHRPR will be divided in four MOSFETs. Therefore, voltage variations have less effect on the V_{DS} of each transistor and leads more linearity. By increasing the number of the pairs of basic pseudo-resistor elements, larger



(a) (b)

Fig. 2. Proposed pseudo-resistor structure. (a) Schematic. (b) Equivalent resistance versus voltage variation across its terminals. The resistance curve of the pseudo-resistor is achieved by the sum of the resistance of each series transistors M_1 and M_2.

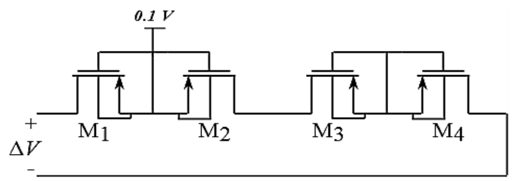
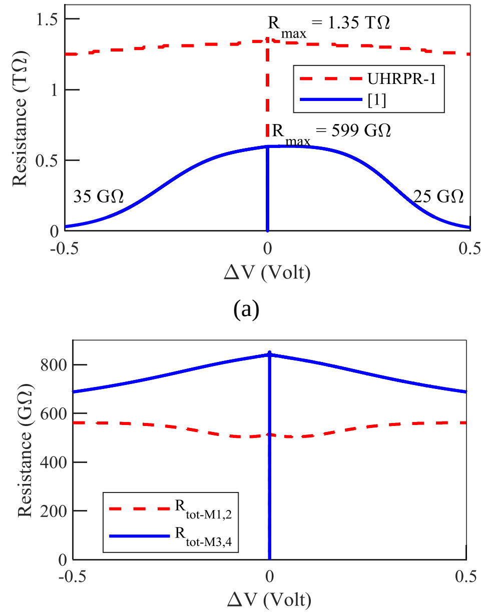


Fig. 3. Proposed ultra-high-resistance pseudo-resistor (UHRPR-1) structure based on the basic pseudo resistor element (Fig.2)



(a)

(b)

Fig. 4. (a) Comparison between conventional diode-connected pseudo-resistor [5] and the proposed UHRPR-1 (Fig. 3). (b) Resistance versus ΔV of each proposed basic pseudo-resistor element according to Fig. 3, and also illustration of the mechanism of how R_{tot} is kept nearly constant using two series basic pseudo-resistor elements.

resistance with smaller variation over ±0.5 V of voltage swing will be achieved. But on the other hand, the number of these serially-connected pseudo-resistor elements should not be increased much more, because the voltage across each MOS transistor will be very small and they don't work well to achieve our goal and desired value of resistance and linearity. In addition, the voltage of the gate (and consequently the bulk and source voltages) for one pair of the pseudo-resistors is set to 0.1 V. This change causes the resistance curve of these two pairs to become symmetric and as a result the variations of the overall resistance versus voltage becomes even less. Moreover, since only four MOS transistors are used in the proposed structure, the structure is compact and occupies a relatively small on-chip area.

To verify the proposed ultra-high resistance pseudo-resistor (named UHRPR-1), transistors with $(W/L)_{1,2}$ = (0.25 /3 µm/ µm) and $(W/L)_{3,4}$ = (0.25 /18 µm/ µm) in a 0.18 µm standard CMOS process were used. While -0.5 V to +0.5 V voltage swing is quite a large range especially in modern technologies, to demonstrate the robustness of the proposed method, this range is used for simulation purposes. Fig. 4(a) depicts the resistance of the conventional diode-connected pseudo-resistor [5] related to Fig. 1, in which $(W/L)_{1,2}$ = (0.25 /20 µm/ µm) to achieve the maximum possible resistance of about 600 GΩ. Note that the curve is not symmetric around the zero voltage and the resistance drops with sever slope from 599 GΩ to about 25 GΩ or 35 GΩ within the given range. In contrast, as shown in Fig. 4(a), the curve related to the proposed UHRPR-1 demonstrates that the total resistance of the proposed structure of Fig. 3 is nearly constant over the considered range of ΔV. Moreover, as shown in 4(b), applying a small voltage (0.1 V) at the gate of one pair of the basic pseudo-resistor elements, changes the slope of the resistance curve such that it can compensate the variations of the resistance of the other pair of transistors. Therefore, the overall resistance of the structure of Fig. 3 would be relatively constant. The simulation results show a total resistance variation about 7% for a ±0.5 V voltage range across the circuit. It is worth mentioning that if two pairs of the PR elements (proposed structure in Fig 2.a) are used in series, while not applying 0.1 V to one pair, the total resistance will vary between about 940 GΩ to 1.2 TΩ. This means about 22% variations over ±0.5 V voltage swing.

At the following, two other high resistance pseudo-resistor structures (named UHRPR-2 and UHRPR-3) based on the UHRPR concept are presented and simulated. The first one is illustrated in Fig. 5(a) and the related resistance of its parts over a voltage swing, ΔV, of -0.5 V to +0.5 V is depicted in Fig. 5(b) while all transistors have the size of W/L= (0.25 /1 µm/ µm) in a 0.18 µm standard CMOS process. The graphs show that the total resistance of $M_{1,2}$ and $M_{3,4}$ act complementarily. Therefore, the total resistance of the ultra-high-resistance pseudo-resistor (UHRPR-2), for all values of ΔV, becomes more linear and also has a relatively high value with a maximum amount of 900 GΩ. The result of this procedure is illustrated in Fig. 6. As illustrated in Fig. 6, the total resistance of this structure varies from 840 to 900 GΩ.

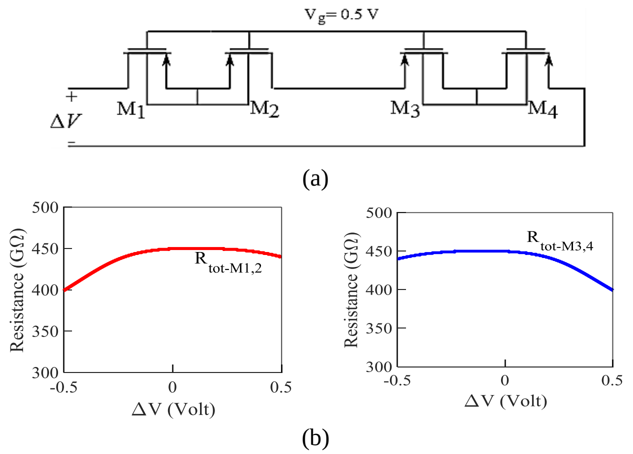


Fig. 5. (a) UHRPR-2 structure to achieve 900 GΩ resistance. (b) The related resistance of each part over the voltage swing of ±0.5V.

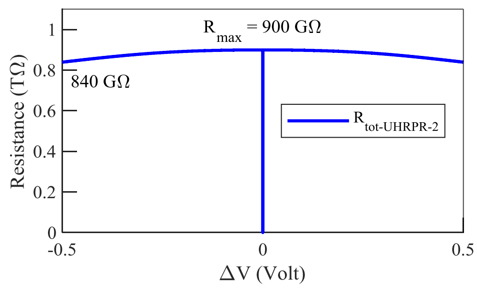


Fig. 6. The total resistance of the UHRPR-2 proposed in Fig. 5 that is the summation of the resistance of its two serial constituent parts.

Therefore, its variation is too small and is limited to 6.6 %. In addition, due to the small sizing of the MOS transistors (0.25 /1 µm/ µm), this structure benefits also from a small silicon area.

The circuit diagram of the third ultra-high-resistance pseudo-resistor structure (UHRPR-3) proposed based on the concept of the proposed UHRPR and its related resistance over the voltage swing (*ΔV*) of -0.5 V to +0.5 V are depicted in Fig. 7. All transistors have the size of *W/L*= (0.25 /1 µm/ µm) in 0.18 µm standard CMOS process, so the on-chip area of the structure is too small like previously presented structure above. In this configuration with respect to prior ones, the source-body connection or drain-body connection has been removed and instead, the body of one pair of the transistors is connected to a voltage of 0.1 V. This structure leads to a maximum of 2 TΩ resistance and the minimum of 1.75 TΩ. So the resistance variation over the ± 0.5 V swing voltage is 12.5 %. PVT analysis could be performed to show the performance of an analog circuit. Actually, section III has investigated the effect of voltage variations on the proposed ultra-high resistances. Regarding process variations, the simulation in other modes in addition to TT mode carried out for all three structures over the voltage swing (*ΔV*) of -0.5 V to +0.5 V. The PVT simulation results for three structures are expressed briefly in Table I. As it is seen in the table, the dependence and variation of UHRPR-2 to process is too small that can be neglected. In this case the amount of the resistance in all corners, is very close to the

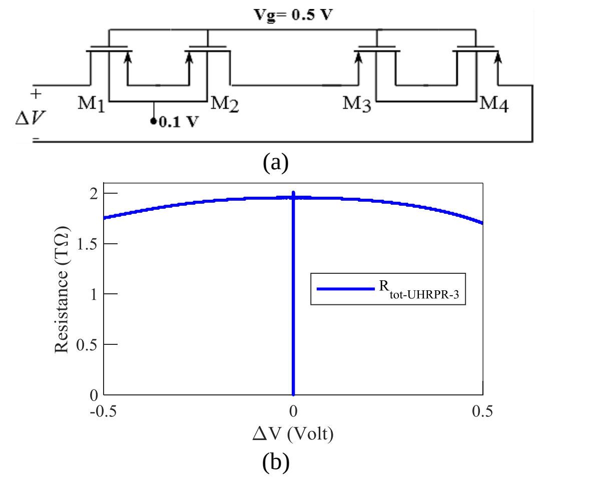


Fig. 7. Proposed UHRPR-3 structure. (a) Schematic. (b) Total resistance over the voltage swing of -0.5 V to +0.5 V that is between 2TΩ and 1.75 TΩ.

amount of the resistance in TT mode. THD analysis is also performed and its results are summarized in Table I. The maximum noise produced by the structures is related to very low frequencies due to flicker noise and is about $3.25\frac{nV}{\sqrt{Hz}}$, $435\frac{pV}{\sqrt{Hz}}$, and, $12\frac{pV}{\sqrt{Hz}}$ in the frequency range of 100 mHz for UHRPR-1, UHRPR-2, and UHRPR-3 respectively.

Monte Carlo simulation results are depicted in Fig. 8 for all three UHRPR structures that prove acceptable robustness of them in terms of both mismatch and process variations.

IV. Comparison with Prior Art

A comparison with several previous works, is summarized in Table 2. The comparison shows that the proposed UHRPRs offer much higher range of resistances, whereas their sensitivity to variations of the applied voltage is much less and their occupied on-chip area is much smaller.

V. Conclusion

A novel configuration for the implementation of ultra-high-resistance pseudo-resistors has been proposed. It has been shown that using only four PMOS transistors biased in subthreshold regime, with shorted bulk, gate and source terminals, a resistance of about 1.3 TΩ can be achieved. It has been further demonstrated that the proposed pseudo-resistor benefits from a symmetric V-R characteristics and a relatively constant resistance over an extended input voltage range. According to the proposed configuration and its working procedure, two other structures have been implemented and shown to achieve 900 GΩ and 2 TΩ with 6.6 % and 12.5% variation, respectively, over -0.5 V up to +0.5 V voltage across them. Simulation results in standard 0.18 µm CMOS technology confirmed the proposed concept. The proposed ultra-high-resistance pseudo-resistors are well suited for applications requiring extremely low cut-off frequency. All proposed structures benefit from small on-chip area and can be used to achieve a very small cut-off frequency with low distortion in the output of the bio-amplifier, filters, etc.

TABLE I
SIMULATION RESULTS OF PVT ANALYSIS FOR ± 0.5 V VOLTAGE SWING

	UHRPR-1	UHRPR-2	UHRPR-3
TT	1.25~1.35 TΩ	840~900 GΩ.	1.75~2 TΩ
FF/SF	520~764 GΩ	838~899GΩ.	1.54~1.95 TΩ
SS/FS	1.85~1.55 TΩ	840~899.5 GΩ.	1.75~1.97 TΩ
-50 °C	1.85~1.99 TΩ	909 GΩ.	2 TΩ
+50 °C	575~870 GΩ	624~651 GΩ	1~1.36 TΩ
+90 °C	13~51 GΩ	14~51 GΩ	14~53 GΩ

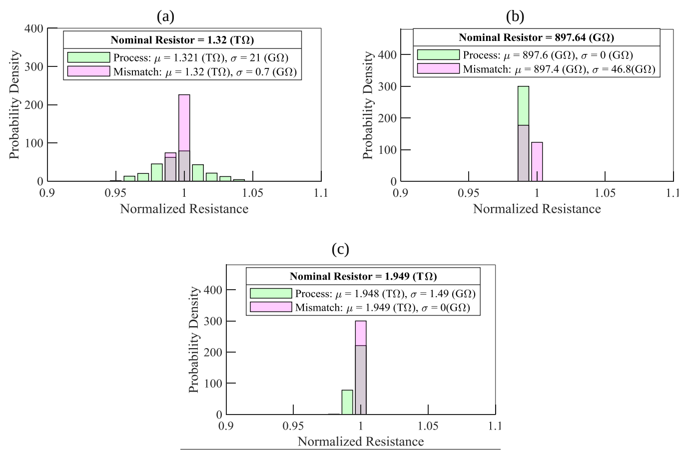


Fig. 8. 300-point Monte Carlo simulation results for all three structures in terms of both mismatch and process variations.

TABLE II
COMPARISON THE PROPOSED STRUCTURE WITH SEVERAL PREVIOUS WORKS. ALL RESULTS ARE REPORTED FOR THE VOLTAGE RANGE OF -0.5 V TO 0.5 V.

	Range of the resistance	Variations (%)	Silicon area	Process σ/μ	Mismatch σ/μ
[5] 1.5 µm CMOS	30 ~599 GΩ	95	--- (small)	---	---
[9] SOI 0.18 µm	1 MΩ ~1 GΩ	11	16000 μm^2	0.043	0.043
[21] 0.18 µm CMOS	50 ~70 GΩ (for V_{ctrl}=0.9 V)	28	--- (Large)	---	---
[23] 0.35 µm CMOS	20 MΩ ~20 GΩ	---	17700 μm^2 to obtain 300 MΩ	0.255	0.067
This work 0.18 µm CMOS — UHRPR-1	1.25~1.35 TΩ	7	90 μm^2 (26 µm ×3.4 µm)	0.016	0.0005
This work 0.18 µm CMOS — UHRPR-2	840~900 GΩ.	6.6	25 μm^2	≈ 0	0.00005
This work 0.18 µm CMOS — UHRPR-3	1.75~2 TΩ	12.5	25 μm^2	0.00007	≈ 0

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