A 10-MHz BW 77.3-dB SNDR 640-MS/s GRO-based CT MASH $\Delta\Sigma$ Modulator

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***Abstract*—We present in this paper a novel multi-stage noise-shaping (MASH) 3-1 continuous-time (CT) delta-sigma modulator ($\Delta\Sigma$M) with gated ring oscillator based quantizers (GROQs) in both stages of the cascade. The use of GROQs increases the linearity performance with respect to the conventional voltage controlled oscillator based quantizers (VCOQs) and allows a more robust extraction of the front-end stage quantization error in the time domain, thus making the proposed architecture more suitable to implement high-order expandable scaling-friendly MASH $\Delta\Sigma$Ms, in which the back-end stages are implemented by mostly-digital GRO-based time-to-digital converters (TDCs). The circuit has been fabricated in a 65-nm CMOS technology with 1-V supply voltage, and it operates at 640-MHz sampling frequency to digitize 10-MHz signals. To the best of the authors' knowledge, this is the first reported experimental validation of a GRO-based CT MASH $\Delta\Sigma$M, featuring a 79.8-dB signal to noise ratio (SNR) at -2.2-dBFS, a 77.3-dB signal to (noise + distortion) ratio (SNDR) at -4-dBFS and a dynamic range (DR) of 81.7 dB, with a power consumption of 12-mW. These metrics demonstrate state-of-the-art performance with a DR-based Schreier FOM of 170.9 dB.**

***Index Terms*—Analog-to-digital converters, $\Delta\Sigma$ modulators, continuous-time circuits, time/frequency-based quantization.**

I. Introduction

Continuous-time (CT) $\Delta\Sigma$ modulators ($\Delta\Sigma$Ms) have demonstrated to be the most efficient technique to implement analog-to-digital converters (ADCs) in a number of applications requiring medium resolution (12-14 bit) within a signal bandwidth (BW) in the order of 10-100 MHz. At these speeds, the oversampling ratio (OSR) is limited by prohibitive sampling rates – usually in the order of several GHz – while the loop-filter order cannot be increased beyond four or five, due to stability constraints. Thus, multi-bit quantization is needed in many cases in order to meet the dynamic range (DR) requirements. However, the design of conventional amplitude-based quantizers –such as Flash, or SAR ADC– is severely conditioned by the reduction of supply voltages associated to technology downscaling [1].

These limitations have prompted the interest for the time/frequency-based quantization rather than the conventional amplitude-based quantization. This way, the DR of the ADC is not limited by the voltage headroom since the information is digitized in the time domain rather than the voltage domain. One of the first successful implementations of frequency-based ADCs was proposed in [2], where the authors replaced the quantizer of a $\Delta\Sigma$M by a VCO-based quantizer (VCOQ), with the additional benefit of having an implicit dynamic element matching (DEM) and first-order noise-shaping. These features have been exploited by $\Delta\Sigma$M designers to increase the noise-shaping filter order of ADCs, without increasing the order of the embedded analog filter, thus resulting in a mostly-digital/scaling-friendly circuit realization [3]–[13].

The main drawback of VCOQs is the nonlinearity associated with their voltage-to-frequency (V-to-F) transfer characteristic [2], what has motivated the exploration of some alternatives such as voltage-to-phase (V-to-P) converters [3], two-stage VCOs [9], or the so-called gated ring oscillators (GROs) [4]. The use of GROs have also been exploited in [5] to implement a single-loop fourth-order $\Delta\Sigma$M with a multi-bit time-encoded quantizer made up of two stages, in which the GRO is placed in the back-end stage. One of the main limitations of VCO-based MASH $\Delta\Sigma$Ms is the difficulty to extract the quantization error from the front-end stages. This has prompted the use of discrete-time (DT) front-end stages followed by a back-end VCOQ [12], or reduce the noise-shaping filter to a second-order 1-1 VCOQ MASH [11].

This paper contributes to this topic, and extends the idea presented in [14], going from a DT $\Delta\Sigma$M to an active-RC circuit realization, and including multi-bit GROQs in both stages of a 3-1 MASH architecture. This way, the proposed approach benefits from the combination of power-efficient CT-$\Delta\Sigma$Ms with the inherent linearity of GROQs. Moreover, the quantization error of the front-end quantizer is extracted in time-domain, so that the back-end stage can be implemented by GRO-based TDCs in a mostly-digital scaling-friendly way. To the best of the authors' knowledge, this is the first successful chip implementation which embeds GRO-based quantizers in both stages of a CT MASH $\Delta\Sigma$M.

II. Proposed Modulator Architecture

Figure 1(a) shows the block diagram of the proposed GRO-based CT MASH $\Delta\Sigma$M. The front-end stage is made up of a CT filter, a pulse width modulator (PWM), a multi-phase GROQ, and a feedback DAC[1], while the back-end stage is a multi-phase GRO TDC. The output voltage of the

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[1]An additional DAC – not shown for the sake of simplicity – is required to compensate for the excess loop delay (ELD).

CT loop filter, $V_{\text{in,f}}(t)$, is compared with a triangle sinewave, $V_{\text{Tri}}(t)$, to generate a PWM signal, P_{in}, which controls the operation of the GRO, so that it oscillates when P_{in} is high or gets frozen otherwise. Then, a counter generates a digital representation of the quantizer input by counting the output edges of the different GRO phases, ph, during a given sampling period, T_s=1/f_s, with f_s being the sampling frequency. A simple digital circuit, named QE-ext in Fig. 1(a), extracts the time-domain quantization error signal of the front-end stage quantizer, which in turns feeds the back-end stage and controls the operation of the GRO-TDC in this stage. The outputs of both stages are generated from their GRO outputs by using a frequency-to-digital converter (FDC), which implements a differentiation transfer function by using D-type flip-flops and a XOR gate as shown in Fig. 1(a). Finally, the outputs of both stages, y_1 and y_2, are processed by the digital cancellation logic (DCL) functions, $\text{DCL}_i(z)$, in order to generate the overall modulator output, y_{overall}.

In order to analyze the proposed modulator, the linear models shown in Fig. 1(b), is used. In this model, a CT loop filter is considered. The PWM block is modeled by a gain, given by $G_{\text{PWM}} = \frac{V_{\text{DD}}}{V_{\text{Tri}}}$ (where V_{DD} is the supply voltage and V_{Tri} is the peak-to-peak amplitude of the carrier frequency of the PWM) and the GRO is modeled by $\frac{K_{\text{GRO}}}{s}$. The time-based quantization error, E_i $(i = 1, 2)$, is modeled by an additive noise and the DT differentiator is represented by $(1 - z^{-1})$.

Analyzing the linear model in Fig. 1(b), the open-loop filter of the front-end stage, i.e. $H'(z)$, is given by:

$$\begin{aligned} H'(z) &= [H(s) \cdot H_{\text{DAC}}(s) \cdot \tfrac{K}{s} \cdot (1 - z^{-1})]^* \\ &= [H(s) \cdot H_{\text{DAC}}(s) \cdot \tfrac{K}{s}]^* \cdot (1 - z^{-1}) \end{aligned} \quad (1)$$

where $K = G_{\text{PWM}}.K_{\text{GRO1}}$, $H_{\text{DAC}}(s)$ is the feedback DAC transfer function, depicted in Fig. 1(b), and sampling operation is denoted by $[\ \ ]^*$ operator [8]. The noise transfer function (NTF) of the front-end stage can be obtained from (1):

$$NTF_1(z) = \frac{(1 - z^{-1})}{1 + [H(s) \cdot H_{\text{DAC}}(s) \cdot \frac{K}{s}]^* \cdot (1 - z^{-1})} \quad (2)$$

Note that $NTF_1(z)$ can be expressed as $NTF_1(z) = NTF'(z) \cdot (1 - z^{-1})$, where $NTF'(z) = \frac{1}{1+H'(z)}$ is the noise transfer function without taking the GRO-TDC into account. This way, the order of the front-end stage is increased by one.

The signal transfer function (STF) of the front-end stage is given by:

$$\begin{aligned} STF_1(s) &= \tfrac{[H(s) \cdot \frac{K}{s}](1 - z^{-1})}{1 + H'(z)} \\ &= H(s) \cdot \tfrac{K}{s} \cdot NTF_1(z), \quad z = e^{-sT_s} \end{aligned} \quad (3)$$

The Z-transform of the front-end stage can be derived from (2) and (3), yielding:

$$Y_1(z) = [X(s) \cdot STF_1(s)]^* + E_1(z) \cdot NTF_1(z) \quad (4)$$

Similarly, the output of the back-end stage can be expressed as:

$$Y_2(z) = E_1(z) \cdot [STF_2(s)]^* + E_2(z) \cdot NTF_2(z) \quad (5)$$

where $NTF_2(z) = (1 - z^{-1})$, $STF_2(s) = \frac{K_{\text{GRO2}}}{s} \cdot (1 - z^{-1})$ and $z = e^{-sT_s}$.

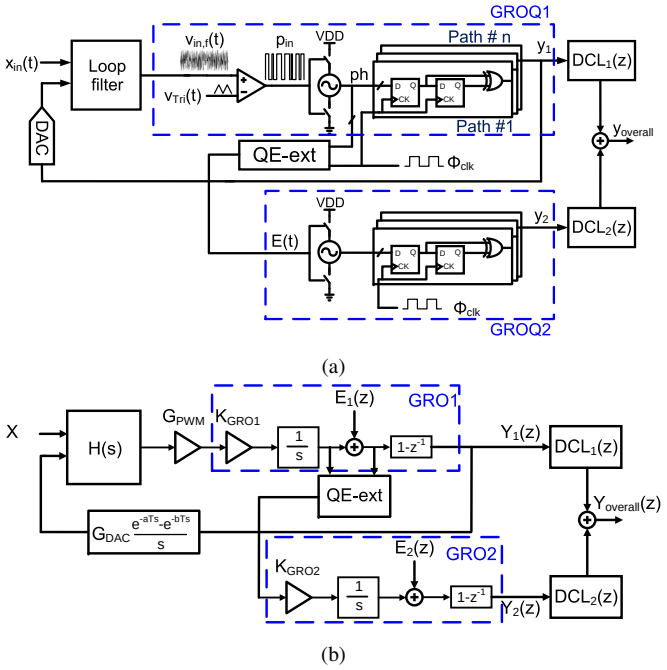


Fig. 1. Proposed GROQ-based CT MASH ΔΣM: (a) Block diagram, (b) Linear model.

The overall output of the modulator is then represented by

$$Y_{\text{overall}}(z) = Y_1(z) \cdot DCL_1(z) + Y_2(z) \cdot DCL_2(z) \quad (6)$$

where $DCL_{1,2}(z)$ are given by:

$$DCL_1(z) = [STF_2(s)]^* \quad (7)$$

$$DCL_2(z) = NTF_1(z) = NTF'(z) \cdot (1 - z^{-1}) \quad (8)$$

The proposed modulator has been synthesized to achieve a target SNDR of 80-dB within a signal bandwidth of 10-MHz. In order to get these requirements, extensive behavioral simulations have been carried out in order to determine the optimum set of modulator system-level parameters, including the overall loop filter order, L, number of bits of the embedded quantizer, B, and OSR. As a result of this study, the required ideal performance can be achieved with a fourth-order ($L = 4$) NTF, $B = 3$, OSR= 32 and an out-of-band gain, $H_{inf} = 1.5$. Considering these system-level parameters, the Schreier's toolbox is used to obtain the ideal NTF, yielding:

$$NTF'(z) = \frac{(z - 1)^2}{(z^2 - 1.225z + 0.4415)} \quad (9)$$

Note that (9) represents the second order NTF while an extra order of the noise shaping is achieved by the GRO-TDC resulting in a third-order NTF, as expressed in (2). Once the overall ideal NTF has been obtained, the equivalent CT loop-filter can be obtained by applying the impulse invariant transformation method, yielding:

$$H_{\text{Loop}}(s) = \frac{0.22 \cdot f_s \cdot s + 0.054 \cdot f_s^2 \cdot}{s^2} \quad (10)$$

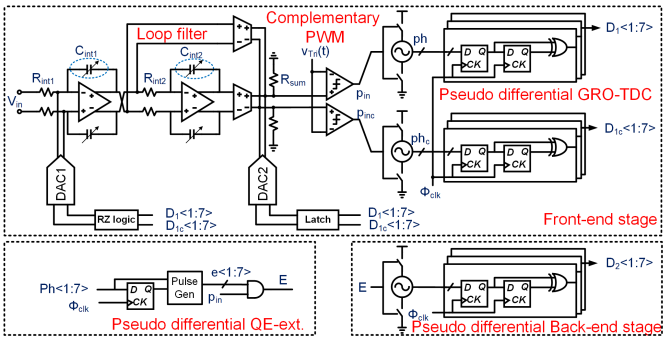


Fig. 2. Proposed GRO-based CT 3-1 MASH ΔΣM.

III. Circuit Implementation

Figure 2 shows the conceptual schematic of the proposed GRO-based quantizer CT-ΔΣM. The front-end stage consists of a second-order loop-filter, realized by two active-RC integrators, which are followed by a PWM[2] that transforms the integrator output voltage into a time-domain signal, which drives a GRO-TDC quantization. The main DAC, i.e. DAC_1, is a return-to-zero (RZ) DAC and the auxiliary DAC, i.e. DAC_2, is realized with non-return-to-zero (NRZ) DAC for ELD compensation. Note that the first stage is designed to accommodate one-clock cycle ELD while a RZ waveform provides a half delay of extra room [2].

A small input resistance, R_{int1}, must be chosen to reduce the in-band thermal noise power. However, for a lower resistance value, a larger integrating capacitance is required resulting in stringent dynamic requirements on the amplifier. This way, the first integrator resistor is opted to be 900-Ω, resulting in an input-referred thermal-noise floor of 91.2-dB below full-scale range and corresponding integrating capacitor of 3-pF. The thermal noise of the second integrator is suppressed by the gain of the loop-filter. Therefore, the input resistance of the second integrator, R_{int2}, is up-scaled to 14.4-kΩ in order to reduce the second integrating capacitor to a value of 0.5-pF and hence relax the second amplifier requirements.

A. Operational amplifiers

To minimize the ELD caused by loop-filter integrators, a high gain-bandwidth product operational amplifier is used. To this end, a 3-stage amplifier with no-capacitor feedforward (NCFF) scheme is adopted [15] in this design, as shown in Fig. 3(a). The high-gain path includes g_{m1}, g_{m2} and g_{m3} and they generate three poles. The high-speed path is provided by g_{mp2} and g_{mp3} where they introduce two left-half-plane (LHP) zeros. These zeros cancel out two of the three poles and guarantee the stability of the op-amp. Fig. 3(b)-(d) shows the transconductance (gm) cells used in the op-amp. A self-biased inverter-based transconductor topology [16] is utilized in the first stage, by providing a DC-gain of 45.6-dB, thus reducing the noise contribution of the following stages, i.e. $g_{m2,3}$. The middle stage of the amplifier includes $g_{m2,mp2}$, while providing a gain of about 31-dB. Note that $g_{m3,mp3}$ are the

[2]A synchronous PWM with a carrier frequency, $f_c = f_s$, is used in order to suppress the influece of carrier sidebands and its harmonics – which usually consumes a wider bandwidth in asynchronous PWMs.

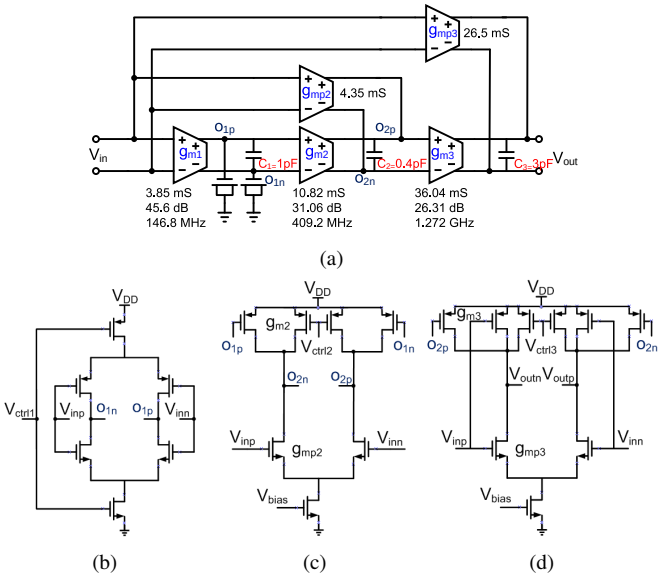


Fig. 3. Op-amps used in the proposed ΔΣM. (a) Overall topology and Schematic of transconductors: (b) g_{m1}, (c) $g_{m2,mp2}$ and (d) $g_{m3,mp3}$.

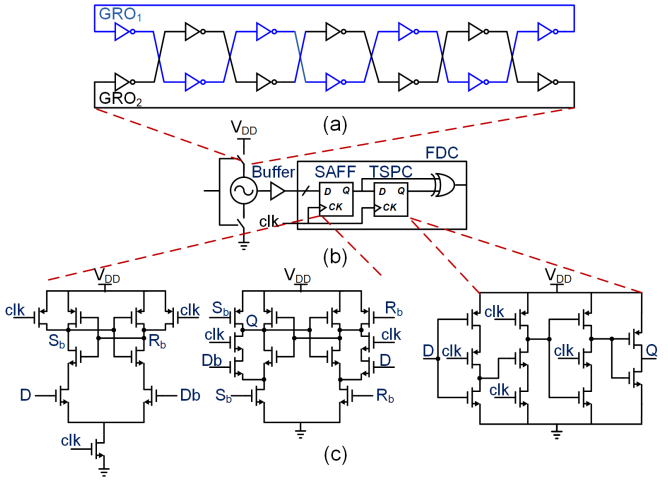
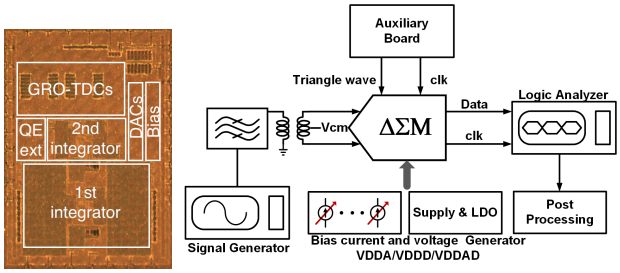


Fig. 4. GRO-TDC, (a) Inter-woven GRO structure, (b) GRO-TDC including GRO and FDC, (c) SAFF and TSPC.

main contributors to widen the bandwidth of the op-amp, by providing transconductances of 36-mS and 26.5-mS, respectively. Post-layout simulations of the front-end amplifier–the most demanding one– feature an 80-dB DC-gain, 65-dB gain at 10-MHz, a unity-gain-bandwidth (UGBW) of 1.82 GHz and a phase margin of 65°. A similar topology is employed for the second RC-integrator, featuring a DC-gain of 76.12 dB, a UGBW of 1.03 GHz and a phase margin of 65.7°. Note that the power consumption of the second op-amp is almost one third of the first op-amp since its noise contribution is less, thus reducing the overall power consumption.

B. GRO-based Quantizer

Figure 4 shows a conceptual (single-ended) schematic of the GRO-TDC. A 7-stage multi-path structure, equivalent to a 3-bit quantizer, is used. In this topology, the effect of leakage current and charge redistributions can be reduced resulting in a reduction of gating clock skew [4]. Buffers are used at the output of GRO phases to isolate GROs from the FDC kick-



(a) (b)

Fig. 5. (a) Chip micrograph, (b) Measurement set-up.

back noise. It also sharpens the rising and falling edges of the GRO output to alleviate rising/falling edges' distortion dependent. Post-layout simulations of the GRO show a phase noise of -80 dBc/Hz at 1-MHz offset frequency. According to system-level simulations, this level of phase noise does not limit the performance of the modulator. Note from Fig. 4 that a sense amplifier flip-flop (SAFF) and a true sample phase clock (TSPC) register are employed for the first and the second flip-flop in the FDC, respectively. The SAFF shows a metastability of less than 1-ps, which makes it appropriate for high-resolution GROQs.

C. Feedback DACs

The proposed ΔΣM incorporates two current steering based DACs, i.e. DAC_1 in the main path and DAC_2 for ELD compensation, adapted from [2]. An RZ waveform is used for the main DAC to allow an additional compensation for ELD at the expense of increasing the sensitivity to clock jitter. Off-chip capacitors are used for the DACs bias voltages to diminish the noise coupling from the current reference. DAC_2 is realized with a NRZ pulse shape [2]. The requirements for the second DAC is relaxed since the sensitivity to clock jitter and inter-symbol-interference (ISI) is suppressed by the loop filter.

D. Time-based Quantization Error Extraction and Generation

In the proposed MASH ΔΣM, the quantization noise is extracted in the time domain with a simple digital circuit, as the quantizer has been implemented in the time domain. To do so, a quantization error extractor based on the ones proposed in [4], [11] is adapted to this ΔΣM topology. The time-domain quantization error is the time interval between the rising edge of the clock signal and the closest rising edge of the GRO output phase. This time interval is detected by a flip-flop. As the quantization noise is the phase difference between the clock signal and GRO output phase, the phase difference can be detected by a phase detector e.g. an XOR gate. However, if the quantization error is narrow, the phase detector is unable to detect the error and causes dead-zone problem. To avoid this, a static offset of 2π is added to the quantization error by a flip-flop [4]. This static offset is removed in the DCL_2 and hence the overall performance is not affected by that offset.

IV. Measurement Results

The proposed GROQ-based CT MASH ΔΣM has been fabricated in a 1P8M 65-nm CMOS technology. Supply voltages of 1-V are generated on-board through off-chip LDOs to bias different voltage domains of the chip i.e. analog, digital and mixed-mode subcircuits. The op-amps are designed with standard MOS transistors while RF MOS devices are used to implement the GROs. Figure 5(a) shows the chip micrograph. A 44-pin QFN package is used to package the die. Note that almost 50% of the chip area is occupied by the first integrator while two GROQs only spend less than 20% of the total area. Fig. 5(b) shows the measurement set-up. A single-ended input sinewave is filtered with a passive band-pass circuit to suppress the harmonics of the signal generator and then convert it to a differential signal using a ADT1-6T+ balun. As shown in Fig. 5(b), an auxiliary board, which has a low jitter phase locked loop (PLL), clock dividers and triangle wave generator, generates a low jitter clock and a carrier signal. The chip, mounted on the auxiliary board, was implemented in 28nm CMOS process. Such a clock is also used by a logic analyzer (Tektronix TLA7012), which also captures the ΔΣM output bitstreams. The stored bitstreams are transferred to a PC for subsequent signal processing in MATLAB.

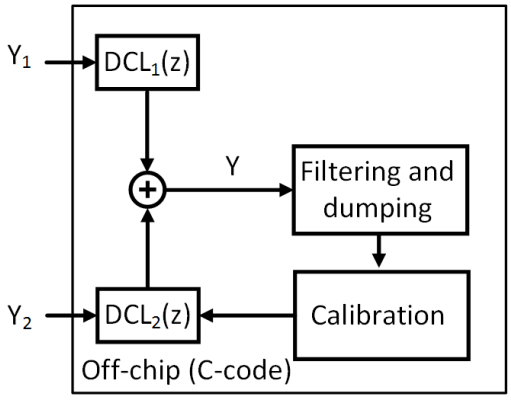
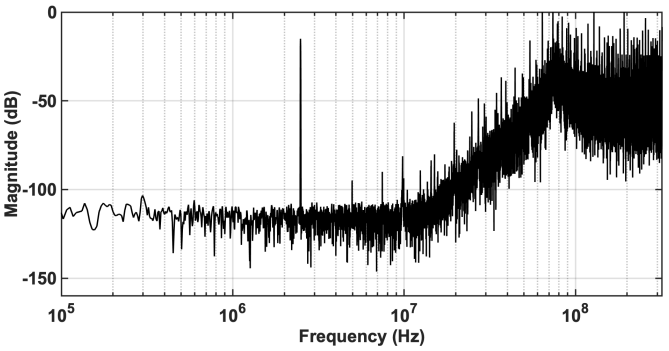


Fig. 6. Block diagram of the DCLs and the calibration block.

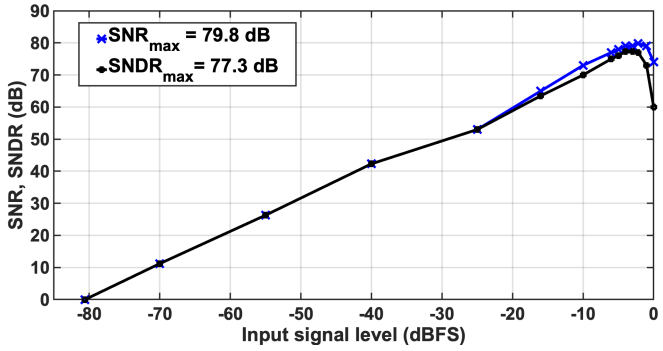
The DCL at the output of the first stage consists of a programmable delay, while the DCL for the second stage is the NTF of the first stage. The second stage DCL, i.e. DCL_2, essentially consists of FIR filter coefficients, fixed gains along with a variable gain for calibration purposes. During the calibration phase of the DCLs, the modulator output should not contain any (AC) signal component [17]. As depicted in Fig. 6, the overall ΔΣM output is processed by a filtering and a dumping block to effectively removes out of band quantization noise. The resulting bit-stream now consists of in-band noise and DC-offset. The variance of the filtered and dumped bit-stream is then calculated by [17]:

$$P_Q = \frac{1}{N}\sum_{n=0}^{N-1} \mid y(n) \mid^2 - \mid \sum_{n=0}^{N-1} y(n) \mid^2 \qquad (11)$$

The calibration algorithm needs to effectively minimize P_Q. For a large mismatch between analog and digital filters, P_Q is large, and the quantization noise power level is higher than the thermal noise. Matching and lower the quantization noise power is improved by changing the variable gain of the DCL_2. This results in diminishing the P_Q such that at a certain



(a)



(b)

Fig. 7. Experimental results: (a) PSD of the proposed CT MASH $\Delta\Sigma$M, (b) SNR and SNDR versus input signal level.

TABLE I
PERFORMANCE AND COMPARISON WITH THE STATE OF THE ART

Ref. Architecture	[5] Double noise-shaping GROQ	[9] Two-stage VCOQ	[12] MASH VCOQ	[13] VCO DPLL	[18] VCO integrator	[19] CT VCOQ	This work
Technology (nm)	130	65	180	40	130	40	65
BW (MHz)	15	50	10	5.2	2	20	10
Fs (MHz)	640	1500	160	260	300	1024	640
SNR (dB)	81.7	76.1	79.1	71.7	68	62.1	79.8
SNDR (dB)	80.4	72.2	77.9	69.4	66.5	59.1	77.3
DR (dB)	82.9	76.1	80.9	72.3	–	63.1	81.7
Power (mW)	11.4	51.8	19.6	0.86	1.75	2.5	12
Area (mm^2)	0.17	0.35	1.19	0.086	0.03	0.02	1
$FOMS_{DR}$ (dB)	174.1	166	168	170.1	–	162.6	170.9
$FOMS_{SNDR}$ (dB)	171.5	162	164.97	167.2	157	158.6	167.8

Note: The carrier (triangle wave) generator power is not included in FOM computation.

gain the quantization noise level becomes lower than thermal noise and P_Q is minimized. Figure 7(a) shows the output spectrum of the proposed modulator with a -15-dBFS input tone (0-dBFS input of 250 mV) located at 2.48-MHz while clocked at 640 MHz. The SNR and SNDR of the modulator versus input signal level are shown in Fig. 7(b). Note that the main metrics are: SNR$=$ 79.8-dB, SNDR$=$ 77.3-dB, and DR$=$ 81.7-dB. Therefore, the corresponding Schreier FOM, as defined in [1], are 170.9-dB and 167.8-dB, respectively. We compare in Table I the performance metrics of the proposed $\Delta\Sigma$M with state-of-the-art VCO-based $\Delta\Sigma$Ms within the same range of signal bandwidths, showing one of the best FOMs.

V. CONCLUSION

A new approach to implement high-order CT MASH $\Delta\Sigma$Ms based on the use of GRO quantizers has been presented. The quantization error is extracted in time-domain, which allows to combine GRO-based quantization with conventional CT loop-filters. The proposed architecture can increase the noise shaping by extending the number of stages with GRO-based TDCs in a mostly-digital scaling-friendly approach. In order to probe the presented techniques, a CT MASH 3-1 $\Delta\Sigma$M has been designed and integrated in 65-nm CMOS, featuring state-of-the-art performance.

REFERENCES

[1] S. Pavan, R. Schreier, and G. C. Temes, *Understanding Delta-Sigma Data Converters*. John Wiley & Sons, 2017.
[2] M. Z. Straayer and M. H. Perrott, "A 12-bit, 10-MHz Bandwidth, Continuous-Time $\Sigma\Delta$ ADC With a 5-bit, 950-MS/s VCO-Based Quantizer," *IEEE J. of Solid-State Circuits*, vol. 43, no. 4, pp. 805–814, Apr. 2008.
[3] K. Reddy *et al.*, "A 54mW 1.2GS/s 71.5dB SNDR 50MHz BW VCO-based CT $\Delta\Sigma$ ADC using Dual Phase/Frequency Feedback in 65nm CMOS," in *Symposium on VLSI Circuits (VLSI Circuits)*, Kyoto, 2015, pp. C256-C257.
[4] W. Yu, K. Kim, and S. Cho, "A 0.22 ps rms Integrated Noise 15 MHz Bandwidth Fourth-Order $\Delta\Sigma$ Time-to-Digital Converter Using Time-Domain Error-Feedback Filter," *IEEE J. of Solid-State Circuits*, vol. 50, no. 5, pp. 1251–1262, May 2015.
[5] T. Kim, C. Han, and N. Maghari, "A 4th-Order Continuous-Time Delta-Sigma Modulator Using 6-bit Double Noise-Shaped Quantizer," *IEEE J. of Solid-State Circuits*, vol. 52, no. 12, pp. 3248–3261, Dec. 2017.
[6] A. Babaie-Fishani and P. Rombouts, "A Mostly Digital VCO-Based CT-SDM With Third-Order Noise Shaping," *IEEE J. of Solid-State Circuits*, vol. 52, no. 8, pp. 2141–2153, Aug. 2017.
[7] F. Cardes *et al.*, "A 0.04-mm^2 103-dB-A Dynamic Range Second-Order VCO-Based Audio $\Sigma\Delta$ ADC in 0.13-μm CMOS," *IEEE J. of Solid-State Circuits*, vol. 53, no. 6, pp. 1731–1742, Jun. 2018.
[8] E. Gutierrez *et al.*, "A Pulse Frequency Modulation Interpretation of VCOs Enabling VCO-ADC Architectures With Extended Noise Shaping," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 65, no. 2, pp. 444–457, Feb. 2018.
[9] S. Dey, K. Reddy, K. Mayaram, and T. S. Fiez, "A 50 MHz BW 76.1 dB DR Two-Stage Continuous-Time Delta-Sigma Modulator With VCO Quantizer Nonlinearity Cancellation," *IEEE J. of Solid-State Circuits*, vol. 53, no. 3, pp. 799–813, Mar. 2018.
[10] H. Maghami *et al.*, "A 0.2-V 30-MS/s 11b-ENOB Open-Loop VCO-Based ADC in 28-nm CMOS," *IEEE Solid-State Circuits Letters*, vol. 1, no. 9, pp. 190-193, Sept. 2018.
[11] H. Maghami *et al.*, "A Highly Linear OTA-Free VCO-Based 1-1 MASH $\Delta\Sigma$ ADC," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 66, no. 7, pp. 2440-2453, July 2019.
[12] M. Sadollahi and G. C. Temes, "A 10-MHz BW 77.9 dB SNDR DT MASH $\Delta\Sigma$ ADC With NC-VCO-Based Quantizer and OPAMP Sharing," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 66, no. 9, pp. 3384-3392, Sept. 2019.
[13] Y. Zhong et al., "A Second-Order Purely VCO-Based CT $\Delta\Sigma$ ADC Using a Modified DPLL Structure in 40-nm CMOS," *IEEE J. of Solid-State Circuits*, vol. 55, no. 2, pp. 356-368, Feb. 2020.
[14] M. Honarparvar *et al.*, "Design Considerations of MASH $\Delta\Sigma$ Modulators with GRO-Based Quantization," in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2018.
[15] B. K. Thandri and J. Silva-Martinez, "A Robust Feedforward Compensation Scheme For Multistage Operational Transconductance Amplifiers With No Miller Capacitors," *IEEE J. of Solid-State Circuits*, vol. 38, no. 2, pp. 237–243, Feb. 2003.
[16] M. Honarparvar, J. M. de la Rosa, and M. Sawan, "A 0.9-V 100-μW Feedforward Adder-Less Inverter-Based MASH $\Delta\Sigma$ Modulator With 91-dB Dynamic Range And 20-kHz Bandwidth,"*IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 65, no. 11, pp. 3675 - 3687, Nov. 2018.
[17] H. Shim, I.C. Park and B. Kim, "A hybrid delta-sigma modulator with adaptive calibration," in *Proceedings of the 2003 International Symposium on Circuits and Systems*, May 2003.
[18] K. Lee, Y. Yoon and N. Sun, "A Scaling-Friendly Low-Power Small-Area$\Delta\Sigma$ ADC With VCO-Based Integrator and Intrinsic Mismatch Shaping Capability," *IEEE J. on Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 4, pp. 561-573, Dec. 2015.
[19] A. Mukherjee *et al.*., "A 1-GS/s 20 MHz-BW Capacitive-Input Continuous-Time $\Delta\Sigma$ ADC Using a Novel Parasitic Pole-Mitigated Fully Differential VCO," *IEEE Solid-State Circuits Letters*, vol. 2, no. 1, pp. 1-4, Jan. 2019.